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New Single-Switch quadratic boost DC/DC converter with Low voltage stress for renewable energy applications

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Abstract: In this paper, a novel non-isolated Single-Switch Quadratic Boost Coupled-Inductor (SSQBCI) DC/DC converter with continuous input current and low voltage stress on the switching component is presented. The suggested structure is based on the traditional quadratic boost converter. In this new topology, to achieve an ultra-high voltage gain without large duty cycle, a Coupled-Inductor (CI) along with a Voltage Multiplier (VM) are employed. The magnetic energy stored in the leakage inductor of the CI is recycled by a regenerative passive clamp capacitor that is connected with the switch in parallel, which helps to limit the maximum voltage across the switch. Therefore, to reduce the switch conduction loss and improve the efficiency, a switch with the low static drain-to-source ON-resistance can be used. Moreover, the low voltage stress on the output side diode alleviates the reverse recovery loss. The steady-state operating principle, comparisons with other related topologies and also design considerations in Continuous Conduction Mode (CCM) will be analyzed in detail. Finally, the performance of the proposed SSQBCI is verified by experimental results using a prototype with 30V input and 200V - 160 W output operation at a constant switching frequency 50 kHz.

1 Introduction

Nowadays, renewable energy sources (RES), such as fuel cells and Photovoltaic (PV), are being considered and developed rapidly in the modern society. Since such sources provide low voltage levels (<50 V), the use of step-up converters as an interface circuit is common to convert into higher voltages for many applications. In this context, given the importance of continuous input current that limits EMI problems, current-fed strategies of step-up converters are a more suitable choice for the RES to extract the maximum power [1]. The other key indicators of such converters for proper performance are high voltage gain ratio, low voltage stress, high efficiency, and low cost [2].

Theoretically, the traditional DC/DC step-up converters with continuous input current such as boost, CUK, and SEPIC can provide a step-up voltage gain for the RES. However, in practice, because of the limitation of the voltage gain ratio, often a very high duty cycle is required in these converters. This leads to a dramatic increase in switching loss and diode reverse recovery problems. So due to high power losses and low efficiency, the voltage gain ratio is severely limited (< 5). As a result, it is necessary to design converters with improved key performance indicators.

To solve this problem, by applying some voltage boosting techniques such as Voltage Lift, Voltage Multipliers (VM) cells, switched-capacitors/inductors, and also combining techniques, various types of step-up converters have been introduced to enhance the voltage conversion ratio of the DC-DC converters [2]. These converters can achieve a higher voltage gain than the traditional step-up converters. Nevertheless, the use of a large number of passive components will be necessary for wider voltage gain applications. These lead to increased cost and complexity of such converters.

In recent years, utilizing Coupled-Inductor (CI) as a valuable component allows the voltage gain ratio of converters to be enhanced in a wider range with the help of a turn's ratio besides the duty cycle. So far, much work of step-up converters based on CI along with other voltage boosting techniques especially VMs have been done to increase the voltage gain of DC-DC converters [2, 3]. It is noteworthy that, the energy stored in the leakage inductor of the CI leads to a high voltage spike on the switching components. This problem can be alleviated by using clamp capacitors (active or passive) in parallel with the switch [4, 5]. It can be pointed out that the passive clamp circuit is simpler than an active clamp circuit and has almost no effect on the control system. Moreover, because of the reflected current effect on the primary side, the coupling of the CI series with the DC input source leads to an increase in the ripple of the input current which increases the EMI problem [3]. Therefore, it is better to apply the CI in the middle stage of the circuits, to be more applicable in the RES.

A simple approach for further extension of the voltage conversion ratio of DC-DC converters with maintaining continuous input current is a cascading connection of two or more simple step-up converters. Cascading of two basic boost converters, which is called quadratic boost, is capable to extend the voltage gain ratio as a quadratic function of the duty cycle [6]. However, in this converter, the second power switch suffers from high voltage stress, which is equal to the output voltage. So far, various modified structures of quadratic boost converters have been presented in scientific papers [4, 7–10]. However, the voltage gain of these converters has not improved significantly.

In recent years, the use of magnetically CI along with VMs has been a favorite candidate to further extension of the voltage gain ratio of quadratic boost converters [11–31]. In [11] a new single switch quadratic boost converter with continuous input current is introduced. However, the mentioned converter can reach an ultra-high voltage gain with the use of a large number of semiconductor components. In [5, 12] new quadratic high step-up DC-DC converters with active clamp capacitors are suggested. In these converters using three magnetic cores, soft switching conditions are achieved. The voltage rate limitation is the main important disadvantage of these topologies. In [13–15] several types of modified quadratic boost base converters are suggested. However, the mentioned converters have demerits including limitation of the voltage conversion ratio along with high ripple input current. Three different types of single-switch quadratic high step-up DC-DC converter with VM and passive clamp capacitor are proposed in [16–18]. Voltage gain ratio limitation is the main important drawback of these topologies. Recently an ultra-high gain DC-DC

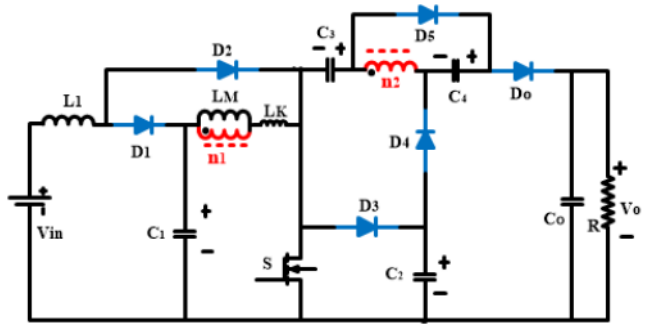

Fig. 1 *Circuit configuration of the proposed SSQBCI*

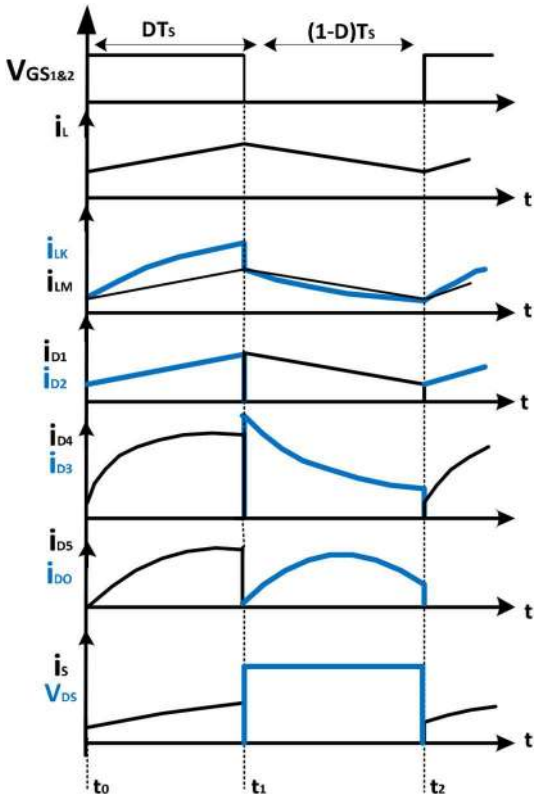

Fig. 2 *Theoretical key waveforms of the proposed SSQBCI*

converter with extendable voltage gain is presented in [19]. Input current with large ripples along with the use of a large number of switching devices are the main demerits of this converter, which limits its application for the RES. Moreover, in [20] a new CI-based high gain converter with active snubber with low voltage stress on the devices is suggested. The mentioned converter has demerits including the use of a large number of semiconductor components. In [21–23] quadratic based hybrid cascade converters are presented. Despite the low voltage rate on the power switch, the voltage conversion ratio is not significantly extended. In addition, other types of single switch step-up converters based on quadratic boost converter are suggested in [24–27]. In these topologies, using the switched-capacitor technique and CI the voltage gain is enhanced significantly. However, an input current with large ripple limits the application of the converter [26]. A new high step-up converter with quadratic voltage gain based on cascading boost and buck-boost is introduced in [28]. In this converter, using two power switches with simultaneous operation along with a CI, an ultra-high step-up/step-down voltage conversion ratio is obtained. In [29, 30], high voltage gain DC-DC converters integrating CI and diode–capacitor techniques with high voltage gain are suggested. Furthermore, a family of high step-up cascade DC-DC converters with CI and clamped circuits is introduced in [31]. In this converter to decrease the voltage stress and volume of the output capacitor, more capacitors in series instead of a single output capacitor are used.

Based on the above aspects in the development of quadratic boost converter, the aim of this work is to propose a new modified single-switch step-up converter (SSQBCI) with outstanding benefits including ultra-high voltage conversion ratio, low input current ripple, and high efficiency. Therefore, the suggested strategy is more useful for applications in the RES. The proposed SSQBCI is based on a quadratic hybrid cascaded connection along with CI and VMs. Moreover, the voltage rate across the single power switch is limited by a regenerative passive clamp capacitor. Hence, the energy stored in the leakage inductor also increases the voltage gain further. Moreover, another merit of the proposed converter is the low voltage stress across the output diode. These low voltage stress levels on the switching components enhance the efficiency of the converter.

This work is organized as follows: circuit description of the proposed converter is presented in Section 2. DC performance analysis and comparative analysis with other topologies are discussed in Sections 3 and 4. Design guidance of the SSQBCI is given in Section 5. Hardware results and discussion are shown in Section 6. Finally, a brief conclusion is drawn.

2 Circuit description

Fig. 1 illustrates the circuit structure of the proposed SSQBCI. This circuit is the combination of two main parts including a traditional quadratic boost converter and a magnetically CI with a VM. The introduced SSQBCI comprises a power switch (S), an input inductor (L_1), a CI, six diodes (D_1, D_2, D_3, D_4, D_5, and D_o) and five capacitors (C_1, C_2, C_3, C_4, and C_o). Moreover, in order to limit the voltage rate on the single power switch, a regenerative passive clamp capacitor C_2 is used. As a result, the energy of the leakage inductor can be recycled in the balancing capacitor C_3 that helps to further increase of voltage gain. To simplify the circuit analysis of the SSQBCI, the following assumptions are made:

(i) All switching devices are considered ideal.
(ii) All capacitors are sufficiently large, so their voltages are assumed constant without a ripple.
(iii) The magnetically CI is modeled with an ideal transformer along with a parallel magnetizing inductor (L_m) and a series merged leakage inductor (L_k) in the primary side with turns ratio 1:n ($n = n_2/n_1$) and coupling-coefficient $K = L_m/(L_m + L_k)$.
(iv) The input and magnetizing inductances are considered large enough with CCM operation, thus their currents are ripple-free.

According to the aforementioned assumptions, some theoretical key waveforms of the introduced converter under CCM operation for one switching period are depicted in Fig. 2. Furthermore, the corresponding equivalent circuits of the two operating modes are shown in Figs. 3*a* and *b*.

***Mode I [t_0 _ t_1]*:** The first mode starts by turning the single power switch S at $t = t_0$. At the same time, diodes D_2, D_4 and D_5 conducts, while diodes D_1, D_3 and D_o are blocked. Fig. 3*a* shows the equivalent circuit and current direction in this interval. The input and magnetizing inductors (L_1 and L_M) receive energy from the input voltage source and the capacitor C_1 respectively, then their current increase linearly. Meanwhile, the energy saved in the regenerative clamp capacitor C_2 is transferred to the balancing capacitor C_3.During this stage, the capacitor C_4 received energy from the secondary-side leakage inductor. Then, the current of the diode D_5 is increased in sinusoidal form. In addition, the output capacitor C_o is discharged to the output load. The following equations can be written in this mode:

$$V_{L1} = V_{\text{in}} \tag{1}$$

$$V_{\text{LM}} = K(V_{C1}) \tag{2}$$

$$V_{C3} = V_{C2} + nV_{\text{LM}} \tag{3}$$

$$V_{C4} = nV_{LM} \tag{4}$$

***Mode II [t_1 - t_2]*:** At the time $t = t_2$, the power switch S is turned OFF. The diodes D_1, D_3, and D_o are forward biased. As it is shown in Fig. 3*b*, the energy saved in the input and the magnetizing inductors are released to the capacitors C_1 and C_2, respectively. Then, their current start to decrease linearly. During this time interval, the voltage stress of the main power switch S is limited by the voltage of clamp capacitor C_2. Moreover, the energy of the capacitors C_3 and C_4 along with the secondary-side of the CI transferred to the output capacitor C_o. In this mode, the following equations are given:

$$v_{L1} = V_{in} - V_{C1} \tag{5}$$

$$v_{LM} = K(V_{C1} - V_{C2}) \tag{6}$$

$$v_o = V_{C2} + V_{C4} + V_{C3} + nV_{LM} \tag{7}$$

3 DC performance analysis

3.1 Output-Input voltage conversion ratio

In order to simplify the DC performance analysis, all assumptions in Section 2 are considered. Using the volt-second balance principle on the input and magnetizing inductors (L_1 and L_M), the voltage of the capacitors C_1 and C_2 are obtained as follows:

$$V_{C1} = \frac{V_{in}}{1-D} \tag{8}$$

$$V_{C2} = \frac{V_{C1}}{1-D} = \frac{V_{in}}{(1-D)^2} \tag{9}$$

Here, D is the duty cycle of the power switch S. On the other hand, by writing KVL in Mode I and also using (2) and (4), the voltage of the balancing capacitor C_3 is expressed as:

$$V_{C3} = \frac{1 + nK(1-D)}{(1-D)^2} V_{in} \tag{10}$$

Moreover, using (2), (4) and (8) in Mode I, the voltage of the capacitor $C4$ is derived as:

$$V_{C4} = nK\frac{V_{in}}{1-D} \tag{11}$$

By substituting (7) and (8)–(11) into (7), the static output-input voltage conversion ratio of the proposed SSQBCI is obtained as follows:

$$M_{CCM} = \frac{2 + n(1 + K - KD) + n(1-D)(1-K)}{(1-D)^2} \tag{12}$$

Fig. 4 illustrates the voltage gain ratio of the proposed SSQBCI versus the duty cycle, different turn's ratios of CI and coupling-coefficients (K). One can see that the proposed converter has a high potential to increase the voltage ratio as a semi-quadratic function by choosing a suitable turn's ratio (n) and duty cycle (D). In addition, it is clear that the voltage conversion ratio does not change considerably under various coupling-coefficients. Consequently, the ideal voltage gain of the SSQBCI at $k = 1$ is given as:

$$M_{CCM(ideal)} = \frac{2 + n(2-D)}{(1-D)^2} \tag{13}$$

3.2 Voltage stresses

The voltage stress on the switching components strongly influences the proper selection of converter components. Referring to the

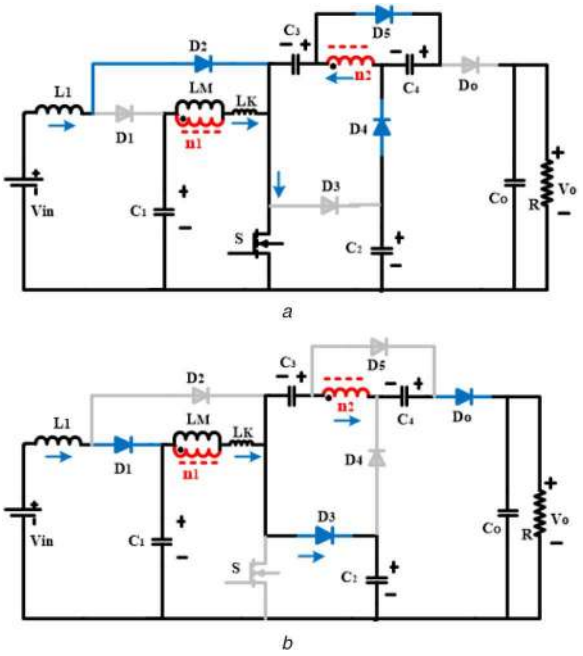

Fig. 3 *Current flow path of the proposed SSQBCI in each operating mode in CCM operation*
(a) Mode I (t_0–t_1), ***(b)*** Mode II (t_1–t_2)

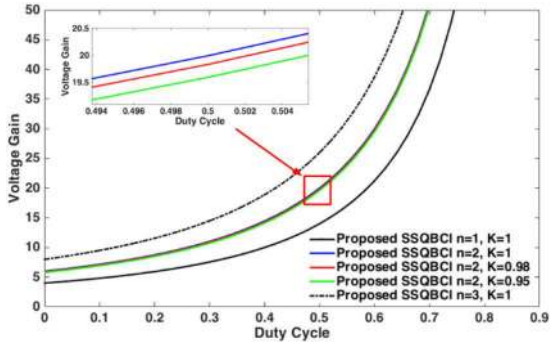

Fig. 4 *Voltage gain of the proposed SSQBCI versus the duty cycle for various turns' ratios of the CI and coupling-coefficients*

previous steady-state description of CCM operating modes, drain-source voltage of the main power switch of the SSQBCI, which is clamped by the capacitor C_2, is obtained as follows:

$$V_{DS} = \frac{V_o}{2 + n(2-D)} \tag{14}$$

Moreover, the maximum peak reverse voltage of the diodes D_1, D_2, D_3, D_4, D_5, and D_o are achieved respectively as:

$$V_{D1} = \frac{(1-D)V_o}{2 + n(2-D)} \tag{15}$$

$$V_{D2} = \frac{DV_o}{2 + n(2-D)} \tag{16}$$

$$V_{D3} = \frac{V_o}{2 + n(2-D)} \tag{17}$$

$$V_{D4} = V_{DO} = \frac{(1+n)V_o}{2 + n(2-D)} \tag{18}$$

$$V_{D5} = \frac{nV_o}{2 + n(2-D)} \tag{19}$$

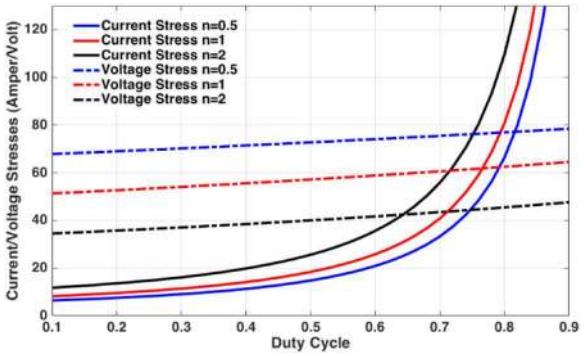

Fig. 5 *Voltage and current rates on the main power switch versus the duty cycle and turns ratio of CI (V_{out} = 200 V and R_{load} = 250 Ω)*

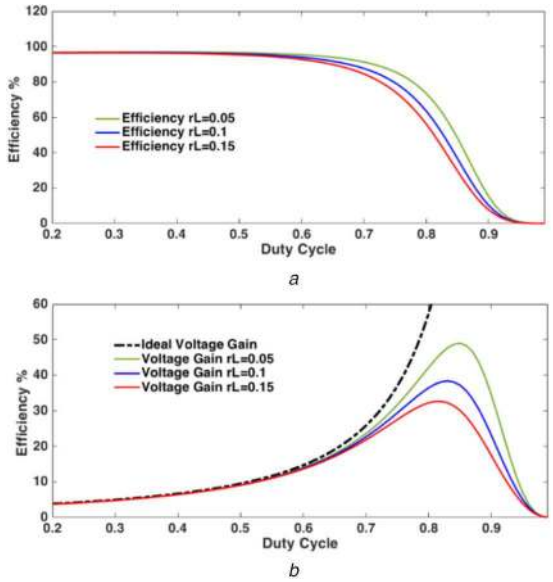

Fig. 6 *Proposed SSQBCI in non-ideal conditions under various input inductor ESRs.*
(a) Calculated efficiency, and, ***(b)*** static voltage gain

It is clear from (15)–(19) that increasing the turn's ratio of the CI (n) leads to a decrease in the voltage stress on switching components.

3.3 Current stresses of the semiconductors

Ignoring the current ripple of magnetic devices in CCM operation, the average value of the magnetizing inductor current is given as follows:

$$I_{\mathrm{LM(AVG)}} = \frac{2+n}{1-D} I_O \tag{20}$$

Here, I_o is the output load current. Moreover, the current stresses passing through on the power switching components are given as follows:

$$I_{D1\mathrm{MAX}} = I_{D2\mathrm{MAX}} = I_{\mathrm{in(AVG)}} \tag{21}$$

$$I_{D3(\mathrm{MAX})} = I_{D0\mathrm{MAX}} \simeq \frac{I_O}{(1-D)} \tag{22}$$

$$I_{D4(\mathrm{MAX})} = I_{D5(\mathrm{MAX})} \simeq \frac{I_O}{D} \tag{23}$$

$$I_{S(\mathrm{MAX})} = \frac{n(2-D)+1+2D-D^2}{\mathrm{D}(1-D)^2} I_O \tag{24}$$

Fig. 5 depicts the voltage and current rating of the power switch of the proposed SSQBCI versus duty cycle and different turn's ratio of the CI at V_{out} = 200 V and R_{load} = 250 Ω. It is clear from the figure that, voltage and current stresses depend on the variation of the turn's ratio (n) of the CI. With the increase in n, the switch voltage stress is decreased while the current stress of the power switch is increased. Also, the appropriate range of duty cycle to induce the lower values of voltage and current stresses is for $D < 0.55$.

3.4 Analysis of theoretical efficiency

Generally, based on the parasitic resistors in the circuit components, the theoretical efficiency of the converter can be estimated. The main parasitic elements of the proposed converter components are listed as follows:

(i) r_{L1} and $r_{L\mathrm{m}}$ are the Equivalent Series Resistance (ESR) of the input and magnetizing inductors.
(ii) $R_{\mathrm{ds(on)}}$ is the static drain-to-source *ON*-resistance of the switch S .
(iii) t_{on} and t_{off} denote the time of turn-off and turn-on transition of the MOSFET.
(iv) r_{C1}, r_{C2}, r_{C3}, r_{C4}, and $r_{C\mathrm{o}}$ represent the ESR of converter capacitors, respectively.
(v) VF1, VF2, V_{F3}, V_{F4}, VF5 and VFo are the threshold voltage of the diodes.

The switch power losses of the SSQBCI are given by:

$$P_{\mathrm{SW(Cond.)}}^{\mathrm{Loss}} = R_{\mathrm{ds(ON)}} \cdot I_{s(\mathrm{RMS})}^2 + \frac{1}{2T_S}[I_S V_{\mathrm{DS}}(t_{\mathrm{on}} + t_{\mathrm{off}})] \tag{25}$$

Where, I_S is the value of the MOSFET current at the switching instant. The copper dissipation of the proposed converter is expressed as:

$$P_{\mathrm{Mag.(Copper)}}^{\mathrm{Loss}} = r_{L1} I_{L1(\mathrm{RMS})}^2 + r_{\mathrm{LM}} I_{\mathrm{LM(RMS)}}^2 \tag{26}$$

Moreover, the power loss of the body diode in the on-state is calculated as:

$$P_{\mathrm{Diode}}^{\mathrm{Loss}} = V_F I_{D(\mathrm{AVG})} \tag{27}$$

It can also be pointed out that the threshold voltage of diodes often enhances at higher current levels. Furthermore, the power loss in the capacitor is given as follows:

$$P_{\mathrm{Cap.}}^{\mathrm{Loss}} = r_{\mathrm{ESR}} I_{C(\mathrm{RMS})}^2 \tag{28}$$

The theoretical efficiency and voltage gain plots of the proposed SSQBCI versus duty cycle variations and several ESR of the input inductor are depicted in Figs. 6*a* and *b*. The value of converter parameters are considered as: V_{in} = 30 V, R_{Load} = 700 Ω, r_{Lm} = 50 mΩ, f_s = 50 kHz, $t_{d(\mathrm{off})}$ = 20 ns, $t_{d(\mathrm{on})}$ = 15 ns, $r_{\mathrm{ds1,2(ON)}}$ = 18 mΩ, $r_{D1} = r_{D01} = r_{D02}$ = 7 mΩ, $r_{\mathrm{esrC1\&2}}$ = 20 mΩ, $r_{\mathrm{esrC3\&4}} = r_{\mathrm{esrCo}}$ = 50 mΩ, $V_{F1} = V_{F01} = V_{F02}$ = 0.5 V and n = 0.25. It is clear that by decreasing the duty cycles or the use of smaller values of the input inductor, the efficiency is improved.

Moreover, at high duty cycles, the voltage gain ratio of the proposed converter increases as an exponential function, which leads to a dramatic increase in the load current. As a result, both the efficiency and voltage gain of the converter drop suddenly at high range of duty ratios.

4 Comparative analysis

In this section, to demonstrate the benefits of the proposed converter, some comparisons with relevant recent topologies published in articles are presented. Table 1 compares several typical performance indicators consisting of voltage conversion ratio, the number of components, input current ripple, the voltage

Table 1 Performance comparison of the quadratic step-up DC-DC converters

Converter Topology	No. of Components S	D	C	CI + L	T	Voltage Gain	Input Current Ripple	Voltage Stress on Switches	Voltage Stress on Output Diodes	Efficiency 150 W
[11]	1	7	6	1 + 2	17	$\frac{2(2+n)}{(1-D)^2}$	Low (0.59 A)	$\frac{V_o}{2+n}$	$\frac{(1+n)V_o}{2+n}$	89.7%
[12]	1	6	4	1 + 2	14	$\frac{1+nD}{(1-D)^2}$	Low (1.27 A))	$\frac{V_o}{1+nD}$	$\frac{(2+D(n-1))V_o}{1+nD}$	93.34%
[20]	2	6	6	1 + 1	16	$\frac{1+2n}{(1-D)^2}$	Low (1.11 A)	$\frac{V_o}{1+2n}$	$\frac{nV_o}{1+2n}, \frac{nV_o}{1+2n}$	94.11%
[21]	1	4	3	1 + 1	10	$\frac{1+nD}{(1-D)^2}$	Low (1.27 A)	$\frac{V_o}{1+nD}$	$\frac{(2+D(n-1))V_o}{1+nD}$	93.00%
[22]	1	4	3	1 + 1	10	$\frac{1+nD}{(1-D)^2}$	Low (1.27 A)	$\frac{V_o}{1+nD}$	$\frac{(2+D(n-1))V_o}{1+nD}$	94.18%
[23]	1	5	3	1 + 2	12	$\frac{1+nD}{(1-D)^2}$	Low (1.27 A)	$\frac{V_o}{1+nD}$	$\frac{(1+D(n-1))V_o}{1+nD}$	92.4%
[24]	1	6	5	1 + 1	14	$\frac{n(3D+2)+(2-D)}{2(1-D)^2}$	Low (1.19 A)	$\frac{(2+D(n-1))V_o}{n(3D+2)+(2-D)}$	$\frac{2nV_o}{n(3D+2)+(2-D)}$	91.6%
[25]	1	5	4	1 + 1	12	$\frac{(1+n)(1+D)}{(1-D)^2}$	Low (1.04 A)	$\frac{V_o}{(1+n)(1+D)}$	$\frac{V_o}{(1+D)}$	94.9%
[26]	1	6	5	1 + 1	14	$\frac{2+n+nD}{(1-D)^2}$	High (16 A)	$\frac{V_o}{2+n+nD}$	$\frac{(1+n)V_o}{2+n+nD}$	94.8%
[27]	1	6	5	1 + 1	14	$\frac{1+n(2-D)}{(1-D)^2}$	Low (1.17 A)	$\frac{V_o}{1+n(2-D)}$	$\frac{nV_o}{1+n(2-D)}$	93.25%
[28]	2	3	3	1 + 1	10	$\frac{(1+n)D}{(1-D)^2}$	Low (1.63 A)	$\frac{(1-D)V_o}{(1+n)D}$	$\frac{nV_o}{(1+n)D}$	93.6%
[29]	1	5	4	1 + 1	12	$\frac{2+n}{(1-D)^2}$	Low (1.00 A)	$\frac{V_o}{2+n}$	$\frac{(1+n)V_o}{2+n}$	95.0%
[30]	1	6	5	1 + 1	14	$\frac{1+n+nD}{(1-D)^2}$	Low (1.15 A)	$\frac{V_o}{1+n+nD}$	$\frac{nV_o}{1+n+nD}$	93.60%
Proposed Converter	1	6	5	1 + 1	14	$\frac{2+n(2-D)}{(1-D)^2}$	Low (0.95 A)	$\frac{V_o}{2+n(2-D)}$	$\frac{(1+n)V_o}{2+n(2-D)}$	95.2%

S = Switch, **D** = Diode, **C** = Capacitor, **CI** = Coupled-Inductor, **L** = inductor, **T** = Total Device Count.

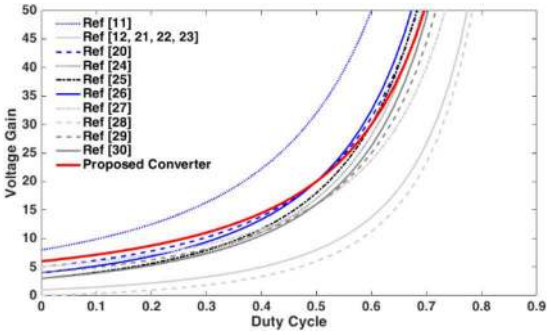

Fig. 7 *Voltage gain comparison of the referenced converters in Table 1 (n = 2)*

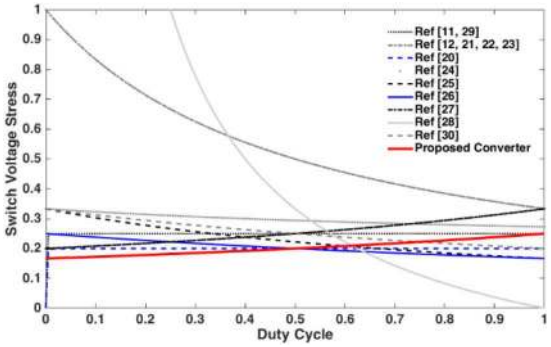

Fig. 8 *Comparison of normalized voltage stress across the power switch of the referenced converters in Table 1 (n = 2)*

stress on switch and output diode and also efficiency of the proposed SSQBCI and other converters.

A quantitative comparison for the input current ripple of the converters is provided in the same working point (20 V-200 V, f_s = 50 kHz and L_{in} = 250 uH and n = 0.5), which are shown in Table 1. According to this table, the only converter in [11] with higher voltage gain has a lower current ripple value than the proposed converter. However, this converter has been forced to use a large number of semiconductor components. For other cases, the proposed converter has a lower input current ripple against the other converters.

Fig. 7 depicts a line chart of the ideal voltage gain ratio over full operation range of duty cycles of the introduced SSQBCI compared with the converters described in Table 1 under turns ratio $n = 2$. As seen from the graph, just converter in [11] has a higher voltage conversion ratio than the proposed converter for all ranges of the duty cycles. However, it is clear from the comparison Table 1, this converter has been forced to use a large number of semiconductor components. In other cases, the proposed SSQBCI can provide a higher voltage gain ratio than the other related converters at the duty cycle range $0 < D < 0.5$.

It is noteworthy that the performance of the step-up converters in high duty cycles should be avoided due to the sharp increase in the power losses of the switching components. Moreover, the normalized maximum voltage rate on the main power switch versus the duty cycle under the same conditions ($n = 2$) of the referenced converters in Table 1 is plotted in Fig. 8. According to this figure, the maximum voltage stress of the presented SSQBCI is at the lowest level in comparison to the other converters at the duty cycle range $0 < D < 0.5$. This leads to the choice of a MOSFET with lower drain-to-source resistance.

Furthermore, Fig. 9 expresses the normalized maximum peak reverse voltage comparison across the output diode. As it is clear, in the SSQBCI, the voltage stress of the output diode is at a very low level, which helps to alleviate the reverse recovery and conduction losses. Moreover, a suitable indicator to evaluate power density is the ratio of the voltage conversion to the number of the

whole components (M/N). This indicator for the referenced converters in Table 1 is plotted in Fig. 10. It is apparent that the suggested SSQBCI exhibits a high value of the M/N ratio.

The comparison of the overall theoretical efficiency between the proposed converter and the other converters have been also done in Table 1. These efficiencies are exactly calculated under the same conditions of working point, including the input and output voltages (30 V/200 V), output power (150 W), switching frequency (50 kHz), turns ratio ($n = 0.25$), and allowable input and magnetizing inductors current ripple (20 and 60%). The selection of parasitic resistances are based on IRFP series for MOSFETs, Aluminum Electrolytic Capacitors VISHAY for capacitors, Schottky barrier rectifier for diodes, EE Ferrite core, and Iron Powder Toroidal cores for CL and inductors, respectively. As it is shown, the proposed converter demonstrates enough high overall theoretical efficiency against the other converters because of its higher voltage gain, lower input, and magnetic inductors and low voltage stress.

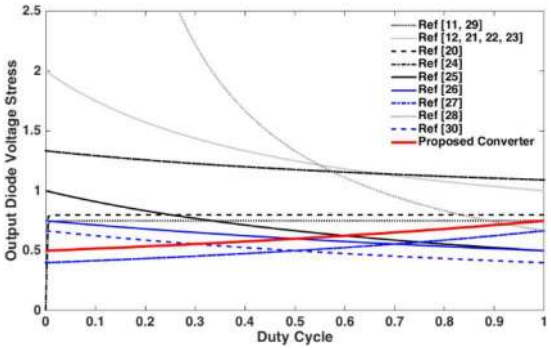

Fig. 9 *Comparison of normalized voltage stress on the output diode of the referenced converters in Table 1 (n = 2)*

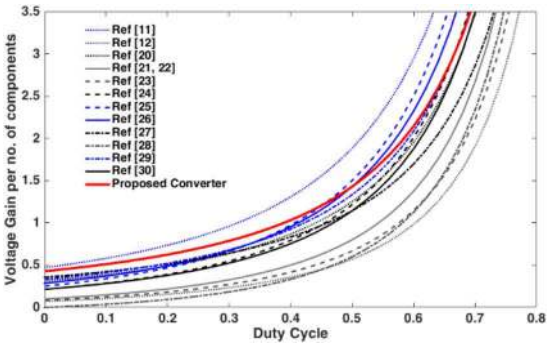

Fig. 10 *Comparison of the static voltage gain per number of components of the referenced converters in Table 1 (n = 2)*

To compare the costs of the referenced converters in Table 1, the devices price that are employed in the circuits should be obtained. Semiconductor elements in different current and voltage stresses are selected from the same brand, including the IRFP series from Vishay Siliconix for MOSFETS, BYV series from Vishay Semiconductors for diodes, ECA series from Panasonic industry for capacitors and toroid and ferrite cores from Micrometals for magnetic components. The estimated prices of devices are taken from *semic, mouser, newark* websites, which are summarized in Table 2. As it can be seen, the cost of the presented converter is just more than the converter in [29] and is at a low level.

It is clear from the above discussion that the proposed converter is more suitable for RES applications than other topologies due to the high voltage gain ratio along with low voltage stresses and a high M / N indicator.

5 Design guidance of the SSQBCI

An effective way for an appropriate selection of the turn's ratio of CI (n) and the duty cycle range (D) is to analyze the curve of the voltage and current stresses of power MOSFETs. For the proposed converter, based on Fig. 5, the best range for the duty cycle to have the minimum values of voltage/current stresses on the MOSFET is $0 < D < 0.55$. After determining the duty cycle, according to the required voltage gain, the turn's ratio of the CI can be calculated using (13) as follows:

$$n = \frac{M(1-D)^2 - 2}{2 - D} \tag{29}$$

Fortunately, the presented SSQBCI has an ultra-high voltage gain in quadratic form, as it does not require the use of magnetically CI with a large turn's ratio.

Continuous input current with a low ripple (CCM condition) in high step-up converters has an undeniable impact on a proper performance and extends the lifespan of the RES. The minimum value of the input inductor (L_1) of the SSQBCI is calculated based on the inductor energy saving equation as follows:

$$L_1 = \frac{V_{in} D}{\Delta I_{L1Max} f_s} \tag{30}$$

Here, ΔI_{L1max} is the maximum allowable current ripple that is often considered as 20% average value for the RES.

According to Fig. 1, the CI is located in the middle stage of the proposed circuit. Therefore, to reduce its dimensions, it can be designed under a larger allowable current ripple, which is also a reduced leakage inductance (L_K). Using (13) and (20) the minimum value of the magnetizing inductor L_M can be given as:

Table 2 Cost comparison of the quadratic step-up DC-DC converters

Conv.	Cores	Switches	Cost of Capacitors	Diodes	Total
[11]	$7.14	$1.61	$4.56	$4.39	$17.70
[12]	$6.91	$2.20	$4.04	$5.52	$18.67
[20]	$4.61	$6.9	$3.98	$3.78	$19.27
[21]	$4.61	2.20	$2.91	$2.61	$12.33
[22]	$4.61	$2.20	$3.03	$3.16	$13.00
[23]	$7.51	$2.20	$2.45	$4.08	$16.24
[24]	$4.61	$2.20	$3.77	$3.96	$14.54
[25]	$3.76	$2.20	$3.44	$3.28	$12.68
[26]	$3.76	$1.61	$3.79	$3.24	$12.40
[27]	$4.84	$2.20	$3.65	$3.95	$14.64
[28]	$5.25	$6.31	$2.45	$2.69	$16.70
[29]	$3.76	$1.61	$3.46	$2.75	$11.58
[30]	$4.61	$2.20	$4.01	$3.98	$14.80
Proposed	$3.76	$1.61	$3.77	$3.14	$12.28

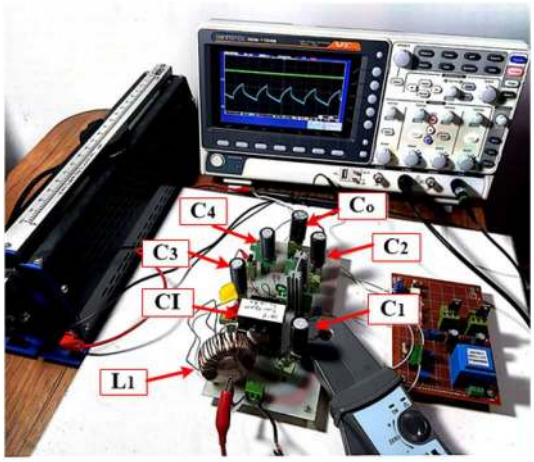

Fig. 11 *Photograph of the presented SSQBCI prototype*

Table 3 Specifications of the implemented prototype

Parameter	Values
output power(P_{out})	160 W
input voltage(V_{in})	30 V
output voltage(V_{out})	200 V
switching frequency(f_s)	50 kHz
capacitors	100 uF/200 V-250 V
power switch S	IRFB4227PbF with $R_{DS(ON)}$ = 19.7 mΩ, $t_{d(on)}$ = 33 ns, $t_{d(off)}$ = 21 ns
input inductor L_1	0.255 mH with r_{L1} = 55 mΩ (T184-52)
CI	EE42/21/15, n = 0.25
magnetizing inductor L_M	0.250 mH
Diode D_1, D_2, D_3 and D_5	MUR410/100 V With Maximum V_F = 0.89 in 4 A
Diode D_4 and D_o	MUR415/150 V With Maximum V_F = 0.71 in 3 A

$$L_M = \frac{V_{\mathrm{LM}} D}{\Delta I_{LM} f_s} > \frac{\mathrm{RD}}{(30-80)\%M(2+n)f_s} \tag{31}$$

The output capacitor (C_o), which limits the output voltage ripple to a reasonable range ($\Delta V_{Co} \approx 1\%\ V_o$), is selected based on the converter output power (P_o) and switching frequency (f_s) as:

$$C_0 = \frac{I_o D}{\Delta V_{C0} f_s} > \frac{P_o D}{1\%\,.\,V_o^2 f_s} \tag{32}$$

The other capacitors of the SSQBCI can be designed based on their maximum current along with the allowable voltage ripple as:

$$C_1 = \frac{(I_{\mathrm{LM}} + n(I_{D4} + I_{D5}))D}{\Delta V_{C1} f_s} > \frac{(2(D+n) - nD)I_0}{\Delta V_{C1}(1-D) f_s} \tag{33}$$

$$C_2 = \frac{I_{D4} D}{\Delta V_{C2} f_s} > \frac{I_0}{\Delta V_{C2} f_s} \tag{34}$$

$$C_3 = \frac{I_{D4} D}{\Delta V_{C3} f_s} > \frac{I_0}{\Delta V_{C3} f_s} \tag{35}$$

$$C_4 = \frac{I_{Do}(1-D)}{\Delta V_{C4} f_s} > \frac{I_0}{\Delta V_{C4} f_s} \tag{36}$$

In practice, larger electrolytic capacitances usually have a small equivalent series resistor (ESR). Thus, to reduce power dissipation and improve efficiency, the converter capacitors C_o- C_4 should be selected larger than the calculated values.

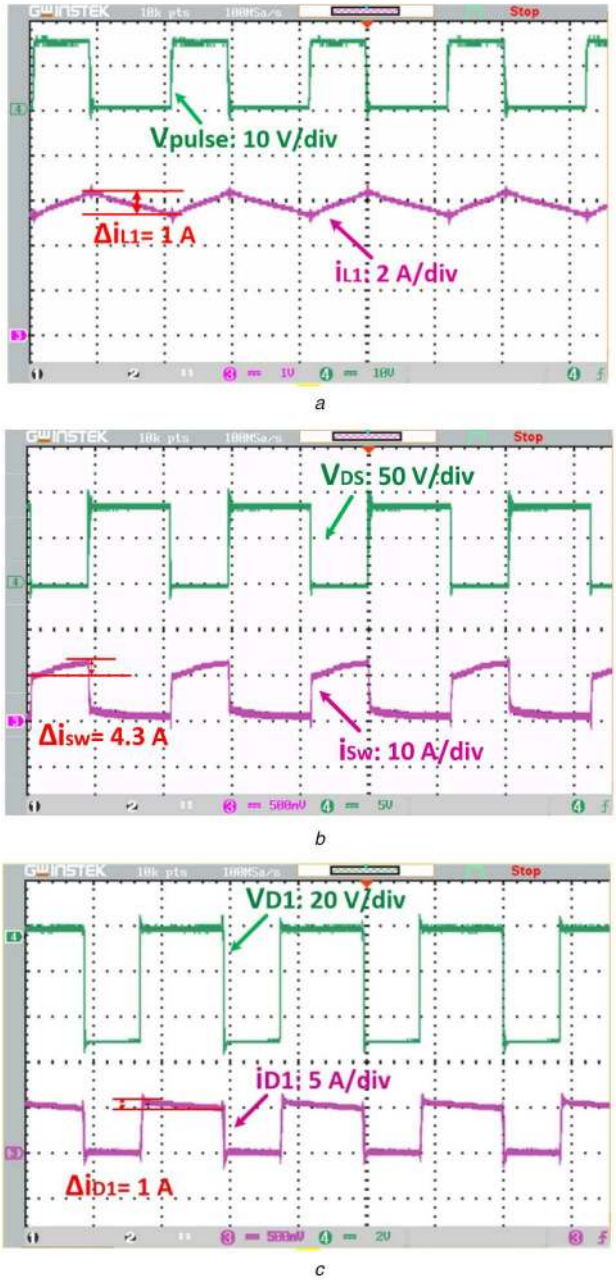

Fig. 12 *Experimental results of the SSQBCI. (Time/Dive = 10 us/div)* ***(a)*** V_{Pulse} and i_{L1}, ***(b)*** V_{DS} and i_S and, ***(c)*** V_{D1} and i_{D1}

6 Hardware results and discussion

To further validate the theoretical analysis of the introduced SSQBCI, a 160 W laboratory prototype is established, which is depicted in Fig. 11. Moreover, Table 3 gives the component details of the prototype. Based on the design guidance of the SSQBCI and prototype specifications, the duty cycle and turns ratio of the CI are considered as $D = 0.4$ and $n = 0.25$. To reduce the volume of energy storage devices, the switching frequency of the converter is selected to be 50 kHz. The magnetic cores of the input and the magnetizing inductors are iron powder toroidal core T 184-52 and ferrite core EE 42/21/15 with a 0.2 mm air gap, respectively. A high-frequency current probe PA-667 1 MHz was used to obtain the current waveforms. The introduced SSQBCI is operated at *CCM* and the experimental key waveforms of the SSQBCI prototype are shown in Figs. 12 and 13. The time division of the figures are same as *Time/DIV = 10* us.

The measured waveforms of the input inductor current along with the gate signal of the MOSFET in the time domain are shown in Fig. 12*a*. It can be seen that the current of the input inductor is continuous with small ripple $\Delta i_{L\mathrm{in}} = 1$ A (17.8% of the average), which is suitable for the RES. Furthermore, Fig. 12*b* depicts the

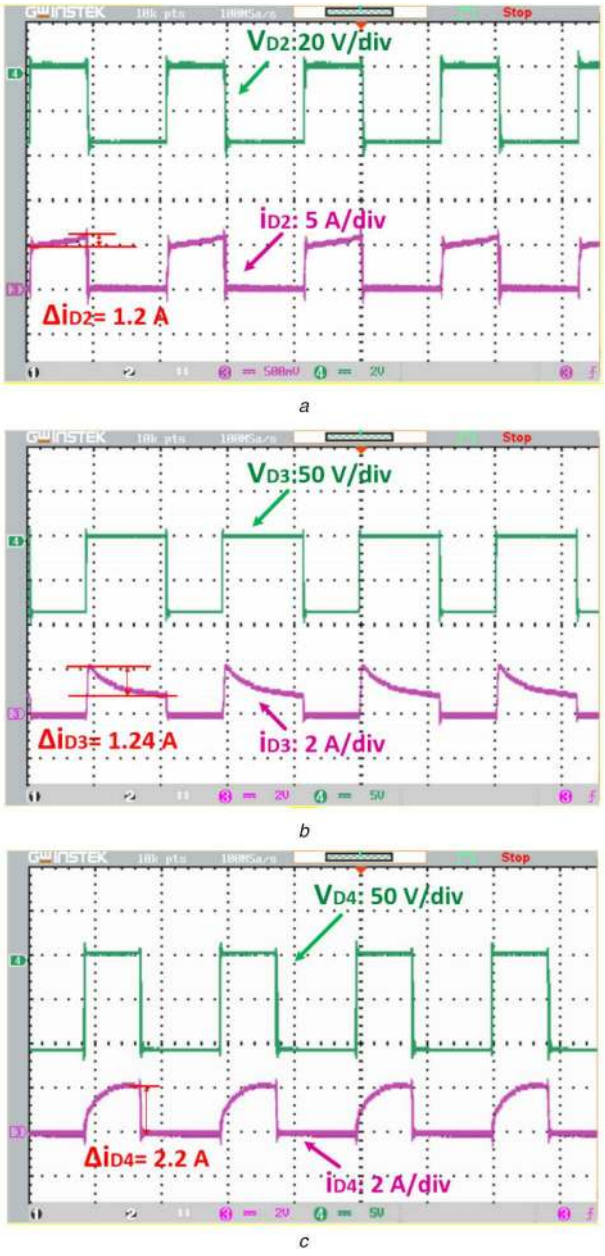

Fig. 13 *Experimental results of the SSQBCI, (Time/Dive = 10 us/div)* ***(a)*** V_{D2} and i_{D2}, ***(b)*** V_{D3} and i_{D3}, ***(c)*** V_{D4} and i_{D4}, ***(d)*** V_{D5} and i_{D5}

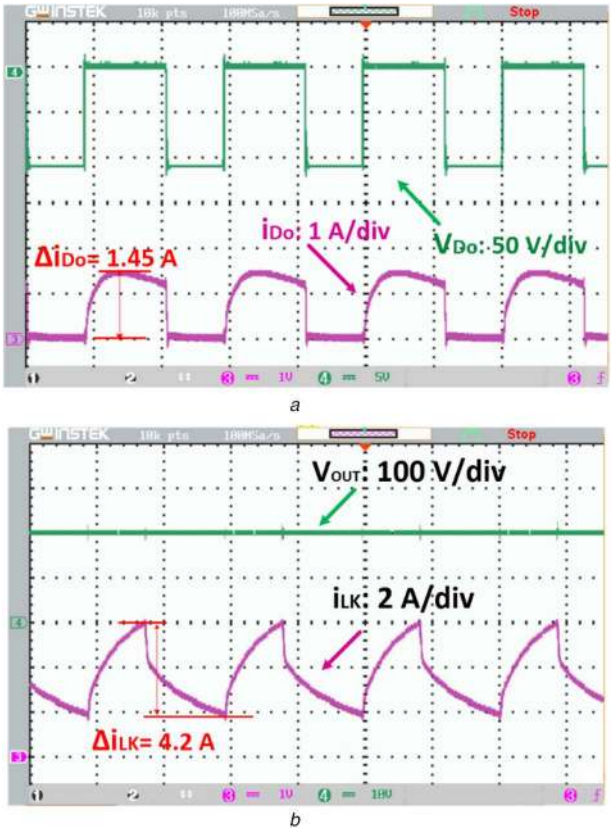

Fig. 14 *Experimental results of the SSQBC (Time/Dive = 10 us/div)* ***(a)*** V_{Do} and i_{Do}, ***(b)*** V_{out} and i_{LK}

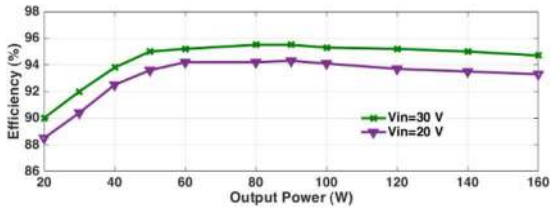

Fig. 15 *Measured efficiency versus several output power for two different input voltages*

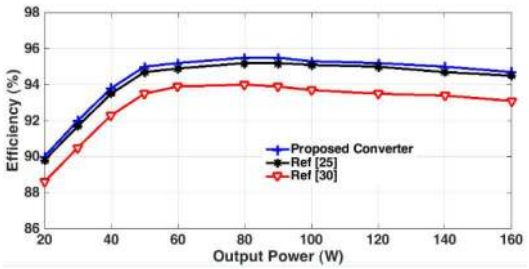

Fig. 16 *Experimentally compare of the efficiency of the SSQBCI, Ref [25] and Ref [30]*

measured voltage and current across in the power MOSFET. As it is shown, the voltage stress across the MOSFET is about 84 V, which is 42% lower than the output voltage. Furthermore, Fig. 12*c*, Figs. 13*a–d* and 14*a* show the experimental key waveforms of the voltage and current rates of the converter diodes (D_1–D_5 and D_o), which are close to the theoretical results. From Fig. 14*a*, the voltage rate of the output diode D_o is about 105 V, which is significantly smaller than the output voltage ($V_{\text{out}} = 200$ V) of the converter. The steady-state behavior of the converter output voltage and the primary-side current of the CI (the leakage inductor (i_{LK})) along with its current ripple are also shown in Fig. 14*b*. It should be noted that there is no need to design magnetic devices that located in the middle stage of the circuit with very little ripple. Because very low ripple requires the use the CI with very high magnetizing inductance, which leads to an increase in ohmic losses.

In addition, Fig. 15 shows the measured efficiency of the SSQBCI versus the output power variation (20 W–160 W). The efficiency is measured for two values of the input voltages $V_{\text{in}} = 20$ V and $V_{\text{in}} = 30$ V while maintaining the output voltage regulation ($V_{\text{out}} = 200$ V). The measured efficiency of the suggested converter at load power of 160 W at $V_{\text{in}} = 30$ V is about 94.7%. As it is clear in this figure, increasing the input voltage source, which leads to reduce the voltage gain, improves the converter efficiency.

The experimental efficiency results of the proposed converter prototypes against the converters in [25, 30] under various output powers $P_{\text{out}} = 20$ W–160 W are also presented in Fig. 16. It can be seen that the efficiency of the proposed converter is acceptable and very close to the converter [25] with twelve components. The converter in [30] has a lower efficiency than the proposed converter and Ref [25] because of the lower voltage gain ratio and higher switch voltage stress. Moreover, The break-down of power losses of the proposed converter components with the output voltage 200 V and the input voltages of 30 V based on the

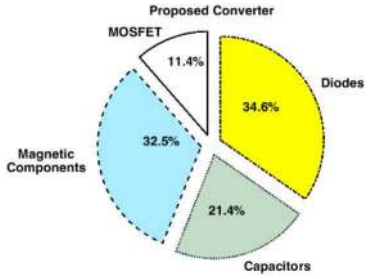

Fig. 17 *Break-down of power losses of the proposed converter at V_o = 200 V, P_{out} = 160 W under V_{in} = 30 V*

mentioned method in Section *IV* is calculated and illustrated in Fig. 17.

As is evident, due to the high current rate in the input section of the converter, the input and magnetizing inductors have dominant dissipation loss than other components.

7 Conclusion

In this paper, a new type of high step-up DC-DC converter with continuous input current has been proposed. The converter structure, which is based on the quadratic boost, utilizes a CI and VM to further lift the voltage gain. The presented topology can provide an ultra-high step-up voltage conversion ratio, input current with low ripple and also low voltage spikes on the semiconductor components. A regenerative passive clamp is adopted for limiting the voltage rate of the single power switch and recycling the energy storied in the leakage inductor. Also, because of the low voltage stress across the output diode, the reverse recovery loss of the output diode is alleviated. Circuit description, steady-state analysis, and the advantages of the suggested converter compared to other related converters have been discussed in details. Moreover, the experimental results of a sample prototype at P_o = 160 W with input voltage V_{in} = 30 V and the output voltage V_o = 200 V verified the feasibility of the introduced converter. All the aforementioned merits can prove that the proposed converter is a proper competitive option to be applied in the RES.

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