New Start-up Schemes for Isolated Full-Bridge Boost Converters

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***Abstract*—Two new start-up schemes for isolated full-bridge boost converters are proposed in this paper. The control timing for each scheme, which is compatible with pulse-width modulated (PWM) control timing for normal boost mode operation, are investigated. Design considerations on the relationship between the turns ratios of the boost choke windings and the main transformer windings, and its effects on the operation of the converter, are studied. The two proposed start-up schemes are experimentally verified on a 1.6 kW, 12 V/288 V prototype.**

***Index Terms*—Coupled-inductor, dc/dc, full-bridge, isolated boost converter, start-up scheme.**

I. Introduction

THE isolated full-bridge boost converter is attractive in applications such as single-stage power factor correction (PFC) with an isolation requirement and bi-directional dc–dc converters [1]–[4]. Similar to all other current-fed converters [5]–[7], the isolated full-bridge boost converter has several merits, including multi-output capability using one shared choke, and inherent over-current and short-circuit protection. The reasons why the isolated full-bridge boost converter has not been widely used so far can be attributed to (1) the requirement of an additional start-up circuit, and (2) the transformer leakage inductance that causes high transient voltage across the bridge switches [2], [3].

The purpose of using a start-up circuit for a boost-type converter is to establish an initial output voltage before the converter operates in the normal boost mode. The initial output voltage should not be lower than the input voltage (reflected). In a low power boost PFC pre-regulator, solutions such as putting a thermistor or resistor in parallel with a bypass switch, are normally chosen for the auxiliary start-up circuit. However, in a high-power isolated boost-type converter, the loss associated with the thermistor or resistor is not acceptable. An additional flyback winding, coupled with the boost choke, is needed to implement the start-up function.

A solution for the voltage spikes associated with the leakage inductance can be found by adding either an active or a passive clamping circuit. Although the circuit example shown in this paper is an active-clamp type, the proposed start-up schemes can be applied to passive-clamp and other types of isolated boost converters.

Manuscript received August 17, 2000; revised January 15, 2003. This work was supported by ERC Shared Facilities, the National Science Foundation under Award EEC-9731677, Oak Ridge National Lab, Oak Ridge, TN, Ford Scientific Research Lab, Dearborn, MI, and Ecostar, Deardorn, MI. Recommended by Associate Editor Y.-F. Liu.

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Digital Object Identifier 10.1109/TPEL.2003.813758

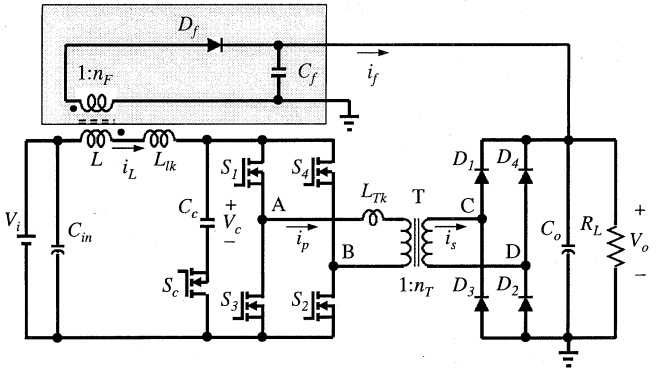

Fig. 1. Active-clamp isolated full-bridge boost converter with an auxiliary start-up circuit.

Two new start-up schemes for the active-clamp type isolated full-bridge boost converters are proposed in this paper. The control timing for each scheme, which are compatible with the control timing for normal boost mode operation, are investigated. Operation principles and steady-state analysis are discussed in Section II. Design considerations on the relationship between the turns-ratios of the boost choke windings and the main transformer windings, and its effects on the operation of the converter, are studied in Section III. Finally, the two proposed start-up schemes are experimentally verified using a 1.6 kW, 12 V/288 V prototype.

II. Proposed Start-Up Schemes

Fig. 1 shows the active-clamp isolated full-bridge boost converter with a start-up circuit shown in the shaded area. It consists of an additional flyback winding which is coupled with the boost choke, L, a high frequency rectifier diode, D_f, and a high frequency capacitor, C_f. The turns ratio of the flyback winding with respect to the boost choke is n_F. The active-clamp branch consists of the clamping switch, S_c, and capacitor, C_c, for transient voltage suppression. Switches $S_1 - \mathrm{S}_4$ constitute the full-bridge circuit.

A. Start-Up Scheme I

Fig. 2 is the functional logic diagram in Scheme I. It consists of both the start-up mode and the normal boost mode, and

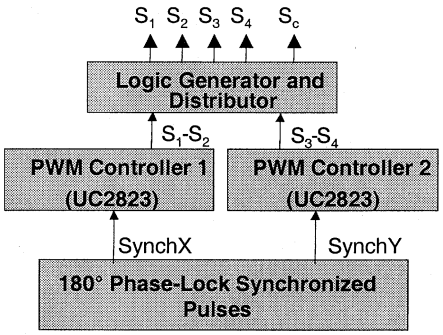

Fig. 2. Functional logic diagram (Scheme I).

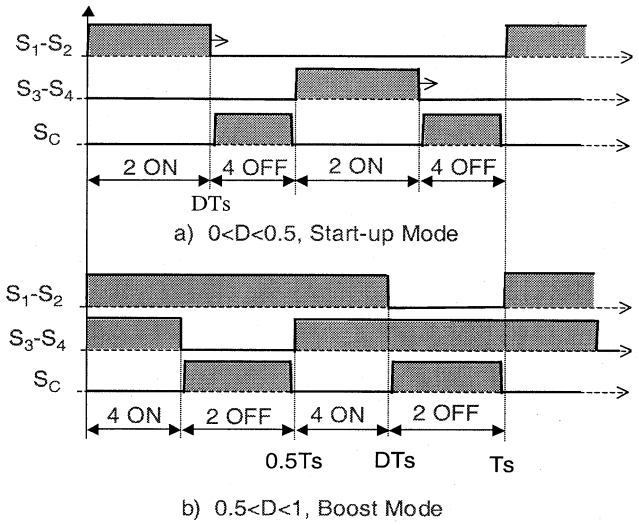

Fig. 3. Timing diagram for Scheme I.

includes two UC2823 PWM control chips, which are synchronized with 180° phase lock.

The timing diagram for start-up scheme I is shown in Fig. 3. Two independent PWM signals (S_1-S_2, S_3-S_4) from the two PWM control chips are synchronized with 180°-phase-shift. The duty cycle D of the two PWM signals is always identical and can vary from 0 to 1. When $0 < D < 0.5$, the circuit operates in start-up or "buck" mode. Once the output voltage is built up, the circuit can be switched to "boost" mode with $0.5 < D < 1$.

1) Start-Up Mode $(0 < D < 0.5)$*:* For $0 < \mathrm{D} < 0.5$, the converter operates in the start-up mode, and the flyback winding, n_F, feeds energy to the output side. Neglecting the short dead time between S_c and the main switches, S_1-S_4, two main intervals 2-ON interval and 4-OFF interval are involved in a switching cycle, as shown in Fig. 3.

Fig. 4 shows the two corresponding equivalent circuits of the two intervals. In the 2-ON interval, the diagonal switch S_1 and S_2 or S_3 and S_4, are turned on, the input energy is partially transferred to the output through the main transformer, T, and is partially stored in the choke, L. This is actually a buck-like interval, although the energy is stored in the primary side of the choke, L. In the 4-OFF interval, all four bridge switches, S_1-S_4, are turned off, energy stored in L is released through the flyback winding, N_f, to output. This is an active-clamp flyback-like interval. The detailed waveforms with the action of the

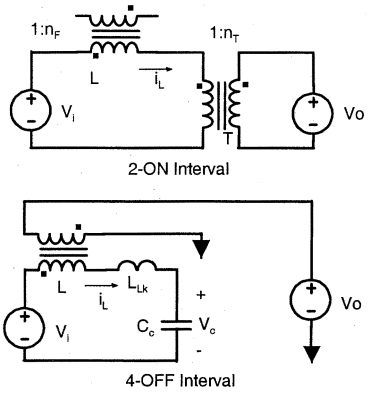

Fig. 4. Two equivalent circuits in start-up mode (Scheme I).

active-clamp branch considered are more complicated as discussed in [2], [3].

Based on the flux balance in choke L during one switching cycle T_s, the steady-state output voltage, V_o, can be derived as

$$V_o = \frac{2D}{\frac{1}{n_F} + \left(\frac{1}{n_T} - \frac{1}{n_F}\right)^* 2D} V_i \tag{1}$$

where n_F is the turns ratio of the boost choke, L, and n_T is the turns ratio of the transformer, T.

If n_F is selected to be equal to n_T, then (1) can be simplified to

$$V_o = 2Dn_F V_i. \tag{2}$$

It turns out that the dc transfer characteristics in the start-up mode are the same as that of a buck converter. The voltage stress across the inverter switches $S_1 - \mathrm{S}_4$ equals the reflected output voltage Vo plus the input voltage Vi. Ignoring the voltage drop across the switch S_c, it can be expressed as the clamping voltage V_c

$$V_c = (1+2D)V_i. \tag{3}$$

2) Boost Mode $(0.5 < D < 1)$*:* When the duty cycle exceeds 0.5, the converter automatically changes to the active-clamp boost mode. As shown in Fig. 3, the PWM pulse of S_1 and S_2 overlaps with that of S_3 and S_4, and it results in a 4-ON interval. In this interval, all four bridge switches, $S_1 - S_4$, are on, the bridge is shorted, and the choke, L, is charged, as shown in Fig. 5. The other interval is 2-OFF interval (S_1, S_2 or S_3, S_4 remain on), the current in choke L attempts to go through the primary winding of the transformer, T, and transfers the energy to the output side. Due to the existence of the leakage inductance in the transformer T, i_P cannot suddenly increase to i_L, which tends to generate a high voltage spike across the bridge. The active-clamp branch $S_c - C_c$ absorbs the energy first, and then transfers the stored energy to the output through the transformer. This is the basic operation principle of the active-clamp isolated full-bridge boost converter [2], [3]. The steady-state output voltage, V_o, is

$$V_o = \frac{1}{2-2D} n_T V_i. \tag{4}$$

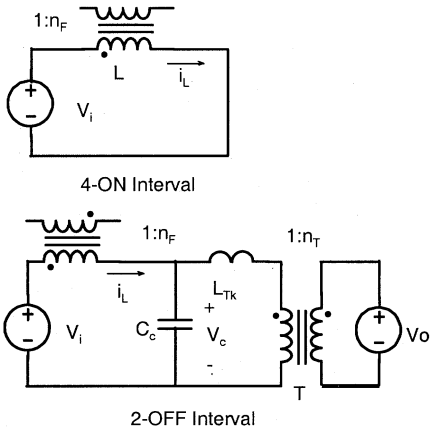

Fig. 5. Two equivalent circuits in boost mode (Scheme I).

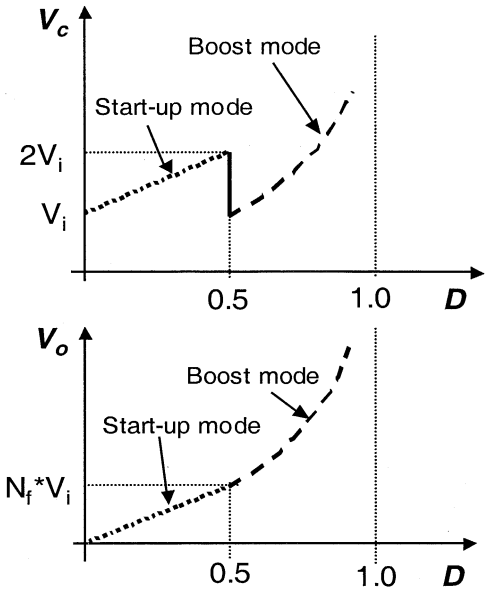

Fig. 6. V_c and V_o versus D for Scheme I.

The voltage stress across $S_1 - \mathrm{S}_4$ at boost mode equals the reflected output voltage Vo, it is

$$V_c = \frac{1}{2-2D} V_i. \tag{5}$$

The output voltage V_o and the clamping voltage V_c, as a function of duty cycle, D, for both start-up and normal boost operation modes can be illustrated as shown in Fig. 6.

B. Start-Up Scheme II

The widths of PWM signals $S_1 - S_2$ and $S_3 - S_4$ shown in Fig. 3 should be exactly identical. Otherwise the waveform of current flowing through the main transformer will be unsymmetrical which can lead to transformer saturation. According to Fig. 2, the PWM signals $S_1 - S_2$ and $S_3 - S_4$ come from two separate control chips, which need to be matched very well in practical application. This component matching is the weak point of the Scheme I.

Therefore, scheme II proposed as an improved soft-start strategy, shown in Fig. 7, needs only one PWM controller chip (UC2825) to implement both start-up and boost mode operations.

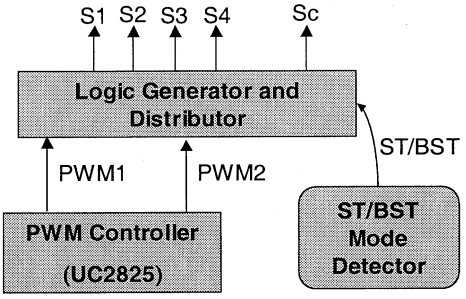

Fig. 7. Functional logic diagram (Scheme II).

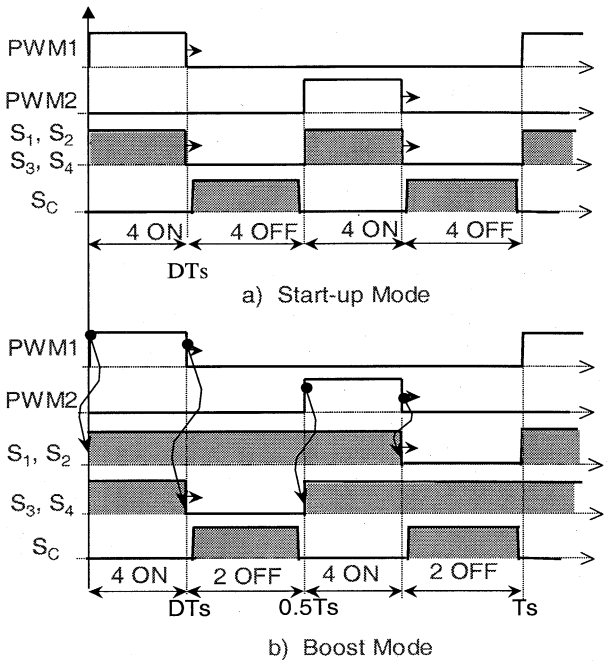

Fig. 8. Timing diagram for Scheme.

As shown in Fig. 8, the control timing in start-up scheme II is not as straightforward as scheme I. PWM1 and PWM2 are generated from UC2825. Different from Scheme I, the duty cycle of each PWM pulse varies only from 0–0.5. The transfer from the start-up mode to normal boost mode is activated by a ST/BST Mode Detector signal.

1) Start-Up Mode: In this mode, the four bridge switches $S_1 - S_4$ are turned on and off simultaneously. The circuit operates exactly as an active-clamp flyback converter. There are two main intervals: the 4-ON interval and the 4-OFF interval. Fig. 9 shows the two corresponding equivalent circuits during these intervals. Based on the flux balance in the choke, L, during one switching cycle, T_s, the steady state output voltage, V_o, is

$$V_o = \frac{2D}{1-2D} n_F V_i. \tag{6}$$

The voltage stress across switches $S_1 - S_4$ is the same as in a flyback converter, that is

$$V_c = \frac{1}{1-2D} V_i. \tag{7}$$

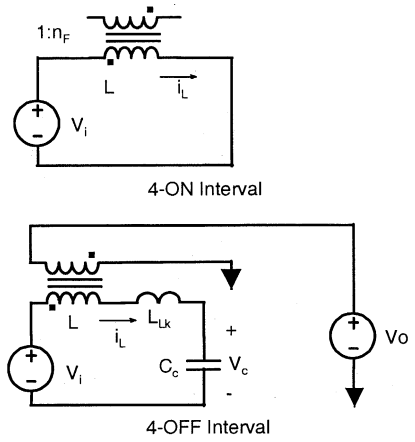

Fig. 9. Two equivalent circuits in start-up mode (Scheme II).

When the duty cycle, D, reaches 0.25^{-}, the output voltage in (6), becomes

$$V_o = n_F V_i. \tag{8}$$

2) Boost Mode: In this mode, the timing diagrams of $S_1 - S_4$, are generated from PWM1 and PWM2, as shown in Fig. 8(b). It also has a 4-ON interval and a 2-OFF interval, the same as in Scheme I. The equivalent circuits in these two intervals are the same as Fig. 5. The output voltage, V_o, is

$$V_o = \frac{1}{1-2D} n_T V_i. \tag{9}$$

The voltage stress across $S_1 - \mathrm{S}_4$ at boost mode equals the reflected output voltage Vo, it is

$$V_c = \frac{1}{1-2D} V_i. \tag{10}$$

The output voltage V_o and the clamping voltage V_c, versus D for both the start-up and the normal boost operation mode is illustrated in Fig. 10.

III. Design Considerations

A. Ratio of n_T/n_F

After the start-up mode, the converter operates in normal boost mode. The flyback winding in the choke, L, should not continue to transfer energy, and the rectifier diode, D_c, in series with the flyback winding should no longer be activated. In order to meet this requirement, the voltage generated by the isolated boost path $V_{o-\mathrm{boost}}$, must be greater than the voltage generated by isolated flyback path, $V_{o-\mathrm{flyback}}$. From this point, the ratio of n_T/n_F should be

$$\frac{n_T}{n_F} \geq 1. \tag{11}$$

B. Clamping Capacitor

The design of the clamping capacitor, C_c, is based on the $L_k - C_c$ resonant period [8]. The leakage inductance, L_k, which resonates with C_c can be either L_{lk} or L_{Tk}. The $L_k - C_c$ resonant period should be longer than one half of the high frequency

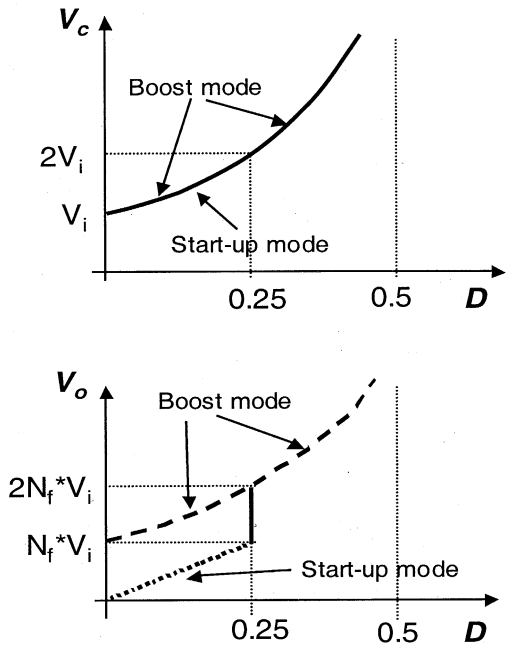

Fig. 10. V_c and V_o versus D for scheme II.

switching period, T_s. Due to the existence of two resonant tanks in different modes, C_c should be

$$Cc \geq \max\left[\frac{1}{16 L_{Tk}\pi^2 f_s^2}, \frac{1}{16 L_{Lk}\pi^2 f_s^2}\right]. \tag{12}$$

IV. Experimental Results

A 1.6 kW, 12 V/288 V active-clamp isolated full-bridge boost converter has been developed for an alternate energy application. The two proposed start-up schemes for the isolated boost converter are verified using prototype. The load of the converter is a 63 Ω resistor in parallel with a 2000 μF bus filter capacitor.

Figs. 11 and 12 show experimental waveforms of the start-up process with the two proposed start-up schemes. Three traces, i_s, V_c and V_o represent the secondary current of the transformer, T, the voltage on C_c and the output voltage respectively. The test conditions are: $n_F = n_T = 12$, $V_i = 12$ V, $V_o = 290$ V, $P_o = 1.29$ kW.

The waveforms clearly show the entire start-up process, which consists of several intervals. During the (t_0, t_1) interval, the converter operates in start-up mode, and the duty cycle, D, is in open-loop control and increases linearly. During the (t_1, t_2) interval, the converter is still in open-loop control, but it has been switched to the boost mode. During the interval (t_2, t_3) interval, the inner current loop de-saturates and then regulates the inductor current as a current source. After t_3, the outer voltage loop de-saturates and then regulates output voltage to the setting value.

In Fig. 11, t_1 is the instant when duty-cycles of the PWM pulses S1-S2 and S3-S4 shown in Fig. 3, reach 0.5. At this time the converter changes to normal boost mode from start-up mode. A very high current spike is observed in transformer current, i_s, at this instant. It is because of charge balancing of the clamping capacitor C_c. Referring to Fig. 3(a), in start-up mode,

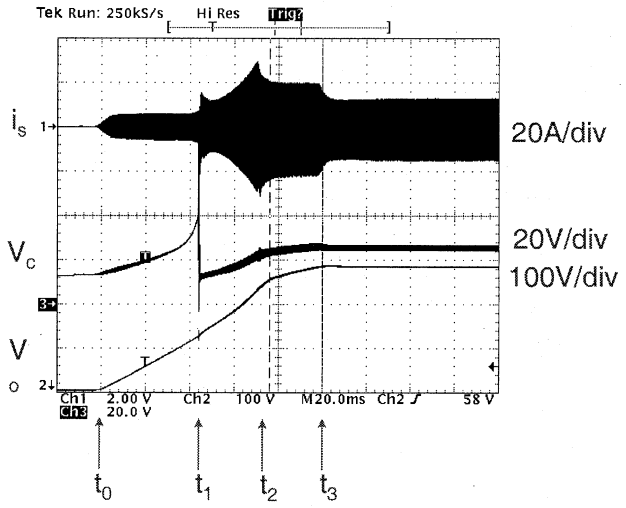

Fig. 11. Start-up waveforms of Scheme I (1.29 kW).

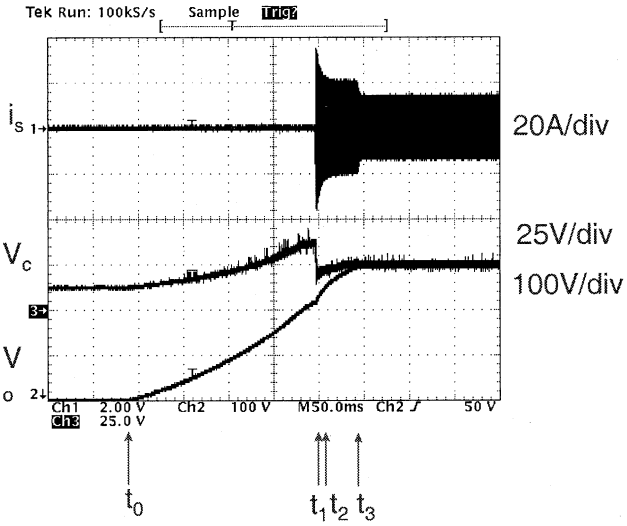

Fig. 12. Start-up waveform of Scheme II (1.29 kW).

while duty cycle D is close to 0.5, the clamping switch S_c duty cycle is reduced toward zero. C_c is charged up. After D passes 0.5 point, ($t = t_1$ instant), the converter automatically changes from start-up mode to boost mode, referring to Fig. 3(b). S_c duty cycle all of a sudden extend to near one. The quick removal of charge in C_c cause the high current spike, as shown in Fig. 11.

In Fig. 12, t_1 occurs when the ST/BST Mode Detector signal shown in Fig. 7 is activated. This switching point is normally set when duty-cycles of the PWM pulses, PWM1 and PWM2, shown in Fig. 8, reach 0.25. In scheme II, only the flyback winding transfers energy to the output side during the (t_0, t_1) interval. That is the reason why Scheme II needs a longer start-up time than Scheme I. Under this scheme, the S_c duty cycle doesn't change dramatically at $t = t_1$, therefore the high peak current at t_1 instant is prevented.

At light load, the current waveform envelope before t_3 in Fig. 11 and Fig. 12 doesn't change too much, because the pre-charging current to the output capacitor dominates the major load during the start-up mode. After time instant t_3, the converter operates at normal boost mode. The current envelope will reduce as load goes lighter.

V. Conclusion

Two start-up schemes for the active-clamp isolated full-bridge boost converter were proposed in this paper. These two schemes use the same auxiliary circuit to charge the output capacitor but employ different timing control methods. They are both successful in suppressing the in-rush current that is normally found in the boost mode start-up operation. Scheme I needs to very closely match two controller chips, for transformer voltage-second balance. Such a matching could be a problem in mass production. Scheme II avoids the controller matching and the sharp current spike during mode transition and is preferred in practical applications. However, both schemes can achieve smooth output voltage transition from start-up mode to normal boost mode operation, and are suitable for high-power isolated boost converters.

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Dr. Lai received several distinctive awards including a Technical Achievement Award in Lockheed Martin Award Night, two IEEE IAS Conference Paper Awards from Industrial Power Converter Committee, one IEEE IECON Best Paper Award, and an Advanced Technology Award from Inventors Clubs of America. He is a member of Phi Kappa Phi and Eta Kappa Nu, the Chairman of the IEEE Power Electronics Society Standards Committee, and he chaired the Technical Committee for the 2001 DOE Future Energy Challenge.