New Techniques for High-Frequency RMS-to-DC Conversion Based on a Multifunctional V-to-I Convertor

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Abstract — **Two new bipolar rms–dc convertor circuits of the computing type are presented, in which no rectifier function is required. Improved frequency response is thus obtained. RMS-to-dc computation is carried out in the current domain. To make the circuit suitable for voltage driving, a dedicated V-to-I convertor is developed. Measured 1-percent bandwidths of the rms-to-dc convertors are 35 and 22 MHz, respectively. Conversion error is less than 1 percent for crest factors up to 5.**

I. Introduction

FOR A long period of time true rms measurement was carried out in the thermal domain. This method offers a wide bandwidth and good accuracy. However, the rather complex packaging does not lead to a low-cost solution. In the second place the sampling method may be mentioned, which is capable of simultaneously providing extra signal information. Although very suitable for lower frequencies, the relatively small bandwidth of the sampling-based technique often constitutes a severe drawback.

Since the availability of bipolar integrated circuit technology, accurate computation has been a challenge. Application of the translinear principle [1], [2] often leads to elegant solutions in circuitry. Due to low-impedance levels and inherently small voltage swing, these current-mode circuits are very suitable for wide-band applications.

A well-known rms–dc convertor [3], briefly discussed in Section II, is based on this principle but is not able to exploit this wide-band property fully. Bandwidth limitations are imposed by the rectifier itself, while at very low input voltages the translinear core is driven at a very low level of transistor currents, which causes a limitation in useful frequency range. An rms–dc convertor of the computing type, that does not need a rectifier function, was proposed in 1984 [4]. In a cross-quad input stage, voltage-to-current conversion and squaring are simultaneously obtained. The advantage of very efficient transistor exploitation is, however, overshadowed by the fact that at a frequency of f_β the input impedance becomes inductive, which, in combination with parasitic capacitance, results in a peaking all-over transfer curve.

The new rms–dc circuits [5] proposed, discussed in Section III, operate according to the computing principle and do not require a rectifier function. Two versions are devised in which a dc bias current takes over the role of the rectifier and the high-frequency problem is overcome by separately optimizing the $V-I$ conversion and the squaring function. The $V-I$ conversion (Section IV) is linearized by inserting a negative resistance [6]. Moreover, base current influence is cancelled. In the squaring part current mismatch influence is reduced by using balanced circuitry. Experimental results for the two proposed circuits are compared in Section V.

II. A Well-Known RMS–DC Convertor Configuration

In Fig. 1 an rms–dc convertor is presented in such a way that it can easily be compared with the newly proposed ones. The input current I_x flows through diode-connected transistors Q_1 and Q_3, which, in combination with Q_2 and Q_4, constitute a so-called translinear loop. In this loop the translinear squaring operation takes place in Q_1 and Q_3. The output current I_z is the final result of the rms computation and is forced through Q_2. Because of the large capacitance C we may consider I_z to be a dc current. The copying function is provided by the mirror circuit. The feedback loop forces I_z to be equal to the mean value of I_y as a consequence of the fact that the mean value of the capacitor current is zero.

Translinear operation can be explained as follows. For the loop $Q_3-Q_1-Q_2-Q_4$ Kirchhoff's voltage law yields

$$V_{BE_3}+V_{BE_1}=V_{BE_2}+V_{BE_4}. \tag{1}$$

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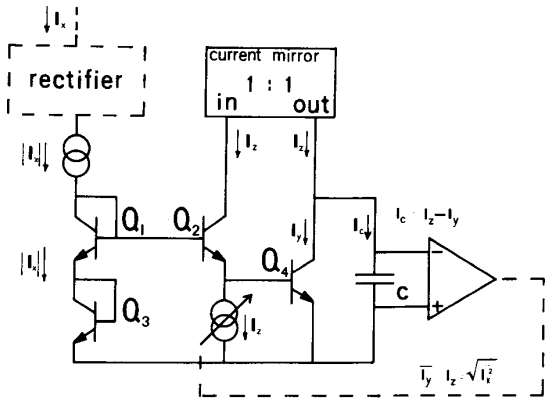


Fig. 1. Structure of well-known rms–dc convertor [3].

For all V_{BE}'s above, some 200-mV exponential relationship between the base–emitter voltage V_{BE} and the collector current I_C can be assumed. Thus (1) may be replaced by

$$\frac{kT_3}{q}\ln\frac{I_{C_3}}{I_{s_3}}+\frac{kT_1}{q}\ln\frac{I_{C_1}}{I_{s_1}}=\frac{kT_2}{q}\ln\frac{I_{C_2}}{I_{s_2}}+\frac{kT_4}{q}\ln\frac{I_{C_4}}{I_{s_4}}. \quad (2)$$

Assuming all transistors to operate at the same temperature T and having equal saturation currents I_s, (2) can be rearranged as

$$I_{C_3}\cdot I_{C_1}=I_{C_2}\cdot I_{C_4}. \quad (3)$$

This operation is more generally known as the translinear principle [1]. In Fig. 1, $I_{C_3}=I_{C_1}=I_x$, $I_{C_2}=I_z$, and $I_{C_4}=I_y$, so (3) leads to

$$I_x^2=I_z\cdot I_y. \quad (4)$$

Hence, averaging left and right and substituting $\overline{I_y}=I_z$ leads to

$$\overline{I_x^2}=I_z\cdot\overline{I_y}=I_z^2 \quad (5)$$

or

$$I_z=\sqrt{\overline{I_x^2}}\,. \quad (6)$$

This circuit can handle only the positive polarity of I_x. So if alternating currents have to be dealt with, a rectifier function is required before entering the computing section. The rectifier function constitutes a drawback by limiting the useful frequency range, as mentioned before. A second drawback lies in the parallel capacitor C_p of the diodes Q_1 and Q_3 for input currents close to zero. This capacitance needs a charging current

$$i_C=C_p\cdot dV/dt=C_p\cdot\frac{kT}{q(I_x+I_{ds})}\cdot\frac{dI_x}{dt} \quad (7)$$

where I_{ds} symbolizes the reverse saturation current of the diodes. For input currents close to zero the capacitive current is no longer negligible; for large values of dI_x/dt the same objection holds. Since the current i_C has to be supplied by I_x, the waveform of the diode voltages will be distorted and a nonlinearity is introduced.

III. Improved RMS–DC Conversion Techniques

The newly proposed rms-computing circuits essentially eliminate both these drawbacks by superimposing the ac-input currents onto a dc-bias current, symbolized by I_o.

A. An RMS–DC Convertor, Version I

In Fig. 2 the principle diagram of the new rms–dc convertor, version I, is shown. It is structured in the same manner as that of Fig. 1. As before, the core Q_1–Q_4 is assumed to comprise identical transistors, all of them operating at the same temperature. A current I_o+I_x is forced through Q_1 and a current I_o-I_x through Q_3 is forced by the current source $2\cdot I_o$. Applying the translinear principle again, the term $I_o^2-I_x^2$ will appear [7], in which the polarity of I_x has become unimportant as long as the absolute value of I_x does not exceed I_o. In order to get rid of the term I_o^2, the currents I_z and I_y are also biased with I_o. For the loop Q_1–Q_4 translinear operation results in the expression

$$(I_o-I_x)(I_o+I_x)=(I_o+I_z)(I_o-I_y). \quad (8)$$

In (8) I_y appears with a negative sign, so the necessary condition $\overline{I_y}=I_z$ has to be imposed by forcing the mean value of the sum of the currents through Q_2 and Q_4 to be equal to $2I_o$.

Elaboration of (8) yields

$$I_o^2-I_x^2=I_o^2+I_o(I_z-I_y)-I_z\cdot I_y. \quad (9)$$

Cancelling common terms leads to

$$I_x^2=-I_o(I_z-I_y)+I_z\cdot I_y. \quad (10)$$

I_o and I_z both being dc currents, substitution of $\overline{I_y}=I_z$ results in

$$\overline{I_x^2}=I_z^2$$

or

$$I_z=\sqrt{\overline{I_x^2}}\,. \quad (11)$$

Until now the operation has been carried out in the current domain. A dedicated *V*-to-*I* convertor is added to deal with voltage driving. A more detailed description is given in Section IV. The most important feature of this *V*-to-*I* convertor here is the availability of balanced output currents I_o-I_x and I_o+I_x with I_x proportional to V_{in}.

The two squaring sections, as shown in Fig. 3, placed in parallel to fight mismatches (see Section III-A-2) can exploit the advantage of the balanced output of the *V*-to-*I* convertor.

For the realization of the transconductance function in the output stage a general-purpose operational amplifier of

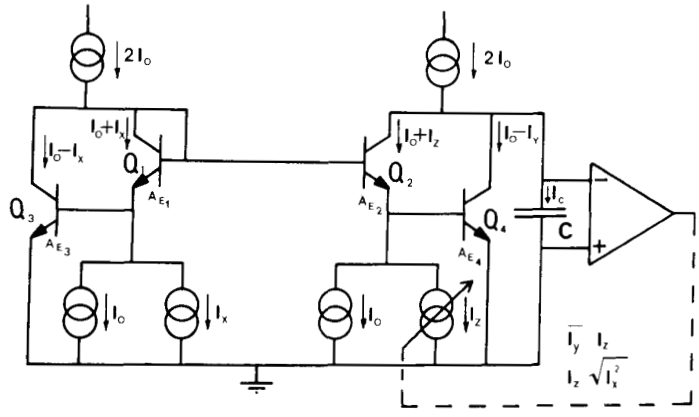


Fig. 2. Structure of the rms–dc convertor, version I.

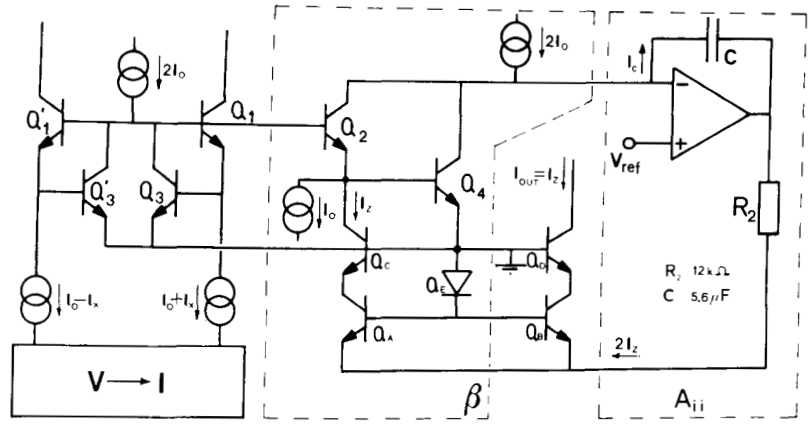


Fig. 3. Doubled squaring input section and output stage of version I.

type 741 is chosen; transconductance is performed by resistor R_2. A cascoded current mirror circuit $Q_A - Q_E$ is implemented, which acts as a current splitter. One output drives transistor Q_2 while the other places the rms result at the user's disposal.

1. Stability: At first sight in the right term of (8), I_z and I_y might have opposite signs. However, the circuit is fed back and so it is of great importance that gain and phase margins are within safe limits. In order to be able to analyze the output circuit, it is represented in the block diagram of Fig. 4, in which A_{ii} represents the transfer from I_c to $2 \cdot I_z$, performed by the active part of the output stage. β corresponds to the feedback from I_z to I_c, performed by the right half of the translinear computing core.

A_{ii} is well described as a first-order network. If β is assumed to be frequency independent, I_c is a nonlinear function of (the magnitude of) I_x. Calculation yields

$$I_c = \frac{I_x^2 - I_z^2}{I_o + I_z}. \tag{12}$$

This function is plotted in Fig. 5 for various values of parameter I_x/I_o.

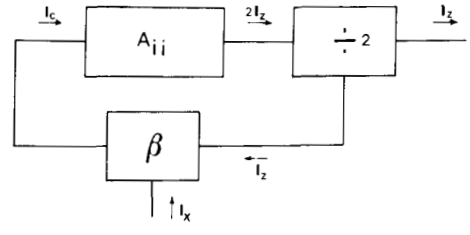


Fig. 4. Block diagram of the output section of version I.

It can be seen that in the first quadrant this function is monotonically decreasing, in contrast to the behavior in the second quadrant. Although interchanging the signal parts of the currents through Q_2 and Q_4 would mathematically lead to the same rms expression, this operation will be located in the second quadrant, and because the slope changes sign, stability cannot be guaranteed for all values of I_x. For this reason in version I transistor currents of Q_2 and Q_4 have been chosen $I_o + I_z$ and $I_o - I_y$, respectively.

2. Mismatch Influence: Generally, translinear circuits can be rather sensitive to mismatch. In Fig. 2 two types of bias current mismatch can occur (upper-lower and upper-upper), combined with emitter-area mismatches.

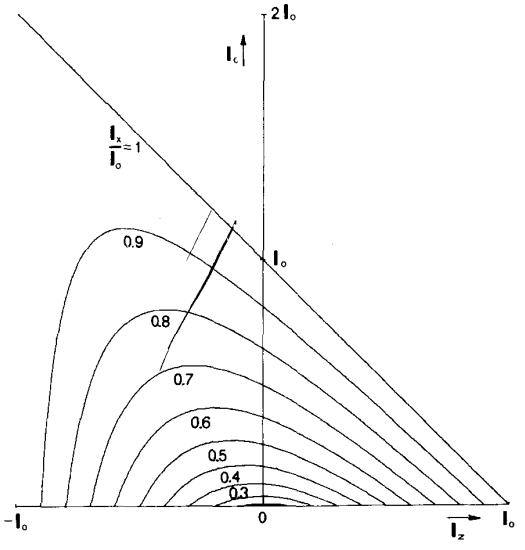


Fig. 5. Transfer curve of β ($I_c = (I_x^2 - I_z^2)/(I_o + I_z)$).

Mismatch of upper and lower bias current sources for Q_1 and Q_3 results in an offset in I_x, while a similar mismatch in the bias sources for Q_2 and Q_4 causes an offset in I_z. Furthermore, mutual mismatch of the upper bias current sources works out in the same way as emitter-area mismatch.

Assuming a certain emitter-area mismatch and neglecting base current and Early influence, examination of the core of the computing circuit leads to

$$I_z = \sqrt{\lambda \overline{I_x^2} + (1-\lambda) I_o^2} \tag{13}$$

with

$$\lambda = (A_{E_2} \cdot A_{E_4})/(A_{E_1} \cdot A_{E_3}); \qquad \lambda \text{ nominally equals } 1.$$

Summarizing, mismatch results in offset and nonlinearity. The latter can degenerate to hysteresis for small values of I_z if λ exceeds 1.

Doubling of the input section (Q_1–Q_1', Q_3–Q_3' in Fig. 3) creates a gain cell structure, which inherently eliminates the offset in I_x. (It can be proven that emitter-area mismatch in the doubled section only leads to a second-order nonlinearity). It is possible to solve the main nonlinearity problem by trimming one of the bias current sources once (an automatic periodical trimming system was devised in order to carry out the required measurements (see Section V)).

B. A Second Technique Not Requiring Trimming, Version II

The principle diagram of the second version is presented in Fig. 6. The relatively high mismatch sensitivity of the circuit discussed above constitutes a severe drawback. So a second version was devised in which the input current is scaled by the output current before being applied to the computing section. The scaling is carried out outside the core Q_1–Q_4, resulting in a current I_z that is principally free of nonlinearity caused by emitter-area mismatch. This technique is of particular significance. The squaring section itself remains unchanged. Now, if the signal part of transistor currents through Q_1 and Q_3 can be forced to equal $(I_x/I_z)\cdot I_o$ and if at the same time the current of Q_2 equals a constant fraction A of I_o, circuit operation is described by

$$\left(I_o - \left(\frac{I_x}{I_z}\right)\cdot I_o\right)\left(I_o + \left(\frac{I_x}{I_z}\right)\cdot I_o\right) = (A \cdot I_o)(I_y). \tag{14}$$

As stated before, the attenuation or division operation must have taken place before entering the squaring section and it is provided by the *V*-to-*I* convertor (see Section IV). In order to keep the currents through Q_1 and Q_3 positive, I_x/I_z must be smaller than 1. As will be shown in the next paragraph, A has a nominal value smaller than 1 and is related to both the scale factor and the maximum crest factor capability. As the mean value of the current through capacitor C is zero, $\overline{I_y}$ will equal I_o. This operation is performed by the feedback loop with I_z as the rms-information carrier. After settling, I_z can be considered as a dc current. The information carrying current $(I_x/I_z)\cdot I_o$ passes through Q_1 and Q_3. Substituting $\overline{I_y} = I_o$ into (14) leads to the desired result:

$$I_z = \frac{1}{\sqrt{1-A}} \cdot \sqrt{\overline{I_x^2}}\,. \tag{15}$$

Note that during this calculation, in contrast to version I, it was not necessary to cancel any common terms.

1. Maximum Crest Factor: The crest factor CF of any periodical signal is defined as

$$CF = \frac{\text{top value}}{\text{rms value}} = \frac{\hat{I}_x}{\sqrt{\overline{I_x^2}}} = \frac{1}{\sqrt{1-A}} \cdot \frac{\hat{I}_x}{I_z}. \tag{16}$$

The maximum value of $\hat{I}_x/I_z$ being 1, the maximum crest factor $CF_{\max}$ results in

$$CF_{\max} = \frac{1}{\sqrt{1-A}}. \tag{17}$$

It follows that (15) can be expressed as

$$I_z = CF_{\max} \cdot \sqrt{\overline{I_x^2}}\,. \tag{18}$$

The version II circuit was designed for a maximum crest factor of 5, which requires A to be 24/25.

2. Influence of Mismatches: Assuming a certain emitter-area mismatch and neglecting base current influence, a straightforward translinear analysis of the circuit of Fig. 6 yields

$$I_z = \frac{1}{\sqrt{1-\mu \cdot A}} \cdot \sqrt{\overline{I_x^2}} \tag{19}$$

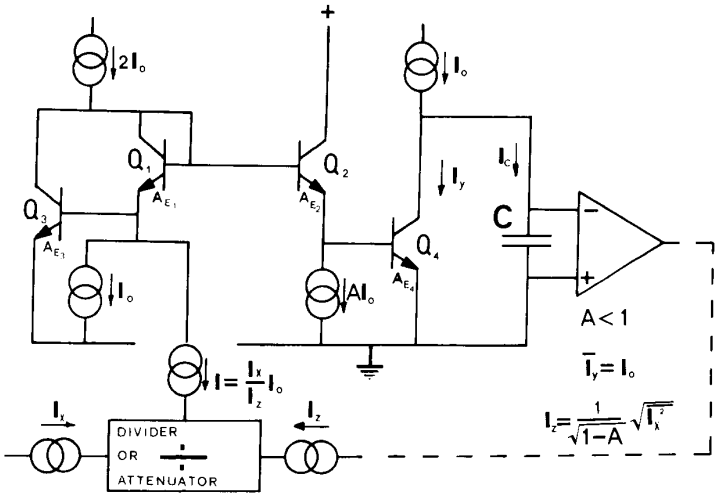


Fig. 6. Structure of the rms–dc convertor, version II.

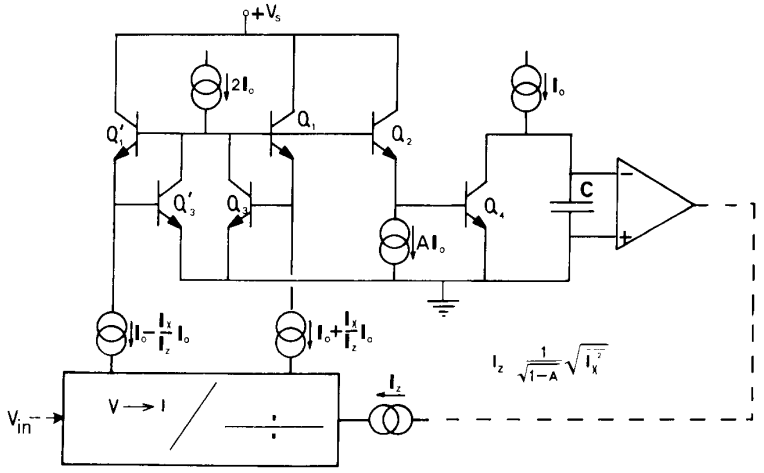


Fig. 7. Doubled squaring input section and output stage of version II.

with

$$\mu = (A_{E_1} \cdot A_{E_3})/(A_{E_2} \cdot A_{E_4}); \qquad \mu \text{ nominally equals } 1.$$

In contrast to version I, emitter-area mismatch in version II does not affect linearity. It only changes the scale factor. Mismatch in current sources of course results in a similar effect.

Due to these measures periodical trimming can be omitted. This freedom from trimming is a major advantage of version II over version I. Fig. 7 shows the circuit of version II with a doubled input section.

IV. A Dedicated V-to-I Convertor

As was mentioned before, a special $V-I$ convertor is developed to drive the rms-computing section. This convertor will turn out to be an attractive interfacing building block for analog signal processing [6]. The principle circuit is shown in Fig. 8.

The gain cell, constituted by transistors $Q_{11}-Q_{14}$, places copies of the input current at the user's disposal. Because of the fact that the emitter of Q_{12} is grounded, the input node P is virtually grounded. The input voltage source V_{in}, which is assumed to have zero output impedance, is to first order converted to an input current by resistor R_c:

$$I_{in} = V_{in}/R_c. \tag{20}$$

The nonlinear properties of the diode-connected transistors Q_{11} and Q_{12}, however, prevent exact linear V-to-I conversion. Linear conversion can be obtained by the insertion of a negative resistance of magnitude $-R_c$ (dotted in Fig. 8) between emitter Q_{11} and ground. As is illustrated in Fig. 9, this combination acts as an ideal current source.

The required negative resistance is provided by the circuit of Fig. 10, which was earlier reported on in [10]. Measured at the collectors of Q_{15} and Q_{16}, the negative resistance includes the emitter input resistances of Q_{15} and

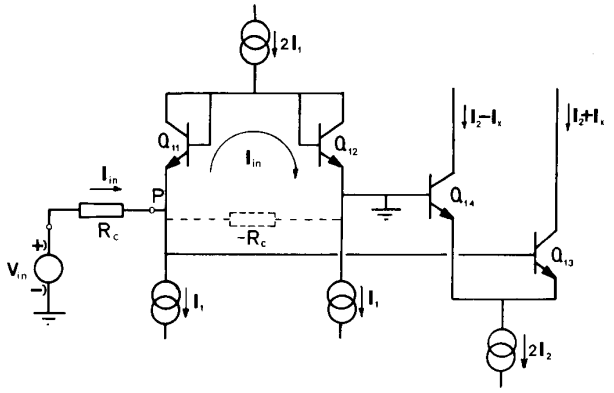


Fig. 8. Principle diagram $V-I$ convertor.

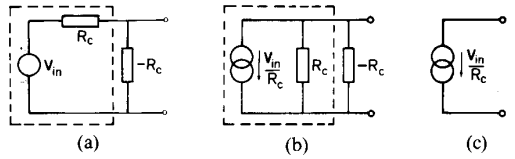


Fig. 9. (a) Insertion of negative resistance. (b) Norton equivalent of (a). (c) Overall equivalent of input circuit.

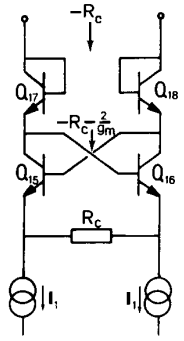


Fig. 10. Negative resistance circuit.

Q_{16}. Diode-connected transistors Q_{17} and Q_{18} were added to compensate for this effect, so the impedance at the collectors of Q_{17} and Q_{18} now exactly equals $-R_c$. Thus perfectly linear conversion is obtained.

The V-to-I convertor has to yield output currents of which the signal part (I_x) should be an exact copy of the input signal part (V_{in}/R_c). The translinear relation for $Q_{11}-Q_{14}$ in Fig. 8 (at first neglecting base currents) reads

$$(I_1 - I_{in})(I_2 + I_x) = (I_1 + I_{in})(I_2 - I_x) \qquad (21)$$

which leads to the wanted relation

$$I_x = (I_2/I_1)\cdot I_{in}. \qquad (22)$$

Now if base currents are taken into account, both dc (carrier) currents in the inner branch (Q_{11}, Q_{12}) and dc (carrier) currents in the outer branch (Q_{13}, Q_{14}) will mutually differ, as is illustrated in Fig. 11(a). Note that the combination of input voltage source, conversion resistor

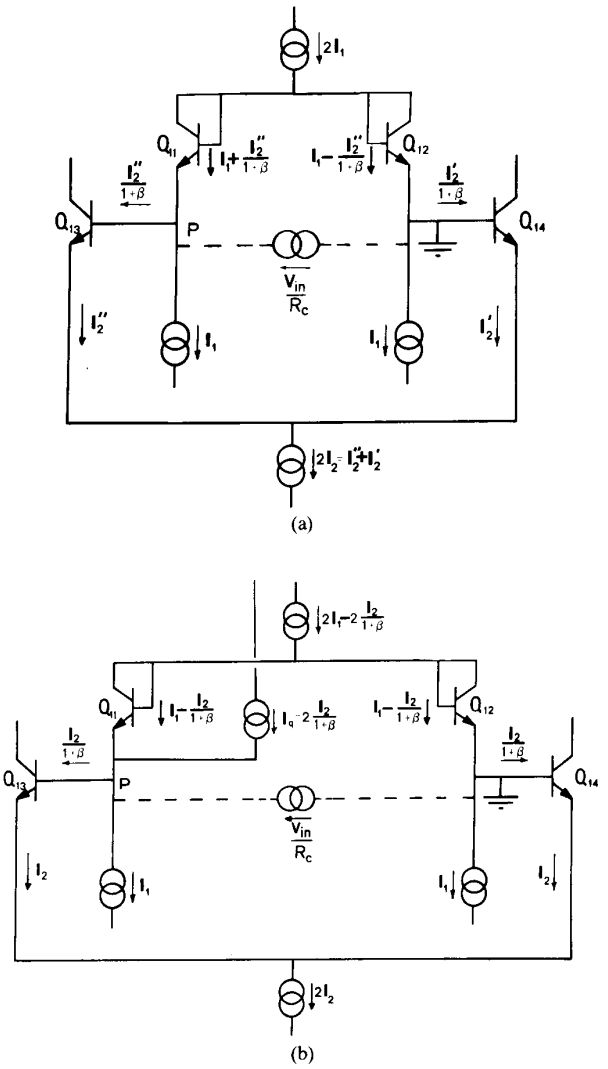


Fig. 11. (a) Base current influence in $V-I$ convertor. (b) Cancelling base current influence by adding a current source I_q.

R_c, and the negative resistance $-R_c$ does not affect the dc conditions.

If, for simplicity, equal β for all transistors and unaffected signal (modulation) currents of opposite polarity are assumed, the translinear relation for the loop $Q_{11}-Q_{14}$ may be written as

$$\{\beta/(\beta+1)\}^2(I_1 + \Delta I_1 - I_{in})(I_2 - \Delta I_2 + I_x) = \{\beta/(\beta+1)\}^2(I_1 - \Delta I_1 + I_{in})(I_2 + \Delta I_2 - I_x) \qquad (23)$$

with

$$\Delta I_1 = (I_{EQ_{11}} - I_{EQ_{12}})/2$$

and

$$\Delta I_2 = (I_{EQ_{14}} - I_{EQ_{13}})/2. \qquad (24)$$

Elaboration of (23) shows that difference currents ΔI_1 and

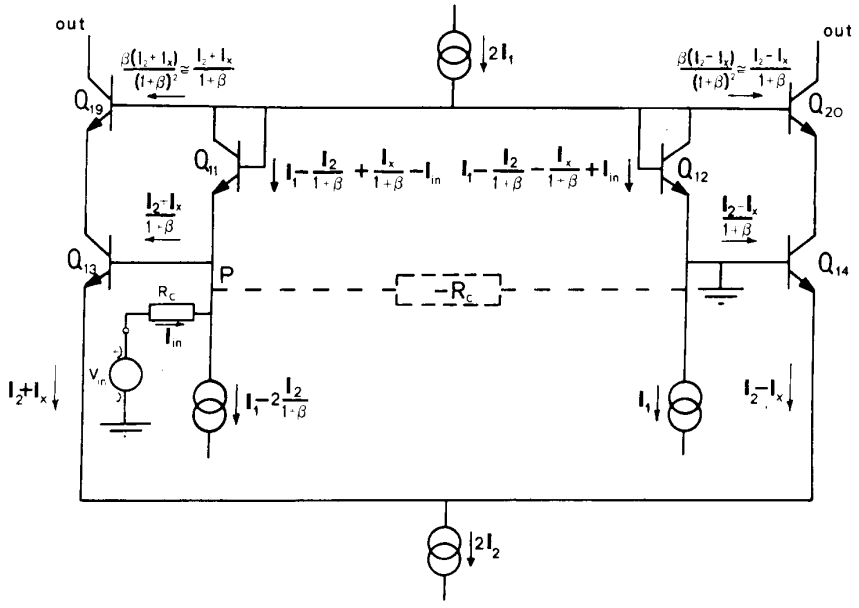


Fig. 12. Cascading $V-I$ output stage with base current compensation.

ΔI_2 will be transferred as if they are signal currents, thus causing unwanted offsets in both input and output, which can even lead to distortion. Further calculation yields that only if both

$$\Delta I_1 = 0$$

and

$$\Delta I_2 = 0 \tag{25}$$

does relation (23) lead, except for a factor $\beta/(\beta+1)$, correctly to (22). So it has to be seen to that mutual symmetry of dc currents through Q_{11} and Q_{12}, respectively, through Q_{13} and Q_{14} is guaranteed.

A. Base Current Compensation

The difference between collector currents of Q_{11} and Q_{12}, caused by the base current of Q_{13}, can easily be cancelled by adapting the bias source at node P by means of an extra dc source I_q as indicated in Fig. 11(b). If I_q equals $2\cdot I_2/(\beta+1)$ and the upper current source of the input branch is modified to $2\cdot I_1 - 2\cdot I_2/(\beta+1)$, equal dc currents through Q_{11} and Q_{12} as well as equal dc currents through Q_{13} and Q_{14} are obtained (Fig. 11(b)). Note that now the signal-to-bias relation is the same as in the ideal case and condition (22) is met again [9]. The source I_q can simply be derived from the base current of a transistor biased at $2\cdot I_2$.

An elegant way to subtract a current $2\cdot I_2/(\beta+1)$ from the source $2\cdot I_1$ is obtained by adding the cascode transistors Q_{19} and Q_{20}, as is shown in Fig. 12. Moreover, a substantial improvement of output impedance of the convertor is obtained.

This base current compensation technique is valid as long as ac-β and dc-β are nominally equal, which condition is roughly satisfied for frequencies below f_β. For maximum bandwidth and minimum influence of emitter series resistances, currents I_1 and I_2 are chosen equal with a nominal magnitude of I_o. The influence of emitter-area mismatch can generally be adequately cancelled by a PTAT-voltage source [10], inserted in the translinear loop. In the case in question the emitter-area mismatch may be efficiently reduced by (nonsynchronously) interchanging input and ground node during operation.

B. Current Division by Means of a $V-I$ Convertor

Inspection of the signal part of the output current (Fig. 12), given as:

$$I_{out} = I_x = (I_2/I_1)\cdot I_{in}$$

with

$$I_{in} = V_{in}/R_c \tag{26}$$

leads to the conclusion that multiplication may be obtained by means of I_2 while division or attenuation may be obtained by means of I_1. In the version II rms–dc convertor (Fig. 7) the $V-I$ convertor must include a dividing function because the input current must be scaled by the output current I_z as becomes clear from (14). Therefore special attention is given to the dividing function.

This operation is more difficult to obtain than the multiplication function because of the fact that all three input circuit bias currents (I_1 in Fig. 8) have to be controlled accurately and simultaneously in a ratio 2:1:1. Moreover this ratio has to cover a wide dynamic range. For this goal a special control circuit is devised. In Fig. 13 the principle circuit is presented in which the required ratio is determined by an accurate n-p-n mirror. Optimum

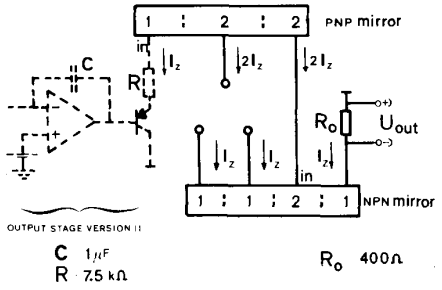


Fig. 13. Schematic setup of accurate 2:1:1 output current mirroring.

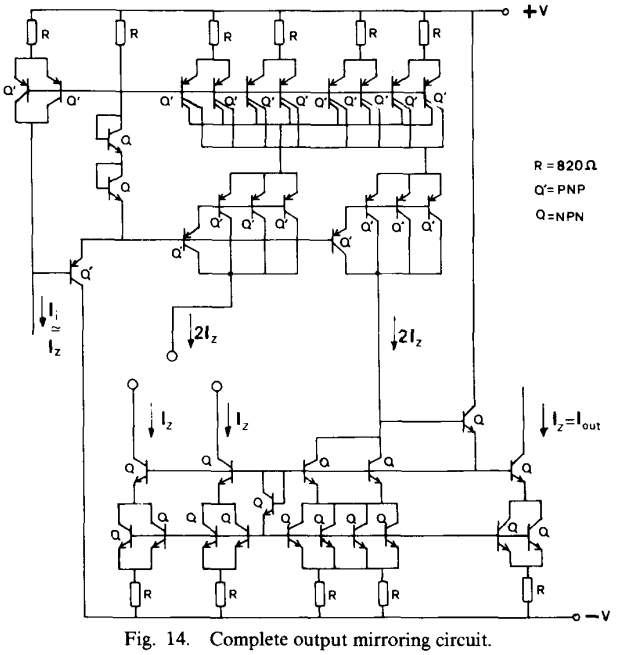


Fig. 14. Complete output mirroring circuit.

tracking performance of both n-p-n and p-n-p mirrors is achieved by applying cascoding transistors, emitter degeneration, base current compensation, and common centroid layout techniques.

Fig. 14 presents the complete current controlling circuit. Measured tracking accuracy was better than 0.1 percent for $I_z = 10$ μA up to $I_z = 1$ mA.

C. Experimental Results of the V–I Convertor

The circuit of Fig. 12 was tested for HF performance at $I_1 = I_2 = 150$ μA and $R_c = 1$ kΩ. The output currents were passed through 50-Ω resistors and the resulting differential voltage was measured. The −3-dB small-signal bandwidth was 85 MHz and the −1-percent bandwidth, of more significance for precision applications, was measured as 25 MHz. The low-frequency linearity was observed as being better than 0.5 percent for signal amplitudes up to 90 percent of full scale.

Fig. 15 presents the transfer curve photographically, measured with and without error correction resistor (f = 1 kHz).

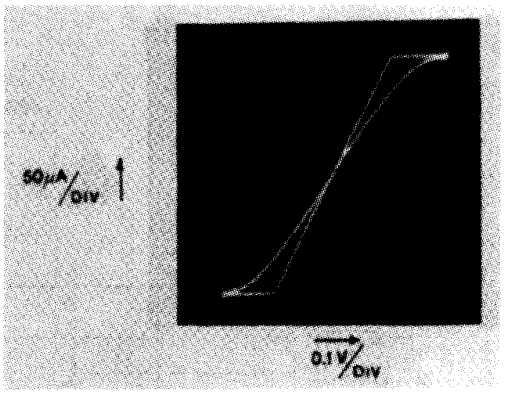


Fig. 15. Transfer curve of *V*–*I* convertor with and without negative resistance $R_C = 1$ kΩ; $f = 1$ kHz.

V. Experimental Results of Both Types of RMS–DC Convertors

A. Experimental Results of Version I

Fig. 16 presents the complete version I rms–dc convertor, which was constructed with transistor arrays, fabricated in a standard bipolar process ($f_T = 300$ MHz). The bias current I_o was 0.5 mA and ±9-V supply voltages were applied. Conversion resistor R_c was chosen as 2 kΩ. An extra (Darlington) transistor Q_H was placed in the squaring part in order to minimize the influence of the loading effect of the base current of Q_2. To prevent parasitic oscillation a small capacitor could be placed in parallel with the base–emitter junction of Q_H. The theoretical behavior of the output current I_z as a function of $V_{\text{in,peak}}$ and the crest factor is presented in Fig. 17(a) and (b), respectively.

The upper measuring level (Fig. 17(b)) is determined by the maximum input voltage ($I_o \cdot R_c$). The lower measuring level is limited by the matching inaccuracy of the current sources $2 \cdot I_o$ and I_o in the output stage which amounts to 2 percent; this mismatch will result in an offset of I_z as was mentioned before. For this reason the linearity error is determined by comparing the measured curve with a straight line through the 20- and 80-percent full-scale values. Fig. 18(a)–(e) shows the measured linearity error as a function of a dc input, a 100-Hz sine-wave input, and a pulse-shaped input (period time 10 ms) with duty cycles of 25, 10, and 4 percent (crest factors of 2, 3.16, and 5, respectively). The deviation is normalized on the full-scale value, which depends on the actual crest factor.

The peak value of the linearity error, measured between 10 and 100 percent of the input scale, is approximately 1 percent for input signals with a crest factor up to 5, as is listed in Table 1.

Fig. 19 shows the measured frequency response for sine waves with amplitudes of 20, 50, and 90 percent of full scale (FS). The 20- and 50-percent FS curves show a slight peaking at $f = 40$ MHz and have 1-percent bandwidth of about 25 MHz. The 1-percent bandwidth of the 90-percent

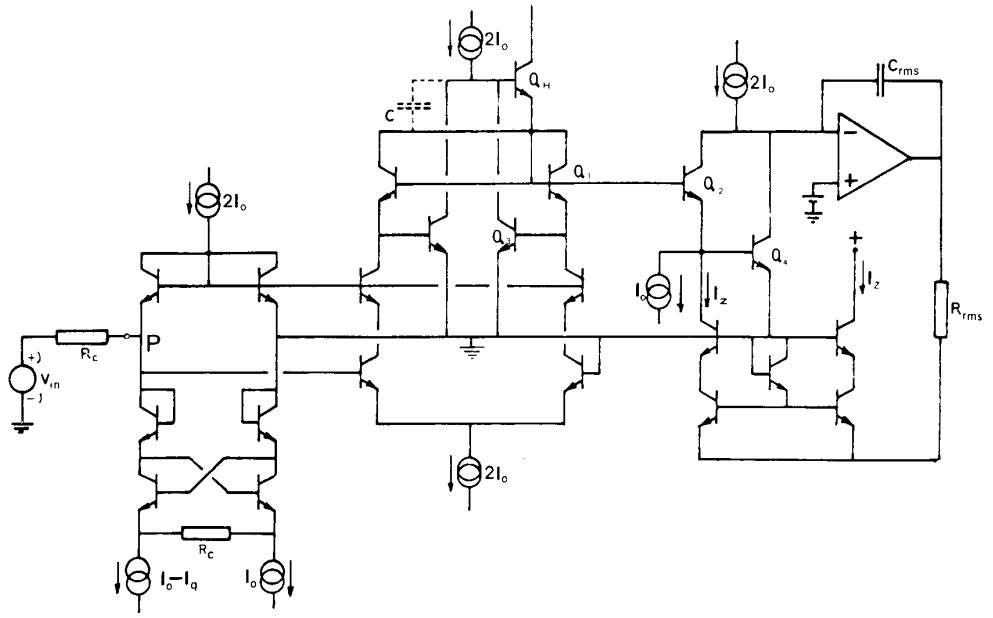
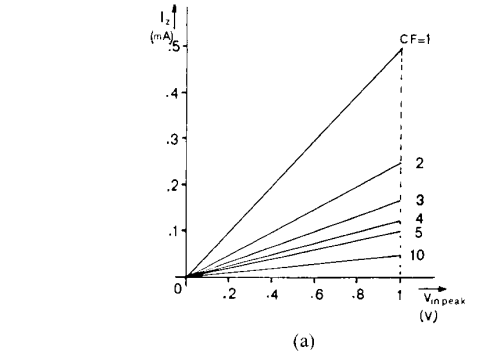
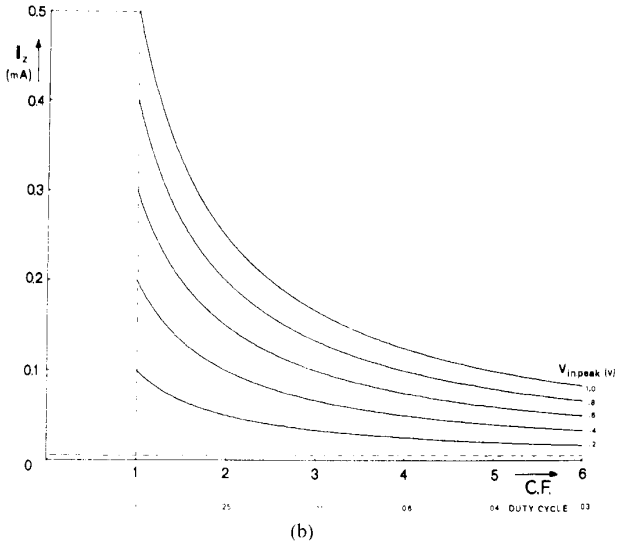


Fig. 16. Complete circuit of version I. $R_C = 2$ kΩ; $R_{rms} = 12$ kΩ; $C_{rms} = 5.6$ μF; $I_o = 0.5$ mA; $V_{supply} = \pm 9$ V.



(a)



(b)

Fig. 17. (a) Theoretical overall transfer curves of version I; I_z versus $V_{in,peak}$. (b) Theoretical overall transfer curves of version I; I_z versus crest factor.

FS curve was cursorily observed to be 35 MHz. All transfer curves show a −10-percent bandwidth of more than 50 MHz.

B. Experimental Results of Version II

In Fig. 20 the complete version II rms–dc convertor is shown, in which for simplicity the current driving circuit of Fig. 14 is represented in a symbolic way. This circuit was completely integrated on our analog cell-based transistor array (ACBA) [11], which is fabricated in a standard 18-V 500-MHz process. The bias current I_o amounts to 0.25 mA and supply voltages were ±6 V. In the squaring section transistors Q_{ABC} are added to make the nominal collector–base voltages of Q_1, Q_1', Q_3, Q_3', and Q_2 all equal to just one V_{BE}.

Fig. 21(a) and (b) depicts the theoretical behavior of the output current I_z as a function of $V_{in,peak}$ and of the crest factor.

In contrast to version I the upper measuring value is now determined by the maximum available value of I_z. The circuit is designed in such a way that at 50 percent of full scale $I_z = I_o$; at this point the error in the $V-I$ convertor, caused by emitter series resistances, is minimal. The maximum input voltage the circuit can handle is given by

$$V_{in,max} = 2 \cdot I_o \cdot R_c \cdot (CF/CF_{max}) \qquad (27)$$

with $I_o = 0.25$ mA, $R_c = 2$ kΩ, and $CF_{max} = 5$ ($A = 24/25$). For crest factors larger than 5 the equilibrium in the charge transport through Q_4 will be disturbed, resulting in a decrease of the voltage of the capacitor C_{rms} in Fig. 20 and an increase of the output voltage of the operational amplifier, required for the condition $I_z = 0$. It can be

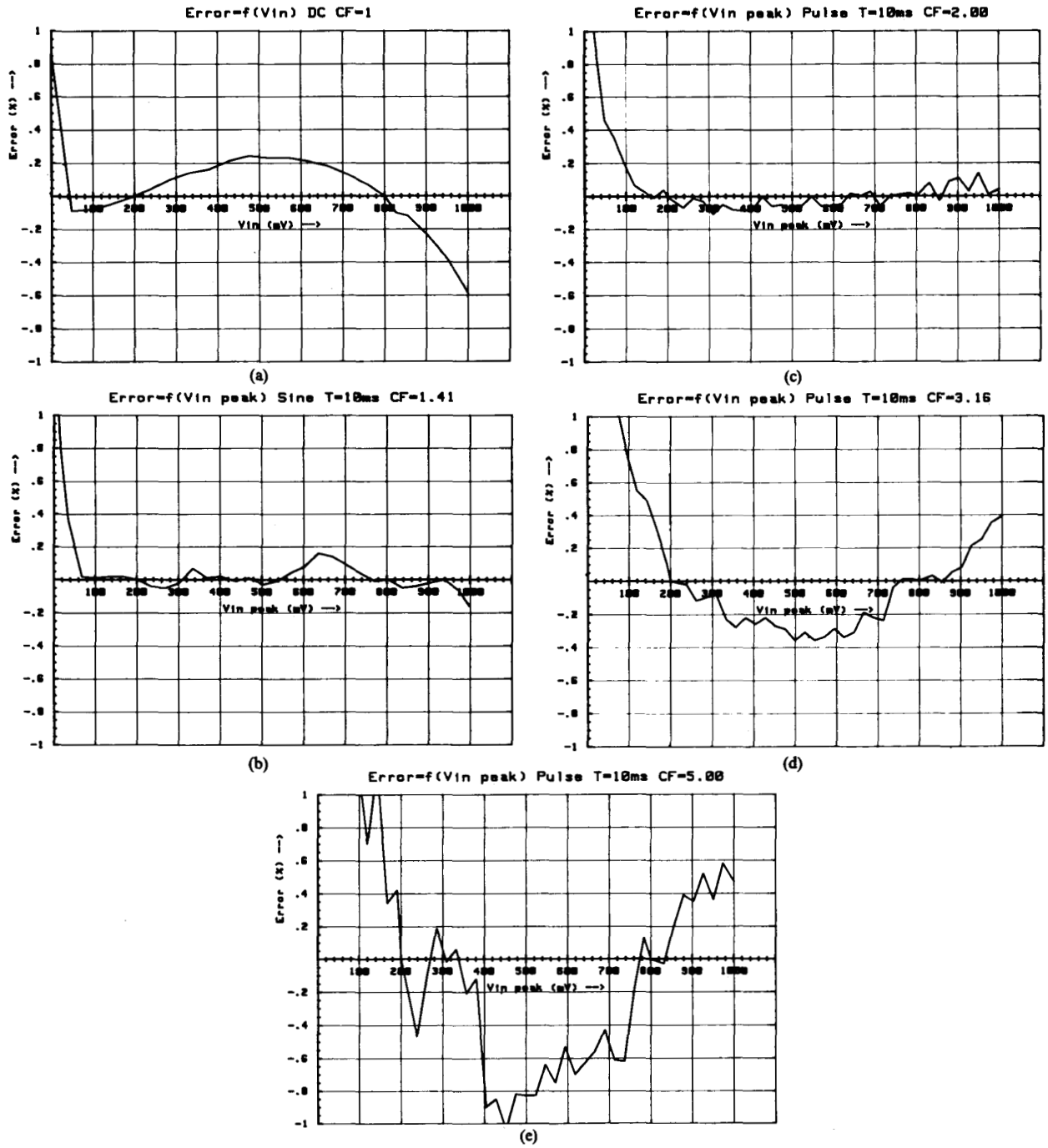


Fig. 18. (a)–(e) Measured transfer error curves of rms–dc convertor version I, as a function of crest factor.

TABLE I
MEASURED LINEARITY ERROR, VERSION I

Crest factor	Peak linearity error (% FS) $V_{in,\ peak} = 1\ V$
1	0.6%
1.4	0.2%
2	0.2%
3.2	0.7%
5	1.0%

proven that for input voltages smaller than

$$V_T \cdot \ln\{(1 + CF/CF_{max})/(1 - CF/CF_{max})\} \qquad (28)$$

beside the normally expected value of I_z, the value $I_z = 0$ also becomes a valid output signal. To prevent this hysteresis, a small input offset current (e.g., 5 μA) can be added. However, the lower part of the scale then remains unreliable, so (28) finally determines the lower useful measuring

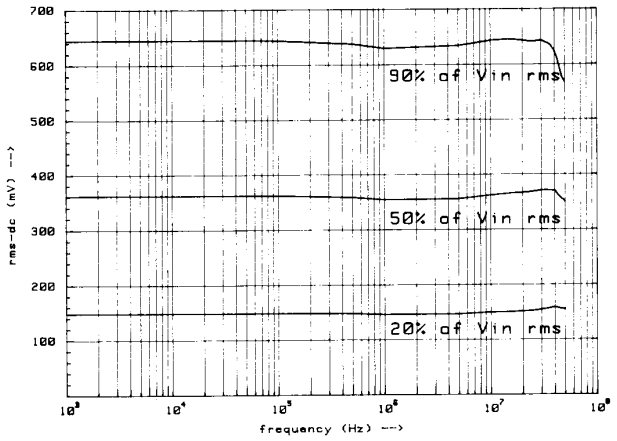


Fig. 19. Measured transfer curves of rms–dc convertor version I, as a function of frequency.

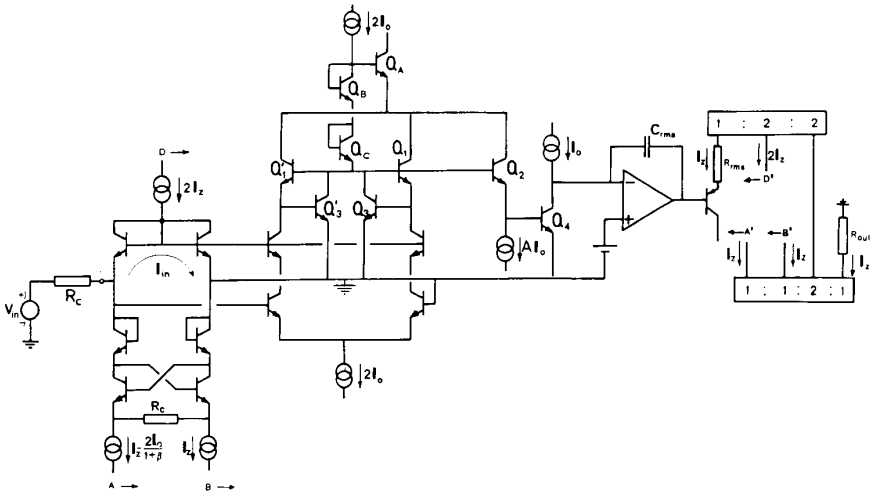


Fig. 20. Complete circuit of version II. $R_C = 2$ kΩ; $R_{out} = 400$ Ω; $R_{rms} = 7.5$ kΩ; $C_{rms} = 1$ μF; $I_o = 0.25$ mA; $V_{supply} = \pm 6$ V.

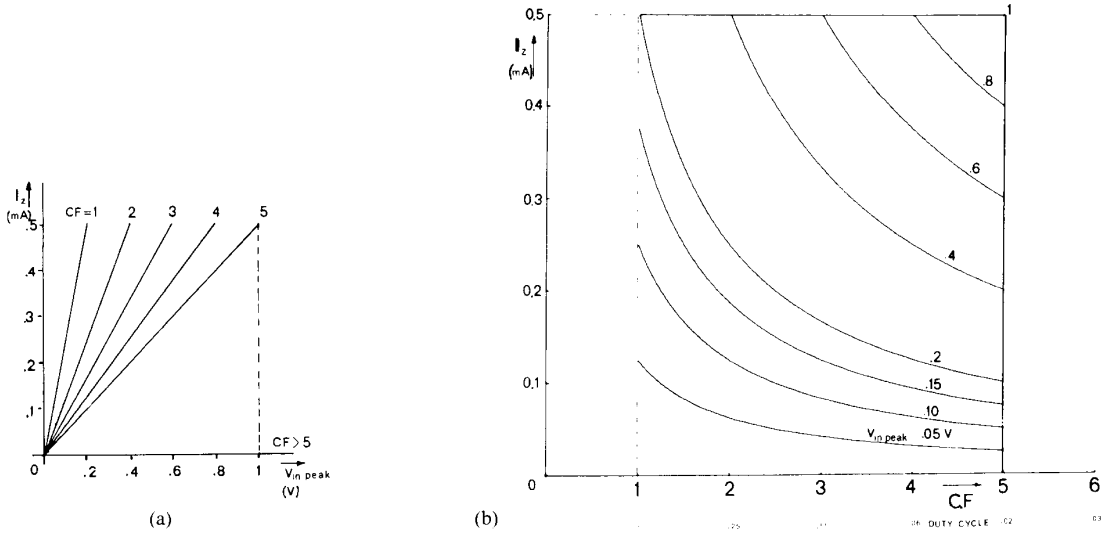


Fig. 21. (a) Theoretical overall transfer curves of version II; I_z versus $V_{in,peak}$. (b) Theoretical overall transfer curves of version II; I_z versus crest factor.

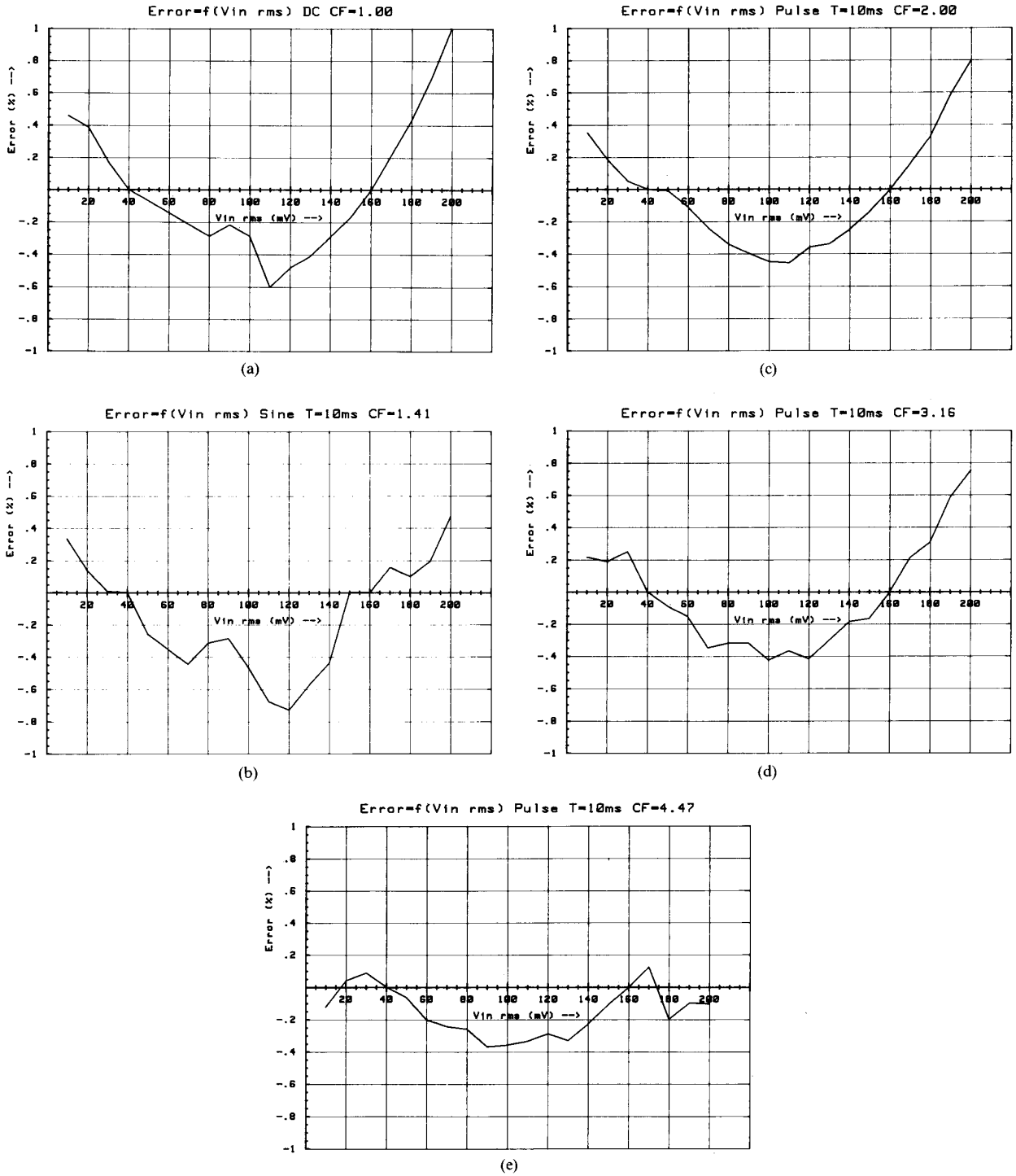


Fig. 22. (a)–(e) Measured transfer error curves of rms–dc convertor version II, as a function of crest factor.

level of the circuit. In Fig. 22(a)–(e) the measured linearity error is shown for various input-signal *CF* values and as a function of the rms-input-signal value. Note that the maximum input voltage is related to the crest factor of the input signal in conformity with (27). For this reason the linearity error is measured at a maximum input voltage equal to $(CF)\cdot 200$ mV. Table II depicts the measured peak value of the linearity error.

The frequency response (Fig. 23) is measured for sine-shaped input signals with an amplitude of 20-, 50-, and 90-percent full scale. In contrast to version I, transfer curves now show a rather strong dependency on the ampli-

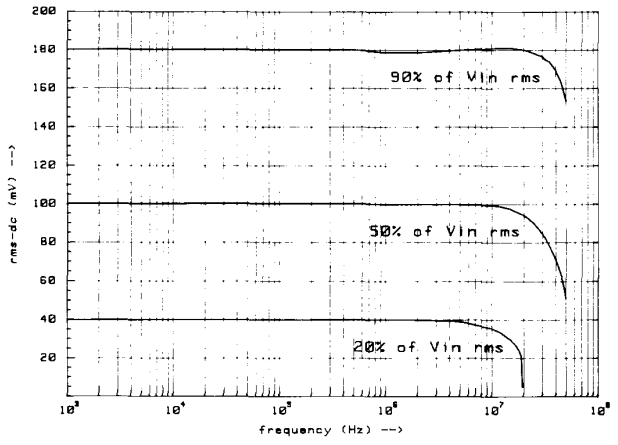


Fig. 23. Measured transfer curves of rms–dc convertor version II, as a function of frequency.

TABLE II
MEASURED LINEARITY ERROR, VERSION II

Crest factor	Peak linearity error (% FS) $V_{in,\ peak}$ = (CF). 200 mV
1	1.0%
1.4	0.7%
2	0.8%
3.2	0.7%
4.5	0.4%

tude of the input signal. A -1-percent bandwidth for an amplitude of 90 percent of FS is measured as 22 MHz. For 20 percent for FS it amounts to 2.5 MHz; the -10-percent bandwidth for 90- and 20-percent FS is 52 and 9 MHz, respectively.

VI. CONCLUSIONS

In computational circuits for wide-band rms–dc conversion implemented on the basis of the translinear principle, the rectifier function can be adequately avoided. The high-frequency performance of both newly devised versions of rms–dc conversion is much improved with respect to existing circuit solutions. However, for small signals, the bandwidth of version II is decreased by the low bias setting, imposed on the V–I convertor by the feedback loop. Higher bias currents would improve the bandwidth. Emitter-area mismatch in version I needs (automatic) periodical trimming. In version II mismatch influence cancelling is obtained by scaling input and output current to one another. Scaling of input current is carried out by exploiting the current-dividing feature of a translinear V-to-I convertor and leads to freedom from trimming at the cost of some bandwidth.

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