# New Two-Inductor Boost Converter With Auxiliary Transformer

Yungtaek Jang, Senior Member, IEEE, and Milan M. Jovanović, Fellow, IEEE

Abstract—A new, two-inductor, two-switch boost converter topology and its variations suitable for applications with a large difference between the input and output voltage are described. The output voltage regulation of the proposed converters is achieved in a wide load and input-voltage range with constant-frequency control by employing an auxiliary transformer that couples the current paths of the two boost inductors.

Index Terms—Auxiliary transformer, boost converter, pulse width modulation, two inductor.

#### I. INTRODUCTION

Converter topology and its variations exhibit a satisfactory performance in the majority of applications where the output voltage is greater than the input voltage. Nevertheless, in a number of high-power applications, the performance of the boost converter can be improved by implementing a boost converter with multiple switches and/or multiple boost inductors. Usually, multiple-switch and/or multiple-inductor boost topologies are employed in high input-current and/or high input-to-output voltage conversion applications. So far, a number of isolated and nonisolated multiple-switch and/or multiple-inductor topologies have been proposed, analyzed, and evaluated [1]–[10].

As an example, an interleaved boost topology is sometimes used in high-power applications to eliminate reverse-recovery losses of the boost rectifier by operating the two boost converters at the boundary of continuous-conduction mode (CCM) and discontinuous-conduction mode (DCM) so that the boost switches are turned on when the current through the corresponding boost rectifier is zero [1]–[4]. Generally, interleaving is employed to reduce the input current ripple and, therefore, to minimize the size of the input filter that would be relatively large if a single DCM boost converter were used. However, to achieve the operation at the CCM/DCM boundary under varying line and load-current conditions, the interleaved boost converter requires variable switching frequency control which is often more complex to implement than constant-frequency control [1]–[4]. In addition, variable-frequency control in some applications is not desirable.

Another multiswitch boost converter is proposed in [5] for high-power applications that require an isolated PFC implementation. The circuit can also be employed in applications that re-

Manuscript received January 9, 2003; revised August 19, 2003. Recommended by Associate Editor P. K. Jain.

The authors are with the Power Electronics Laboratory, Delta Products Corporation, Research Triangle Park, NC 27709 USA (e-mail: ytjang@deltartp.com).

Digital Object Identifier 10.1109/TPEL.2003.820588

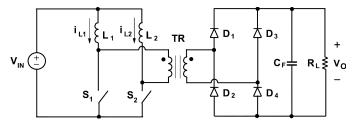


Fig. 1. Conventional two-inductor boost converter.

quire a high input-to-output-voltage conversion ratio. However, this current-fed push-pull converter suffers from a high voltage stress on the primary switches and high peak currents of the boost inductor and output capacitor.

Finally, the two-inductor, two-switch circuit shown in Fig. 1 that is described in [6]–[10] exhibits some interesting properties. Specifically, the main feature of this circuit is that the voltage stress of each switch is one half the voltage stress of the switches in the single-inductor implementation in [5]. In addition, the input current is distributed evenly through the two boost inductors so that the current ripple in the output capacitor is smaller than in the single-inductor implementation. However, the major limitation of the two-inductor circuit in Fig. 1 is its inability to regulate the load in a wide range with constant-frequency control. To facilitate the explanation of this limitation, Fig. 2 shows key waveforms of the circuit in Fig. 1. As can be seen from Fig. 2, current  $i_{L1}$  in inductor  $L_1$  increases during the entire on time of switch  $S_1$  and decreases during the entire off time of switch  $S_1$ . Similarly, current  $i_{L2}$  in inductor  $L_2$  increases during the on time of switch  $S_2$  and decreases during its off time. As a result, even when the effective converter duty cycle D, which is defined as the ratio of the overlapping conduction time of the two switches to half of their switching period, is reduced to zero, the inductors continue to store energy since switches  $S_1$  and  $S_2$ are conducting for half of switching period  $T_S$ . To reduce the stored energy and extend the load regulation range, it is necessary to shorten the conduction time of the switches. This can be accomplished by increasing the switching frequency. Therefore, the circuit in Fig. 1 requires variable-frequency control to maintain the output voltage regulation in a wide load range.

In this paper, a new two-inductor, two-switch boost converter topology that can achieve output-voltage regulation from full load to no load in a wide input-voltage range using constant-frequency control is introduced. This topology employs an auxiliary transformer with a unity turns ratio to couple the current paths of the two boost inductors so that both inductors conduct identical currents. Due to this current-mirror effect of the auxiliary transformer, no energy is stored in the inductors when there is no overlapping of conduction times of the two switches, i.e.,

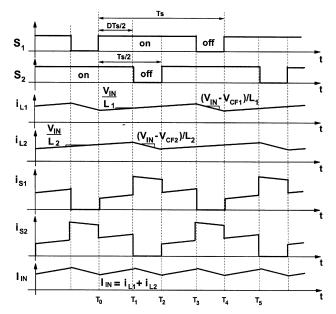


Fig. 2. Key waveforms of conventional two-inductor boost converter shown in Fig. 1 where voltages  $V_{CF1}$  and  $V_{CF2}$  are reflected output voltage  $V_{O}$  at the primary side of transformer TR.

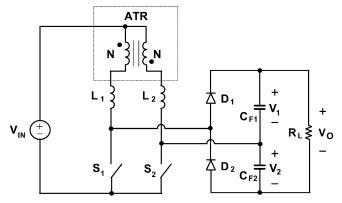


Fig. 3. Proposed two-inductor boost converter with auxiliary transformer.

when D=0. This auxiliary-transformer approach can be applied to isolated or nonisolated two-inductor, two-switch topologies with any type of output rectifier.

# II. ANALYSIS OF OPERATION

A nonisolated implementation of the boost circuit described in this paper is shown in Fig. 3. The input side of the circuit consists of two switches  $S_1$  and  $S_2$ , two boost inductors  $L_1$  and  $L_2$ , and auxiliary transformer ATR. To maximize the voltage gain of the converter, the output side of the circuit is configured as a voltage doubler rectifier that consists of boost rectifiers  $D_1$  and  $D_2$  and output filter capacitors  $C_{F1}$  and  $C_{F2}$  connected across load  $R_L$ .

To facilitate the explanation of the circuit operation, Fig. 4 shows a simplified circuit diagram of the circuit in Fig. 3. In the simplified circuit, auxiliary transformer ATR is modeled as an ideal transformer with turns ratio  $n_{ATR}=1$  and four times of magnetizing inductance  $L_M$ . It should be noted that magnetizing inductance  $L_M$  is the measured inductance across one of the windings of auxiliary transformer ATR which has an unity turns ratio. In addition, it is assumed that filter capacitors  $C_{F1}$ 

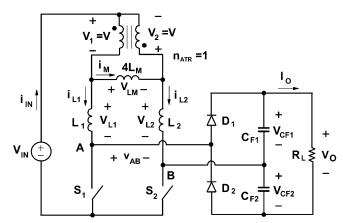


Fig. 4. Simplified circuit model of proposed converter that shows reference directions of currents and voltages.

and  $C_{F2}$  are large enough so that the voltage ripple across them is small compared to their dc voltages. Finally, in this analysis it is also assumed that all semiconductor components are ideal, i.e., that they represent zero impedances while in the on state and infinite impedances while in the off state.

To further facilitate the analysis of operation, Fig. 5 shows the topological stages of the circuit in Fig. 3 during a switching cycle, whereas Fig. 6 shows its key waveforms. The reference directions of currents and voltages plotted in Fig. 6 are shown in Fig. 4. As can be seen from the timing diagrams of the control signals for switches  $S_1$  and  $S_2$  shown in Fig. 6, switches  $S_1$  and  $S_2$  conduct simultaneously, i.e., they operates with overlapping control signals. The time of the simultaneous conduction, defined from the turn-on moment of one switch until the turn-off instant of the other switch, represents duty cycle period DTs/2 of the converter, as indicated in Fig. 6.

During the time interval when both switches are on, i.e., during the time interval  $T_0-T_1$  in Fig. 6, inductor currents  $i_{L1}$  and  $i_{L2}$  are increasing at the same rate. The rate of change of  $i_{L1}$  and  $i_{L2}$  can be calculated from Fig. 5(a), which represents the equivalent circuit diagram of the converter during the time interval  $T_0-T_1$ . Since according to Figs. 4 and 5(a)

$$V_{\rm IN} = v_1 + V_{L1} \tag{1}$$

and

$$V_{\rm IN} = -v_2 + V_{L2} \tag{2}$$

where  $v_1 = v_2 = -V_{LM}/2$  because  $n_{ATR} = 1$ . Since input current  $i_{\rm IN}$  is always divided equally through the ideal transformer windings of the ATR model

$$\frac{di_{L1}}{dt} = \frac{di_{IN}}{2dt} - \frac{di_M}{dt} \tag{3}$$

and

$$\frac{di_{L2}}{dt} = \frac{di_{IN}}{2dt} + \frac{di_M}{dt}.$$
 (4)

Therefore, by substracting (4) from (3)

$$\frac{V_{L1}}{L_1} - \frac{V_{L2}}{L_2} = -\frac{V_{LM}}{2L_M}. (5)$$

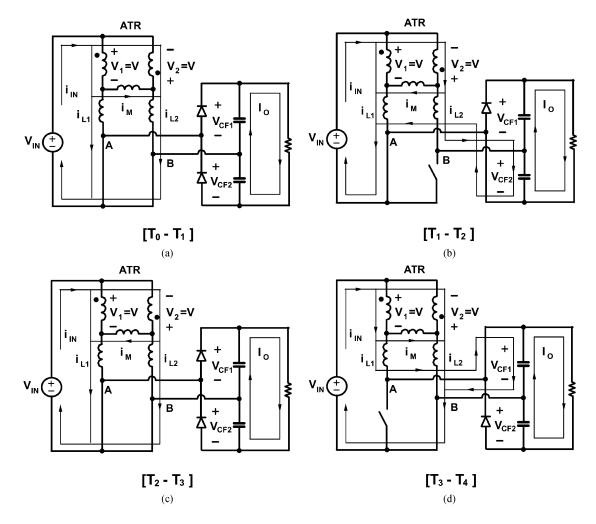


Fig. 5. Topological stages of proposed converter.

From (1), (2), and (5)

$$V_{LM} = \frac{2(L_1 - L_2)}{L_1 + L_2 + \left(\frac{L_1 L_2}{L_M}\right)} V_{IN}.$$
 (6)

If both inductances have the same value  $L=L_1=L_2$ , it follows that  $V_{LM}=0$  and

$$\frac{di_{L1}}{dt} = \frac{di_{L2}}{dt} = \frac{V_{\rm IN}}{L} \tag{7}$$

as indicated in Fig. 6.

The output is decoupled from the input when both switches are on and rectifiers  $D_1$  and  $D_2$  are reverse biased. As a result, during this stage the load current is supplied from the filter capacitors and capacitor voltages  $V_{CF1}$  and  $V_{CF2}$  slowly decrease, as seen in Fig. 6. Since output voltage  $V_O = V_{CF1} + V_{CF2}$ , the output voltage also slowly decreases.

When at  $t=T_1$  switch  $S_2$  is turned off, inductor current  $i_{L2}$  is diverted from the switch to rectifier  $D_2$ , as shown in Fig. 5(b), and the energy stored in inductor  $L_2$  starts to discharge into filter capacitor  $C_{F2}$ . The rate of change of  $i_{L1}$  and  $i_{L2}$  can be calculated from Fig. 5(b), which represents the equivalent circuit diagram of the converter during the time interval  $T_1-T_2$ . Since according to Figs. 4 and 5(b)

$$V_{\rm IN} = v_1 + V_{L1} \tag{8}$$

and

$$V_{\rm IN} = -v_2 + V_{L2} + V_{CF2}. (9)$$

Because the condition of (5) is true during this period,  $V_{LM}$  can be derived from (5), (8), and (9) as

$$V_{LM} = \frac{2(L_1 - L_2)}{L_1 + L_2 + \left(\frac{L_1 L_2}{L_M}\right)} V_{IN} - \frac{2V_{CF2}}{1 + \frac{L_2}{L_1} + \frac{L_2}{L_M}}.$$
 (10)

If both inductances have the same value  $L=L_1=L_2$  and  $V_{CF}=V_{CF1}=V_{CF2}$ 

$$V_{LM} = -\frac{V_{CF}}{1 + \frac{L}{2L_M}}. (11)$$

Therefore, from (8), (9), and (11)

$$\frac{di_{L1}}{dt} = \frac{1}{L} \left( V_{\text{IN}} - \frac{V_{CF}}{2 + \frac{L}{L_{CF}}} \right) \text{ and}$$
 (12)

$$\frac{di_{L2}}{dt} = \frac{1}{L} \left( V_{\rm IN} + \frac{V_{CF}}{2 + \frac{L}{L_M}} - V_{CF} \right) \tag{13}$$

as indicated in Fig. 6.

Because during the topological stage shown in Fig. 5(b), current  $i_{L2}$  charges capacitor  $C_{F2}$ , capacitor voltage  $V_{CF2}$  increases. At the same time, voltage  $V_{CF1}$  across capacitor

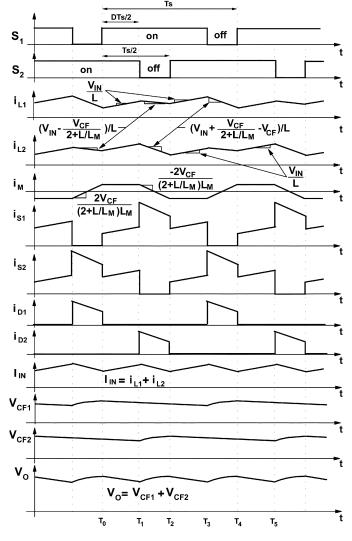


Fig. 6. Key waveforms of proposed converter.

 $C_{F1}$  continues to decrease because this capacitor continues to be discharged by the load current, as shown in Fig. 6.

When at  $t=T_2$  switch  $S_2$  is turned on again, the circuit enters the topological stage shown in Fig. 5(c), which is identical to the topological stage in Fig. 5(a). During this stage both switches are on and both inductor currents  $i_{L1}$  and  $i_{L2}$  increase at the same rate given by (7). At the same time, both output filter capacitors are being discharge by the load current since rectifiers  $D_1$  and  $D_2$  are reverse biased and the output part of the circuit is decoupled from the input part.

The converter enters the final topological stage shown in Fig. 5(d) at  $t=T_3$  when switch  $S_1$  is turned off and current  $i_{L1}$  is commutated from the switch into rectifier  $D_1$ . During this stage, energy stored in inductors  $L_1$  and  $L_2$  during the preceding topological stage discharges into capacitor  $C_{F1}$ . The rates of decrease of currents  $i_{L1}$  and  $i_{L2}$  are

$$\frac{di_{L1}}{dt} = \frac{1}{L} \left( V_{\rm IN} + \frac{V_{CF}}{2 + \frac{L}{L_{col}}} - V_{CF} \right) \text{ and}$$
 (14)

$$\frac{di_{L2}}{dt} = \frac{1}{L} \left( V_{\rm IN} - \frac{V_{CF}}{2 + \frac{L}{L_{M}}} \right), \text{ respectively.}$$
 (15)

Due to the flow of current  $i_{L1}$  into capacitor  $C_{F1}$ , voltage  $V_{CF1}$  increases, whereas voltage  $V_{CF2}$  continues to decrease because capacitor  $C_{F2}$  continues to be discharged by the load current. The circuit enter a new switching cycle at  $t=T_4$  when switch  $S_1$  is turned on again.

The voltage conversion ratio of the circuit can be calculated from the volt-second balance on the boost inductors. From Figs. 5 and 6, the volt-second balance equation for  $L_1$  is

$$V_{\rm IN}D\frac{T_S}{2} = \left(\frac{V_{CF}}{2} - V_{\rm IN}\right) \cdot \left(\frac{T_S}{2} - D\frac{T_S}{2}\right) \tag{16}$$

so that

$$\frac{V_O}{V_{\rm IN}} = \frac{4}{1 - D} \tag{17}$$

since  $V_O=2V_{CF}$ . As can be seen from (17), the output voltage of the converter in Fig. 3 is at least four times larger than the input voltage. This high conversion ratio makes this converter very suitable for applications with a large difference between the output and input voltage.

It also should be noted that because of the converter's unique property to simultaneously charge and discharge both boost inductors due to the coupling of inductor currents through the auxiliary transformer, the converter can maintain the regulation of the output voltage with a constant frequency control in a wide range of the load current. Namely, with the duty cycle close to unity, the maximum power is transferred from the input to the output since the maximum energy is stored in the inductors. As the duty cycle decreases toward zero, less and less energy is stored in both inductors, which enables the output voltage regulation leg down to very light loads. Finally, it should be noted that if  $L_1 = L_2 = L$  and  $n_{ATR} = 1$ , both inductors in Fig. 3 store and transfer the same amount of energy, i.e., each of the converter processes one half of the total power. Since the total power is processed in two parallel legs, the conduction loss of the circuit is reduced compared to a circuit with a single power path.

Since, according to (17), proper operation of the circuit in Fig. 3 requires the output voltage to be at least four times greater than the input voltage, the output capacitors need to be precharged during a start-up period. This precharging can be implemented solely by a proper design of the control circuit, i.e., without any additional components. To accomplish this, switches  $S_1$  and  $S_2$  should be operated with complimentary switching (D=0) for a fixed time interval during the start-up period. Since boost inductors  $L_1$  and  $L_2$  are saturated by the charging current during the start-up period, the magnetizing inductance of ATR is much larger than the inductances of boost inductors  $L_1$  and  $L_2$ . As a result, ATR operates as an auto transformer with a 1:2 turns ratio when switches  $S_1$  and  $S_2$  operate with complimentary switching so that each output capacitor is charged to two times the input voltage. After the output voltage reaches approximately four times the input voltage, the duty cycle of the converter should be linearly increased to the steady-state value to obtain the desired output voltage.

Finally, it should be noted that a number of other implementations of the two-inductor, two-switch conveter with the ATR are possible. As an illustration, Fig. 7(a) shows the implementation with an isolation transformer and a full-wave bridge rectifier. The operation of this isolated circuit and its properties are similar to those of the nonisolated converter in Fig. 3. However, the

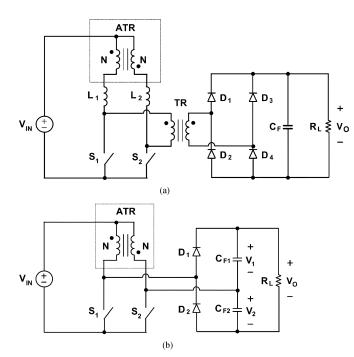


Fig. 7. Topology variations of proposed two-inductor boost converter: (a) implementation with isolation transformer and full-wave rectifier and (b) implementation with integrated magnetics.

leakage inductance of the isolation transformer may result in severe voltage ringing on the switches. To prevent this undesirable voltage stress, an additional snubber circuit is required [6]. The circuit in Fig. 3 can also be implemented with a single magnetic component, as shown in Fig. 7(b). In this integrated magnetics implementation, the auxiliary transformer and the boost inductors can be integrated in a variety of ways. For example, the integration can be achieved by adjusting the coupling between the transformer windings so that the leakage inductance of the transformer windings is used as the boost inductances.

#### III. EXPERIMENTAL RESULTS

### A. Specifications

To verify the operation and evaluate the performance, a 1-kW, two-inductor boost rectifier was designed to the following specifications.

- Input Voltage  $V_{\text{in}}$ : 40 V<sub>DC</sub>-70 V<sub>DC</sub>.
- Input Current Ripple: <5%.
- Output Voltage  $V_0$ : 380  $V_{DC}$  (0-100% load).
- Power  $P_0$ : 1 kW.
- Ripple Voltage:  $<6.5~V_{\rm peak-peak}$  (80 kHz).
- Switch Frequency  $f_S$ : 40 kHz.
- Efficiency: >90% at full load.
- · Cooling: Force Convection.

# B. Component Selections

Semiconductors: Since the drain voltages of switches  $S_1$  and  $S_2$  are clamped to output capacitors  $C_{F1}$  and  $C_{F2}$ , respectively, the peak voltage stress on switches  $S_1$  and  $S_2$  is approximately 190 V. The peak current stress on switches  $S_1$  and  $S_2$  that occurs at full load and low line is approximately 27.5 A. Therefore, two IRFP264 MOSFET's  $(V_{DSS} = 250 \text{ V}, I_{D25} = 38 \text{ A},$ 

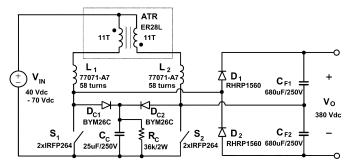


Fig. 8. Schematic diagram of 1-kW, two-inductor boost converter with auxiliary transformer.

 $R_{DS}=0.075~\Omega$ ) from IR connected in parallel were used for each of the switches. Since output diodes  $D_1$  and  $D_2$  must block the output voltage and must conduct the peak load current which is 2.9 A, a RHRP1560 diode ( $V_{RRM}=600~\mathrm{V}, I_{FAVM}=15~\mathrm{A}$ ) from Fairchild was used as output diodes  $D_1$  and  $D_2$ . To reduce the conduction losses of the switches and output diodes, devices which have higher current ratings than the designed maximum current were selected.

Boost Inductor: To obtain the desired inductance of boost inductors  $L_1$  and  $L_2$ , each boost inductor was built using a toroidal core (Magnetics, Kool- $\mu$  77 071-A7) and 58 turns of magnet wire (AWG #14). The measured inductance of boost inductors  $L_1$  and  $L_2$  is approximately 88  $\mu$ H at 13 A bias current. The peak-to-peak ripple current is approximately 20% of the average boost inductor current at full load. A ferrite toroidal core (Philips, Ferrite TX29/19/7.6) was used in parallel with a Kool- $\mu$  core to increase the continuous conduction mode operation boundary. Specifically, a Kool- $\mu$  core and a ferrite toroidal core were wound together using magnet wire. As indicated in (11), the stored energy in magnetizing inductance  $L_M$  is proportional to the ratio of magnetizing inductance  $L_M$  and boost inductor L. By using a ferrite toroidal core, the stored energy in magnetizing inductance  $\mathcal{L}_{M}$  is almost negligible at light load condition because the inductance of boost inductor L is much larger than magnetizing inductance  $L_M$ . The measured inductance of boost inductors  $L_1$  and  $L_2$  is approximately 15 mH at no bias current.

Auxiliary Transformer: ATR was built using a pair of ferrite cores (Philips, ER28L-3F3) with an air gap (2 mils). Two AWG #14 magnet wires with equal number of turns (11 turns:11 turns) were used to obtain a desired magnetizing inductance which is approximately 100  $\mu$ H.

Capacitors: Two aluminum capacitors (680  $\mu$ F, 250 VDC) were used for output capacitors  $C_{F1}$  and  $C_{F2}$ . Both capacitors have equal voltage stresses which is equal to half the output voltage, since the converter naturally balances the voltages of output capacitors  $C_{F1}$  and  $C_{F2}$ .

Clamp Circuit: It should be noted that an accidental simultaneous opening of both switches would lead to a catastrophic circuit failure since the energy stored in the boost inductors would not have a path to discharge. Therefore, to prevent the circuit failure, it is necessary to provide a discharging path for the energy of the boost inductors when both switches are open. Fig. 8 shows a protection circuit implemented with a RCD snubber connected across the switches. The clamp circuit consists of two

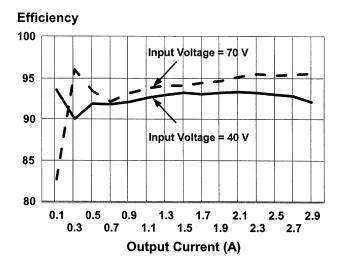


Fig. 9. Measured efficiency of prototype circuit for  $V_O = 380 \text{ V}$ .

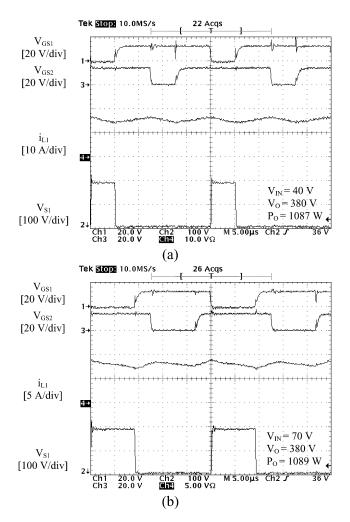


Fig. 10. Measured gate-to-source voltage waveforms  $V_{GS1}$  and  $V_{GS2}$ , boost-inductor current waveform  $I_{L1}$ , and drain-to-source voltage waveform  $V_{S1}$ , at: (a)  $V_{\rm IN}=40$  V,  $P_O=1087$  W, and  $V_O=380$  V: (b)  $V_{\rm IN}=70$  V,  $P_O=1089$  W, and  $V_O=380$ . Time base 5  $\mu$ s/div.

diodes  $D_{C1}$  and  $D_{C2}$ , capacitor  $C_C$ , and resistor  $R_C$ . An aluminum capacitor (25  $\mu \rm F$ , 250 VDC) was used for clamp capacitor  $C_C$  and a carbon resistor (36 k $\Omega$ /2 W) was used for clamp resistor  $R_C$ .

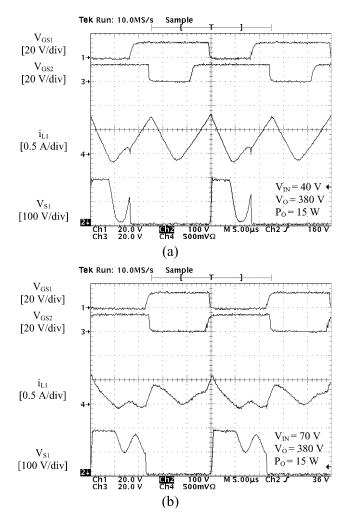


Fig. 11. Measured gate-to-source voltage waveforms  $V_{GS1}$  and  $V_{GS2}$ , boost-inductor current waveform  $I_{L1}$ , and drain-to-source voltage waveform  $V_{S1}$ , at (a)  $V_{\rm IN}=40\,{\rm V},\,P_O=15\,{\rm W},\,{\rm and}\,V_O=380\,{\rm V},\,{\rm and}\,({\rm b})\,V_{\rm IN}=70\,{\rm V},\,P_O=15\,{\rm W},\,{\rm and}\,V_O=380$ . Time base 5  $\mu$ s/div.

# C. Experimental Results

The performance of the proposed two-inductor boost converter was verified on a 1-kW prototype circuit that was designed to operate from a 40–70-V battery input and deliver up to 2.9 A at a 380-V output. The simplified schematic diagram is shown in Fig. 8. This converter was operated at 40 kHz switching frequency. However, the ripple of the input current and the ripple of the output voltage are 80 kHz, since the switching periods of the two switches are interleaved as shown in Fig. 6. The efficiency measurements for the prototype converter at 40 V and 70 V input are summarized in Fig. 9. As can be seen from the figure, the measured full-load efficiency was around 92% at the minimum line voltage. The peaking of efficiency at  $I_{\rm OUT}=0.3$  A for  $V_{\rm IN}=70$  V and at  $I_{\rm OUT}=0.1$  A for  $V_{\rm IN}=40$  V indicates the saturation of the ferrite toroidal core in boost inductors  $L_1$  and  $L_2$ .

Figs. 10 and 11 show the measured waveforms of the proposed two-inductor boost converter at 40 V and 70 V input voltages under the full load and 1.5% load conditions, respectively. As can be seen in the figures, the boost inductor current increases during the period when both switches  $S_1$  and  $S_2$  are

on. During the period when one of the switches is off, the boost inductor current decreases. There is a good agreement between the experimental and theoretical waveforms. It should be noted that the blocking voltage of the switch is approximately 190 V which is half of the output voltage. Moreover, inductor current  $i_{L1}$  is also half of the input current, since two inductors  $L_1$  and  $L_2$  share the current equally.

### IV. CONCLUSION

A new two-inductor, two-switch boost converter topology and its variations that can regulate the output voltage in a wide range of load current and input voltage with a constant-frequency control are introduced. The constant-frequency control is achieved with the employment of a unity-turns-ratio auxiliary transformer that couples the current paths of the two inductors and forces them to be virtually identical. Since in this topology no energy can be stored in the inductors when the conduction times of the switches do not overlap (D=0), the output voltage can be regulated from full load down to practically no load.

The described two-inductor topologies with the auxiliary transformer are suitable for applications that require a high input-to-output voltage conversion ratio. Specifically, a nonisolated implementation with a voltage-doubler rectifier exhibits a voltage gain that is four times of the corresponding gain of the conventional nonisolated boost converter

The performance of the proposed two-inductor boost converter was verified on a 1-kW prototype circuit that was designed to operate from a 40–70-V battery voltage input and deliver up to 2.9 A at a 380-V output.

#### REFERENCES

- M. S. Elmore, "Input current ripple cancellation in synchronized, parallel connected critically continuous boost converters," in *Proc. IEEE Appl. Power Electron. Conf. (APEC)*, 1996, pp. 152–158.
- [2] J. W. Kolar, G. R. Kamath, N. Mohan, and F. C. Zach, "Self-adjusting input current ripple cancellation of coupled parallel connected hysteresis-controlled boost power factor correctors," in *Proc. IEEE Power Electron. Spec. Conf.*, 1995, pp. 164–173.
- [3] B. T. Irving, Y. Jang, and M. M. Jovanović, "A comparative study of soft-switched CCM boost rectifiers and interleaved variable-frequency DCM boost rectifier," in *Proc. IEEE Appl. Power Electron. Conf. (APEC)*, 2000, pp. 171–177.

- [4] J. Zhang, J. Shao, P. Xu, F. C. Lee, and M. M. Jovanović, "Evaluation of input current in the critical mode boost PFC converter for distributed power systems," in *Proc. IEEE Appl. Power Electron. Conf. (APEC)*, 2001, pp. 130–136.
- [5] E. X. Yang, Y. Jiang, G. Hua, and F. C. Lee, "Isolated boost circuit for power correction," in *Proc. IEEE Appl. Power Electron. Conf. (APEC)*, 1993, pp. 196–203.
- [6] P. J. Wolfs, "A current-sourced dc-dc converter derived via duality principle from half bridge converter," *IEEE Trans. Ind. Electron.*, vol. 40, pp. 139–144, 1993.
- [7] G. Ivensky, I. Elkin, and S. Ben-Yaakov, "An isolated dc-dc converter using two zero current switched IGBT's in a symmetrical topology," in Proc. IEEE Power Electron. Spec. Conf., 1994, pp. 1218–1225.
- [8] W. C. P. de Aragão Filho and I. Barbi, "A comparison between two current-fed push-pull dc-dc converters—Analysis, design and experimentation," in *Proc. IEEE Int. Telecommun. Energy Conf.*, 1996, pp. 313–320.
- [9] W. Abida, D. Sadarnac, and P. Henrard, "Minimization of conduction losses in the boost converter with galvanic isolation," in *Proc. IEEE Int. Telecommun. Energy Conf.*, 2001, pp. 334–340.
- [10] Z. I. Kovatchev, "Design of 1.2 kW inverter building block for telecommunication supply systems," in *Proc. IEEE Int. Telecommun. Energy Conf.*, 2002, pp. 188–194.



Yungtaek Jang (S'92–M'95–SM'01) was born in Seoul, Korea. He received the B.S. degree from Yonsei University, Seoul, in 1982, and the M.S. and Ph.D. degrees from the University of Colorado, Boulder, in 1991 and 1995, respectively, all in electrical engineering.

From 1982 to 1988, he was a Design Engineer at Hyundai Engineering Co., Seoul. From 1995 to 1996, he was a Senior Engineer at Advanced Energy Industries, Inc., Fort Collins, CO. Since 1996, he has been a Senior Member of R&D Staff at the Delta Power

Electronics Laboratory, Research Triangle Park, NC. He holds 17 U.S. patents and has published more than 30 papers in power electronics journals and conferences. His research interests include high-frequency power conversion, converter modeling, control techniques, and low harmonic rectification.

Dr. Jang received the IEEE TRANSACTIONS ON POWER ELECTRONICS Prize paper award for the best paper published in 1996.



**Milan M. Jovanović** (F'01) was born in Belgrade, Serbia. He received the Dipl.Ing.degree in electrical engineering from the University of Belgrade, Serbia.

Presently, he is the Vice President for Research and Development of Delta Products Corporation, Research Triangle Park, NC (U.S. subsidiary of Delta Electronics, Inc., Taiwan).