nMOS Reversible Energy Recovery Logic for Ultra-Low-Energy Applications

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***Abstract*—We propose a new fully reversible adiabatic logic, nMOS reversible energy recovery logic (nRERL), which uses nMOS transistors only and a simpler 6-phase clocked power. Its area overhead and energy consumption are smaller, compared with the other fully adiabatic logics. We employed bootstrapped nMOS switches to simplify the nRERL circuits. With the simulation results for a full adder, we confirmed that the nRERL circuit consumed substantially less energy than the other adiabatic logic circuits at low-speed operation. We evaluated a test chip implemented with 0.8-μm CMOS technology, which included a chain of nRERL inverters integrated with a clocked power generator. The nRERL inverter chain of 2400 stages consumed the minimum energy at $V_{\rm dd} = 3.5$ V at 55 kHz, where the adiabatic and leakage losses are about equal, which is only 4.50% of the dissipated energy of its corresponding CMOS circuit at $V_{\rm dd} = 0.9$ V. In conclusion, nRERL is more suitable than the other adiabatic logic circuits for the applications that do not require high performance but low energy consumption.**

***Index Terms*—6-phase clocked power generator, adiabatic circuit, bootstrapped switch, energy consumption, nMOS reversible energy recovery logic.**

I. Introduction

BESIDES leakage loss, the adiabatic circuits have two types of energy consumption: adiabatic loss and nonadiabatic loss. The adiabatic loss always exists if there is charge transfer through a turned-on switch. This loss, which is unavoidable for any logic operation, is inversely proportional to the transition time of the clocked power if the clock transition time is sufficiently larger than the time constant of the circuit [1]. This adiabatic-switching condition must be satisfied for proper operation. In contrast, the nonadiabatic loss occurs only if there is nonzero voltage difference between the two terminals of a switch when it is turned on. This nonadiabatic loss, which does not depend on the operating frequency, can be much larger than the adiabatic loss if the operating frequency is lowered.

We can classify the adiabatic circuits into two classes: quasi-adiabatic circuits, which have nonadiabatic loss, and fully adiabatic circuits, which do not have any nonadiabatic loss. Here, we just consider the frequency range where the adiabatic-switching condition is satisfied. If the rise–fall time of the clocked power is too short, the adiabatic circuit does not function properly. Therefore, there exists the minimum clock transition time for an adiabatic circuit. With SPICE simulation, we found the ratio of the minimum clock transition time to the time-constant frequency for several adiabatic circuits: about 1 for 2N-2N2P [2] and SCRL [3], 3.5 for transmission-gate RERL (tRERL)[4]–[6], and 4.2 for nRERL. In all the simulations in this paper, we used the SPICE parameters for a 0.8-μm CMOS technology, with which a test chip was fabricated. We will refer to the RERL [4]–[6] as tRERL to distinguish it from nRERL.

In the quasi-adiabatic circuits [2], [7]–[9], we can divide the range of operating frequency into three regions: adiabatic-loss-dominant one, nonadiabatic-loss-dominant one and leakage-loss-dominant one, as shown in Fig. 1(a). The adiabatic loss is dominant in the highest operating frequency range in the adiabatic circuits. If the operating frequency is lowered in the adiabatic-loss-dominant region, the energy consumption is reduced linearly. If the operating frequency is lowered further, the energy consumption remains constant because the circuit

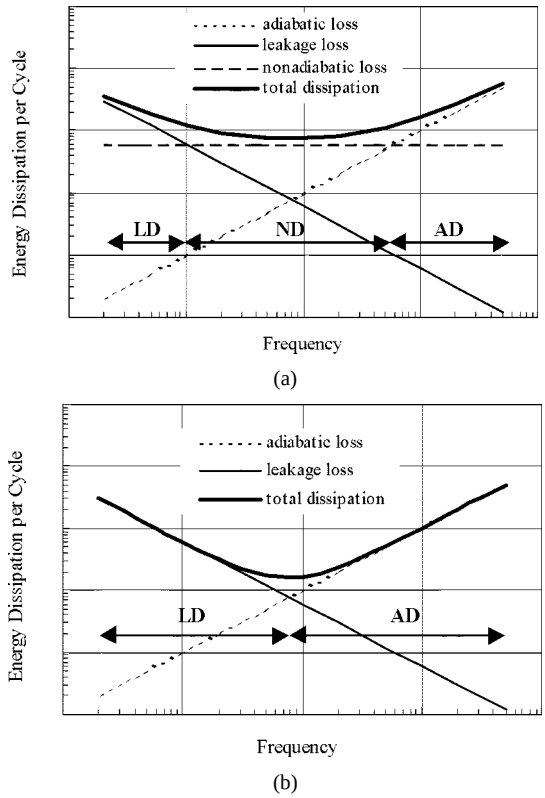

Fig. 1. (a) Energy curve for a quasi-adiabatic circuit. (b) Energy curve for a fully adiabatic circuit. LD, ND, and AD stand for the leakage-loss-dominant, nonadiabatic-loss-dominant, and adiabatic-loss-dominant regions, respectively.

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is in the nonadiabatic-loss-dominant region. If the operating frequency is lowered continuously, the circuit goes into the leakage-loss-dominant region so that the energy consumption is increased.

In the fully adiabatic circuits, which employed the reversible logic to eliminate the nonadiabatic loss virtually [3]–[6], there are only two distinct regions: adiabatic-loss-dominant and leakage-loss-dominant regions as shown in Fig. 1(b). Because the energy consumption is increased in the leakage-loss-dominant region if the operating frequency is lowered, the energy consumption can be reduced until the adiabatic loss is comparable to the leakage loss. The circuit operation in the leakage-current level is attractive for the ultra-low-energy applications. However, the complexity of the fully adiabatic circuits is high because they have both forward and backward logic paths due to reversible logic. Consequently, they require a larger silicon area. Furthermore, the number of phases required in the clocked power is large. For example, the number of required clock rails is 24 in split-level charge recovery logic (SCRL) [3], and 8 in both tRERL [4]–[6] and Patra's work [10]. To make a fully adiabatic circuit more competitive, its circuit complexity must be reduced further as well as its clocked power.

In the fully adiabatic circuits, there are two types of switches in a logic stage: logic and isolation. Logic switches are used to implement a logic function and isolation switches are used to connect or disconnect an output node to/from its energy-charging path and its energy-discharging path. To avoid nonadiabatic loss due to the signal degradation, the transmission gates have been used for both the isolation switch and the logic switch [1], [3]–[6], although their area overhead is relatively large. However, recently Tzartzanis used a bootstrapped nMOS switch instead of a transmission gate as a logic switch because a bootstrapped switch, which consists of two nMOS transistors, occupies less area and has lower turn-on resistance [11], [12].

Patra [10] also mentioned briefly the implementation of a fully adiabatic circuit with an 8-phase clocked power by using the bootstrapped switch. In this paper, we propose nRERL, which is a simpler fully adiabatic logic with a 6-phase clocked power. We use only nMOS transistors in nRERL by utilizing the bootstrapped switches instead of the transmission gates. Therefore, we can reduce the energy consumption substantially, because a bootstrapped switch requires less area and has lower turn-on resistance, compared with a transmission gate.

In Section II, we explain the nMOS switches used in nRERL. We describe the operation of an nRERL buffer and its clocking method, and present the simulation result of an nRERL full adder in Section III. We explain a 6-phase, clocked power generator in Section IV. We present the experimental results of the test chip in Section V, which is followed by the conclusion in Section VI.

II. Bootstrapped Switches in nRERL

In this section, we describe the operation and energy consumption of a bootstrapped switch in a fully adiabatic circuit. Then we derive the optimal supply voltage for the minimal energy consumption of a bootstrapped switch for a given threshold voltage. We also explain how a bootstrapped switch is used in nRERL to eliminate the nonadiabatic loss. To eliminate the nonadiabatic loss in the adiabatic circuits, each switch should be turned on or off only when there is no voltage difference between its two terminals, which will be referred to as the zero-voltage switching (ZVS) condition. In addition, we show how its energy consumption is changed when the supply voltage and the transistor size are scaled.

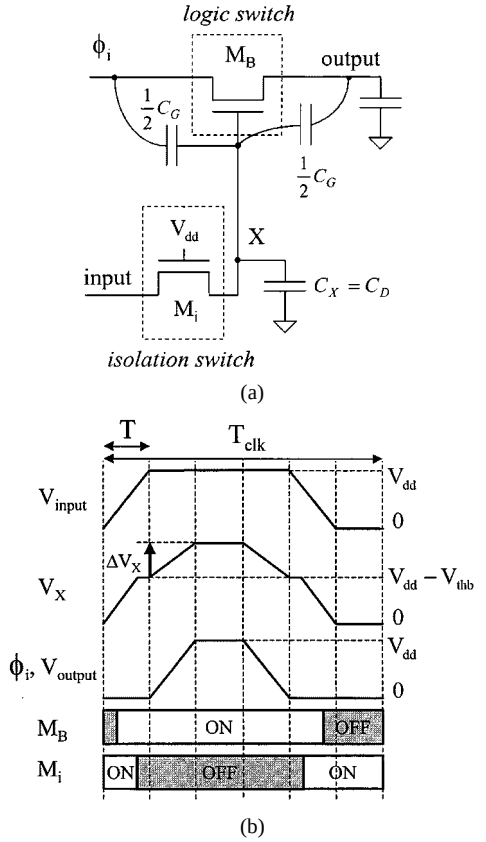


Fig. 2. A bootstrapped nMOS switch. (a) A logic switch and an isolation switch. (b) Their node waveforms and ON-OFF diagram.

A. Operation of a Bootstrapped Switch

A bootstrapped switch in nRERL consists of two nMOS transistors: a logic switch M_B and an isolation switch M_i, as shown in Fig. 2(a). Assume that all the nodes in Fig. 2(a) are low initially. If the input is low, M_B is off. Therefore, the output stays low while the clocked power ϕ_i is rising.

When the input is charged up slowly, the node X goes up to about $V_{dd} - V_{thb}$ and isolation switch M_i is turned off so that the node X is in the high-impedance state. Concurrently, logic switch M_B becomes on without nonadiabatic loss because both the two terminals, ϕ_i and output, are grounded, as shown in Fig. 2(b). Here, V_{thb} denotes the threshold voltage with the body effect when the isolation switch M_i is off and its drain-to-substrate voltage is V_{dd}. Then, while ϕ_i is rising, X is boosted due to the capacitive coupling. Assume that X is boosted to the voltage higher than about $V_{dd} + V_{thb}$ so that the output follows ϕ_i exactly without degradation. While ϕ_i is falling, X is discharged back to $V_{dd} - V_{thb}$.

When the input is falling, isolation switch M_i is turned on without nonadiabatic loss because its two terminals, both the input and X, are at $V_{dd} - V_{thb}$. Note that the input must nest ϕ_i fully without any edge overlapping in the bootstrapped switch, as shown in the clock timing in Fig. 2(b).

B. Energy Consumption in a Bootstrapped Switch

In Fig. 2(a), when the input is rising, the isolation switch is first in the linear region, in which it consumes adiabatic loss only. Then the isolation switch goes into the saturation region, where its V_{DS} becomes larger since its drain voltage increases but its source voltage remains near $V_{dd} - V_{thb}$. According to the simulation results, the energy consumption in saturation region, which does not depend on the clock transition time in the low-frequency region, is nonadiabatic. Futhermore, this nonadiabatic loss is substantially larger than the adiabatic loss consumed in the linear region. However, this nonadiabatic loss is substantially smaller than that in quasi-adiabatic circuits, which is negligible in the total energy consumed in an nRERL circuit in a low-frequency region. Therefore, its energy dissipation per cycle is represented as

$$E_{diss} = \frac{2R_{on}C_L}{T} C_L V_{dd}^2 + V_{dd} I_{leak} kT \tag{1}$$

where R_{on} is the turn-on resistance of the switch, C_L is the load capacitance, and I_{leak} is the leakage current. k is the number of phases that a large sub-threshold leakage current flows in a cycle, and T is the transition time of clocked power, which is the duration of a phase [6].

According to (1), there is a single optimal transition time, where the switch consumes the minimum energy because adiabatic and leakage losses are equal [5], [6]. Although (1) is valid only for a bootstrapped switch, the behavior of energy consumption in a complex nRERL circuit will be similar because the majority of an nRERL circuit consists of the bootstrapped switches.

The turn-on resistance of a switch is a function of V_{dd}. The turn-on resistance of a bootstrapped switch considering the body effect is approximated as

$$R_{on} \approx \frac{1}{\beta(\alpha m - 2\xi)V_{tho}} \tag{2}$$

where $\alpha = (1+b)/2$, $\beta = \mu_n C_n / L^2$, $\xi(m) = V_{thb}/V_{tho}$, $m = V_{dd}/V_{tho}$, L is the channel length, μ_n is the charge mobility, and C_n is the gate capacitance of the nMOS transistor. The boosting factor b is defined as $C_G/(C_G + C_X)$, where C_G is the gate capacitance of M_B and C_X is the capacitance to the ground of the node X. If the routing capacitance of the node X is negligible, C_X equals to C_D the diffusion capacitance of the isolation switch M_i.

With the optimal transition time derived in [6] and the turn-on resistance in (2), the minimal energy consumption is approximated as

$$E_{min} \approx \sqrt{\frac{8km^3 \overline{I}_{leak} C_L^2 V_{tho}^2}{\beta(\alpha m - 2\xi)}} \tag{3}$$

where $\overline{I}_{leak}$ is the average leakage current. The sub-threshold leakage current of an isolation switch is dominant in the nRERL circuits and its maximum leakage occurs when V_{GS} of the isolation switch is about V_{tho}. Therefore, we used its average value, $\overline{I}_{leak}$, for simplicity, which depends on the device technology. The energy-optimal supply voltage scaling can be obtained by solving $(\partial E_{min}/\partial m) = 0$ from (3). Then, for a given threshold voltage V_{tho} we find the energy-optimal supply voltage $V_{dd} = m_{opt} V_{tho}$, when

$$m_{opt} = \frac{3\xi}{\alpha + \xi'}. \tag{4}$$

Here, ξ' is the differentiation of ξ to m.

The turn-on resistance of a bootstrapped switch and its energy consumption per cycle are shown as a function of m in Fig. 3, which were obtained from the SPICE simulation and the derived equations. Here, we used the following parameters: $b = 0.84$, $\beta = 1.05$ mAV^{-2}, $\Phi = 0.65$ V, $\gamma = 0.5$ V$^{0.5}$, $C_L = 0.1$ pF, $\overline{I}_{leak} = 50$ pA, $k = 3$, and $V_{tho} = 0.74$ V. Note that the minimum of the energy consumption occurs when m is about 4.7 in both (4) and the simulation results. When m is below about 4.3, the energy consumption increases sharply because the bootstrapped switch is not turned on always during each clock transition, which increases its equivalent turn-on resistance substantially.

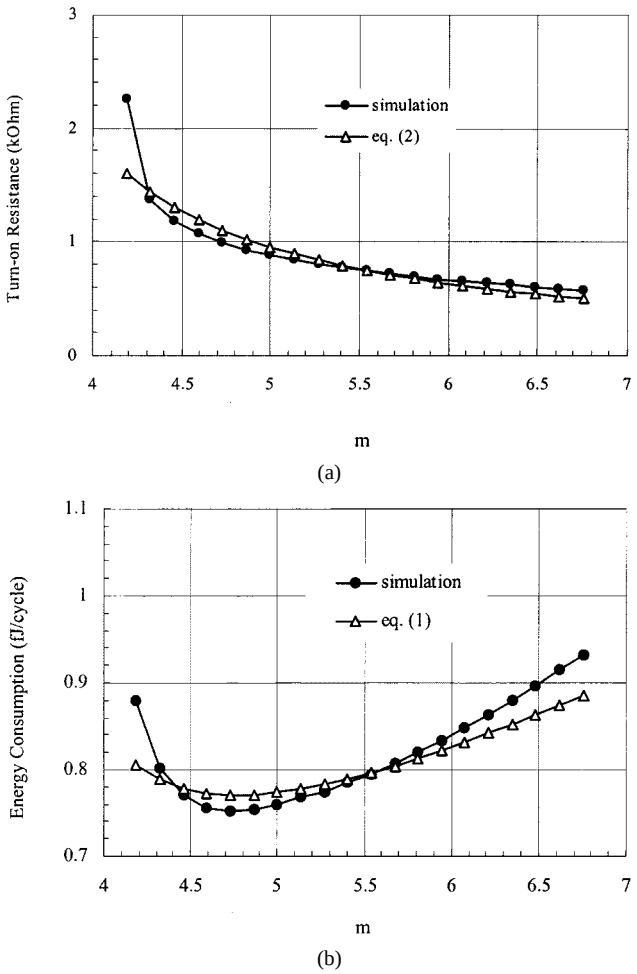


Fig. 3. (a) Turn-on resistance and (b) energy consumption in a bootstrapped nMOS switch. The operating frequency is 200 kHz, where adiabatic and leakage losses were about equal.

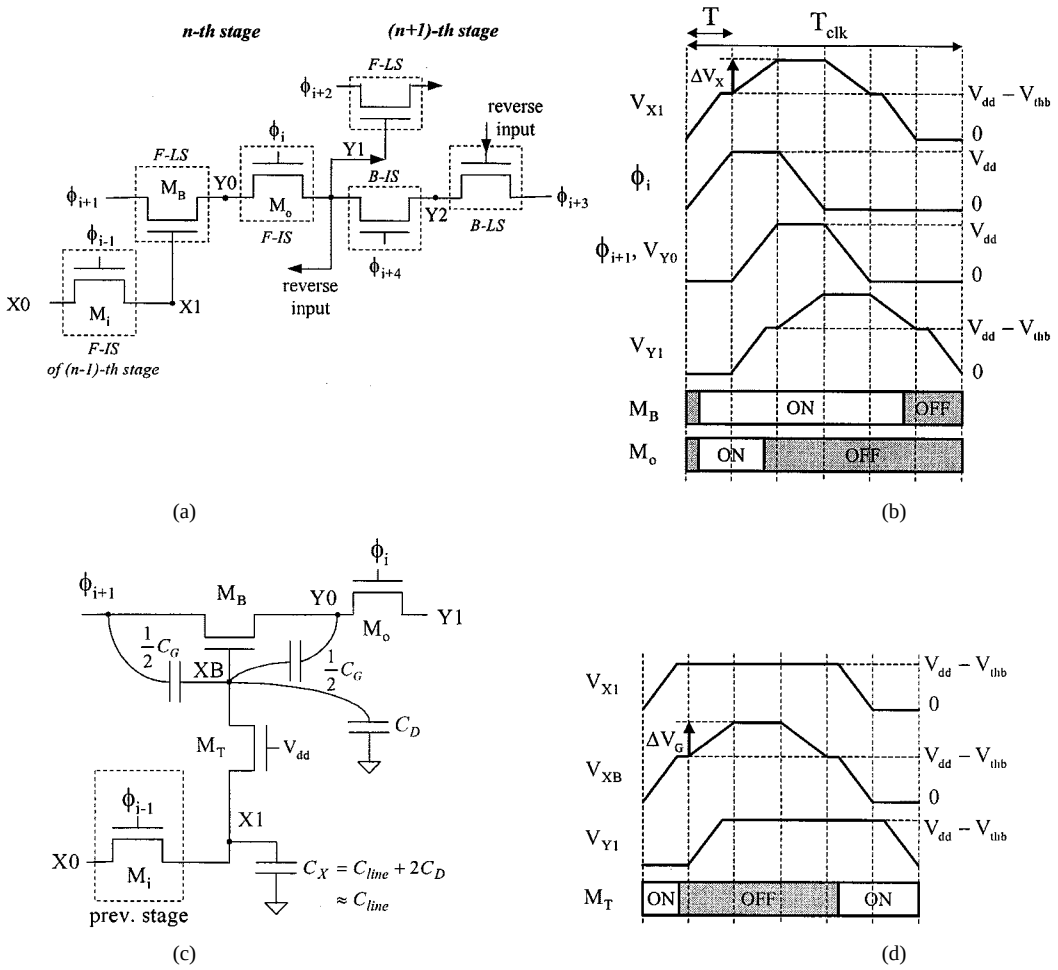


Fig. 4. (a) Bootstrapped switches used in nRERL. (b) Waveforms of the internal nodes and ON-OFF diagram for $\mathrm{M_B}$ and M_o. (c) A modified bootstrapped nMOS switch for large capacitance C_X. (d) The node waveforms of some internal nodes and the ON-OFF diagram of $\mathrm{M_T}$. The waveforms of the nodes omitted in (d) are equal to those in (b). In (a), $F-$, $B-$, LS, and IS are forward, backward, logic switch, and isolation switch, respectively.

C. Employing Bootstrapped Switches in nRERL

In the bootstrapped switch, the input must nest ϕ_i fully without any edge overlapping to eliminate any nonadiabatic losses, as shown in the clock timing in Fig. 2(b). This condition is often called the "retractile cascades" problem as it seriously limits the throughput of the circuit [13]. Therefore, we have to resolve the retractile cascades problem by using the proper clocking scheme as in other fully adiabatic circuits [3]–[6], [10].

In nRERL, this problem is solved with the 6-phase clocked power shown in Fig. 7(a). As shown in Fig. 4(a), the bootstrapped switch in nRERL is slightly different from that in Fig. 2(a). Two logic paths are required for each logic stage in nRERL: a forward logic path and its forward isolation switch for energy supply, and a backward logic path and its backward isolation switch for energy recovery. A pulse that nests the pulse of the clock that drives its logic switch was generated by connecting an appropriate clock phase to the gate of each isolation switch, as shown in Fig. 4(a). Consequently, we do not need to use the retractile cascades clocked power. However, we must use reversible logic to turn on the backward isolation switch without any nonadiabatic loss by making the node Y0 equal to the node Y1.

Energy supply to the output Y1 in Fig. 4(a) is as follows. When ϕ_{i+1} is rising, M_i is off because both its source and drain are high and its gate voltage is falling. Therefore, the node X1 is boosted above V_{dd}, and the node Y0 follows ϕ_{i+1} exactly but the node Y1 is charged to $V_{\mathrm{dd}} - V_{\mathrm{thb}}$. Y1 is boosted above V_{dd} when ϕ_{i+2} is rising. Although the gates of isolation transistors are not tied to V_{dd}, boosting is performed successfully, which is shown in Fig. 4(b).

When ϕ_{i+1} rises to V_{dd}, the voltage of X1 is boosted by ΔV_X $(=bV_{\mathrm{dd}})$, which is high enough to pass the clock waveform, only if the node X1 is high. Therefore, the full-swing condition of Y0 is that X1 must be boosted to at least one threshold voltage above V_{dd} from $V_{\mathrm{dd}} - V_{\mathrm{thb}}$ when X1 is high:

$$(V_{\mathrm{dd}} - V_{\mathrm{thb}}) + \Delta V_X > V_{\mathrm{dd}} + V_{\mathrm{thb}}. \tag{5}$$

Therefore

$$mb > 2\xi. \tag{6}$$

Note that ξ is a function of m. If the condition (6) is not satisfied, the energy consumption is drastically increased because the logic switch $\mathrm{M_B}$ is turned off so that its equivalent turn-on resistance becomes large and there exists a significant leakage current flow.

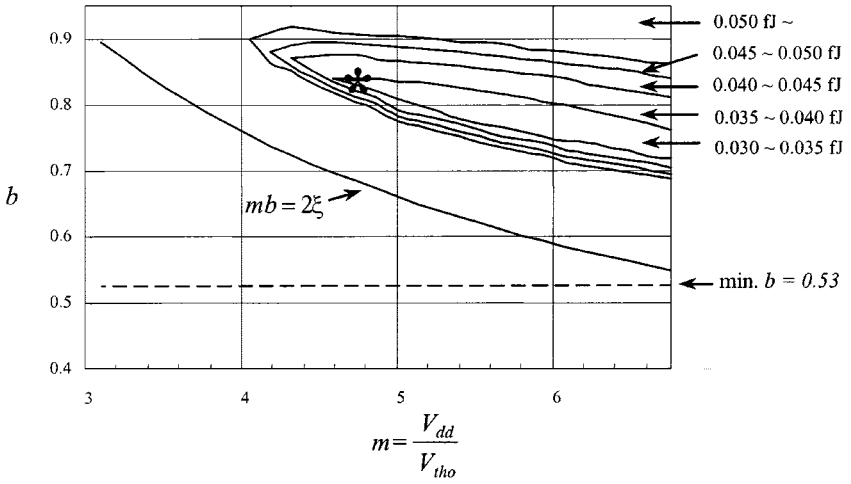


Fig. 5. Energy consumption in a bootstrapped switch when the supply voltage and the boosting factor are changed, which was obtained from the SPICE simulation. In the test chip, we used $V_{\rm dd}$ of 3.5 V and a bootstrapped switch with $\rm M_B$ of 6.0 μm/0.8 μm and M_i of 1.4 μm/0.8 μm, which corresponds the position of $m = 4.73$ and $b = 0.84$, which is marked with $\star$ in the figure.

When the fan-out of a logic stage is large or its wiring capacitance is large, the condition (6) cannot be satisfied easily for a given m because b gets smaller. To satisfy the full-swing condition, we can increase the boosting factor b by using a logic switch with wider width. However, it also increases the energy consumption in the previous stage because of its increased load capacitance. We can solve this problem easily by inserting a small nMOS transistor $\rm M_T$ as an additional isolation switch, as shown in Fig. 4(c). Then, when ϕ_{i+1} rises, the gate of $\rm M_B$ can be boosted high enough because its capacitance to the ground is only the diffusion capacitance of $\rm M_T$. The node waveforms and ON-OFF diagram of this switch are illustrated in Fig. 4(d).

We should properly size the three nMOS transistors, $\rm M_B$, $\rm M_o$, and $\rm M_T$, to optimize its energy consumption for a given technology. Fig. 5 shows the energy consumption in a bootstrapped switch when the supply voltage and the boosting factor are scaled. In this simulation, the minimum size of 1.4 μm/0.8 μm was used for both $\rm M_T$ and M_o, and the boosting factor was changed with the width of $\rm M_B$. The load capacitance of the bootstrapped switch was equal to twice the gate capacitance of $\rm M_B$. In Fig. 5, the dashed line of "min. b" implies the case when the minimum-sized transistor is used for $\rm M_B$, which is determined by the given technology. Note that the minimal-energy consumption is obtained only in the region that satisfies the full-swing condition in this simulation, as shown in Fig. 5.

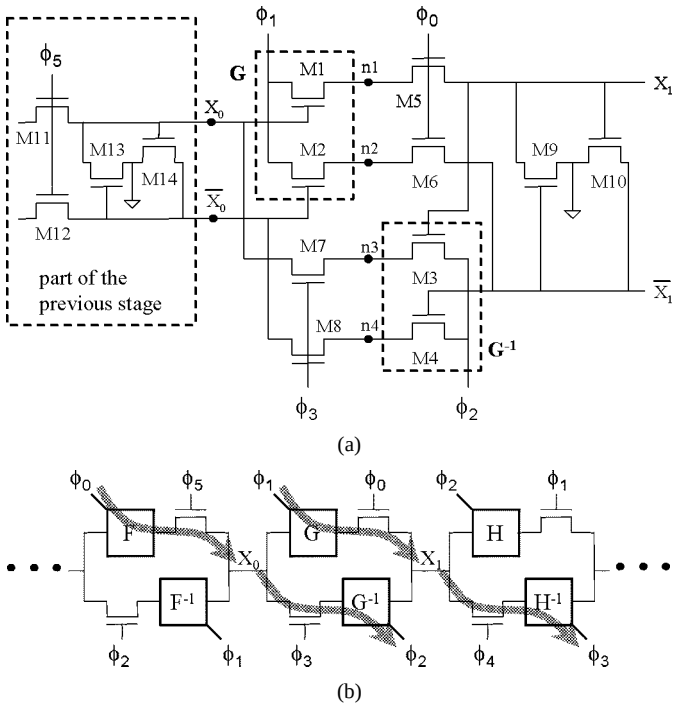


Fig. 6. nRERL. (a) Buffer. (b) Pipeline connection and energy-flow. F, G, and H are forward functions of each logic stage, and F^{-1}, G^{-1}, and H^{-1} are their backward functions, respectively.

III. nRERL

A. Operation

An nRERL buffer is in Fig. 6(a), and its 6-phase clock is in Fig. 7(a). The bootstrapped switches M1 and M2 (M3 and M4) compose a forward (backward) logic function, which determines a charging (discharging) path to one of the output nodes. The nMOS switches M5 and M6 (M7 and M8) are forward (backward) isolation switches, which isolate charging (discharging) paths from the outputs. The clamp transistors M9 and M10 make an undriven output node grounded. The waveforms of all the nodes in an nRERL buffer for an input sequence "11" are in Fig. 7(b). Here, we assume that the bootstrapped switches satisfy the full swing condition. They do not have any abrupt voltage drop so that there is no nonadiabatic loss. Reversible pipelining connection and energy-flow of nRERL are shown in Fig. 6(b). Each gray arrow indicates the energy-flow. The subscript of each signal indicates that when its corresponding clock phase is rising, the energy is supplied to the signal. For example, the rising ϕ_1 supplies the energy to X_1, whereas the falling ϕ_3 recovers the energy of X_1.

The operation of an nRERL buffer gate is as follows. Assume that initially all the internal nodes except clocks are grounded. During the time interval T_0, the input X_0 goes up to $V_{\rm dd} - V_{\rm thb}$, which is driven through the forward isolation switch M11

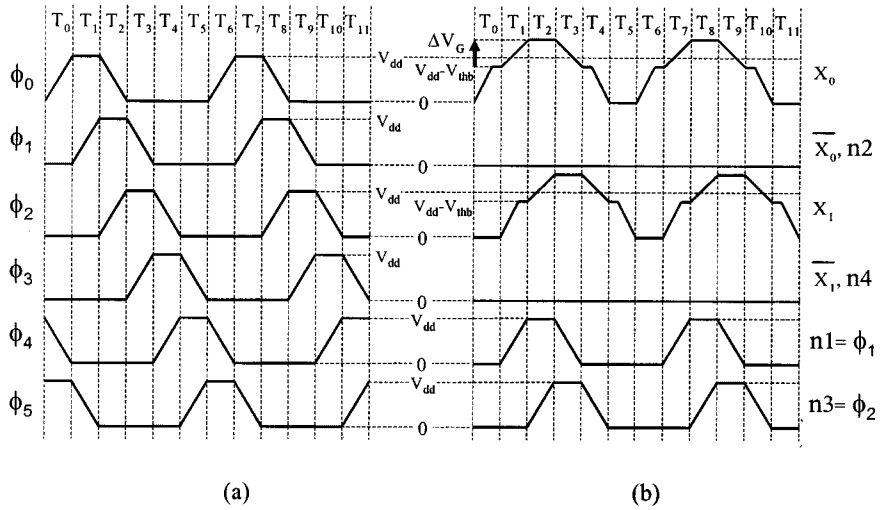


Fig. 7. Waveforms of (a) the 6-phase clocked power and (b) all the nodes in the buffer in Fig. 6(a).

in the previous stage. At the end of T_0, M1 is on, M11 is off and M2 remains off. In addition, the forward isolation switches M5 and M6 are on. During T_1, both X_1 and n1 become high because ϕ_1 is rising and both M1 and M5 are on. However, both $\bar{X}_1$ and n2 are driven to ground because M2 is off and the clamp device M10 is on. During this interval, n1 rises to $V_{\rm dd}$ without any signal degradation because X_0 is boosted to higher than $V_{\rm dd} + V_{\rm thb}$ while ϕ_1 is rising, which is the full-swing condition. However, X_1 is limited to $V_{\rm dd} - V_{\rm thb}$ due to the isolation transistor M5. During T_2, n3 rises to $V_{\rm dd}$ because X_1 is boosted while ϕ_2 is rising, and n4 is still at ground because M4 is off. Besides, M5 and M6 are turned off because ϕ_0 is falling to isolate the outputs from the forward logic switches.

During T_3, the falling ϕ_1 discharges n1 to ground because M1 is still on, and makes the voltage of X_0 return to $V_{\rm dd} - V_{\rm thb}$ due to the negative boosting effect of the falling ϕ_1. Note that even though ϕ_3 is rising to $V_{\rm dd}$, M7 is still off because its source and drain voltages are not less than $V_{\rm dd} - V_{\rm thb}$. During T_4, n3 is discharged when ϕ_2 is falling because M3 is on, then M7 is also turned on when n3 falls below $V_{\rm dd} - V_{\rm thb}$. There is no nonadiabatic loss in M7 because the voltages of n3 and X_0 are equal when M7 is turned on. After M7 is turned on, X_0 follows the falling ϕ_2. At the same time, the voltage of X_1 returns to $V_{\rm dd} - V_{\rm thb}$ due to the negative boosting effect of the falling ϕ_2. During T_5, the reverse isolation switches M7 and M8 are turned off to isolate both the grounded inputs from the reverse logic switches and to repeat six steps. Consequently, for a 6-phase cycle there is no nonadiabatic charging or discharging loss at any node, including the internal nodes (n1–n4), as shown in Fig. 7(b), because the voltage difference between the two terminals of a switch is always zero when it is turned on. However, the gate voltage of an isolation switch is ramped up from 0 to $V_{\rm dd}$ when the voltage difference between the drain and source is nonzero (its drain and source voltage are $V_{\rm dd}$ and $V_{\rm dd} - V_{\rm thb}$, respectively). In this case, the isolation transistor is still off while its gate voltage is rising. It is turned on when its drain voltage is falling below $V_{\rm dd} - V_{\rm thb}$.

There is no trap charge in the intermediate nodes in the nRERL circuit such as that in Fig. 9. All the charges of the internal nodes between the clock source and the output are recovered back to the clock source after the isolation switch disconnects the intermediate node from the output. It is because the inputs of a logic network are not changed at all until the clock, which supplies the energy to the output node while rising, is falling.

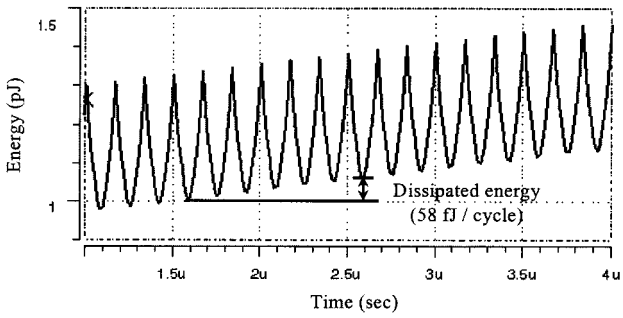


Fig. 8. Energy curve for a chain of six nRERL inverters obtained from SPICE simulation. The operating frequency is 1.0 MHz and $V_{\rm dd} = 5$ V.

In Fig. 6(a), if a minimum-sized transistor is used for each logic switch, the boosting factor may not be high enough because of the clamp transistors. This problem can be addressed using either of the methods of Section II.C. An alternative solution is to utilize two pairs of clamp transistors instead of one at the output: one in the forward path and the other in the backward path. For example, a pair of clamp transistors is connected between n1 and n2 and another pair between n3 and n4.

B. Reversible Logic

The energy dissipation curve in Fig. 8 was obtained with SPICE simulation for a chain of six buffers. The clocked power gives energy to the circuit and takes the energy back repeatedly, as shown in Fig. 8. Although the nRERL buffer shown in Fig. 6(a) is basically reversible, most of the Boolean gates are not reversible. To recover the signal energy delivered through a forward logic path, we must construct its corresponding backward logic path, which is possible only for the reversible logic. Therefore, we must convert each Boolean logic function to a

TABLE I
TRUTH TABLES OF A 2-INPUT REVERSIBLE XOR GATE. (a) FORWARD TRUTH TABLE ($Z = X$ XOR Y) (b) REVERSE TRUTH TABLE ($Y_2 = X_1$ XOR Z). X_1 AND X_2 ARE DELAYED COPIES OF X AND Y_2 IS A DELAYED COPY OF Y

Forward input		XOR	
X	Y	X_1	Z
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

(a)

Backward input		XOR^{-1}	
X_1	Z	X_2	Y_2
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

(b)

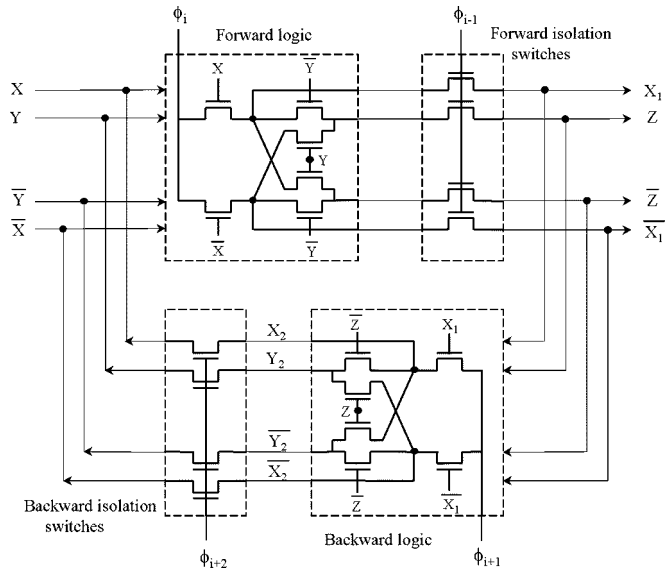


Fig. 9. Two-input reversible XOR gate and its reverse one. X_1 and X_2 are delayed copies of X. Y_2 is a delayed copy of Y. The clamp devices are omitted.

reversible one. In reversible logic, input-to-output mapping is always one-to-one. Fortunately, we can make any Boolean function reversible by adding some "garbage" information [14]. For example, truth tables of a 2-input reversible XOR gate are shown in Table I. X_1 and X_2, which are delayed copies of X, are garbage, and Y_2 is a delayed copy of Y.

The true and complementary logic networks in a complex nRERL gate can be easily implemented with nMOS networks just like those in the cascode voltage switch logic (CVSL). For example, a 2-input reversible XOR gate and its reverse one are

TABLE II
NUMBER OF TRANSISTORS IN A FULL ADDER FOR THE STATIC CMOS CIRCUIT AND FOUR ADIABATIC LOGIC CIRCUITS

	# of nMOSs / pMOSs	# of tr's normalized to CMOS	# of required clock rails
Static CMOS	14 / 14	1	1
2N-2N2P [2]	37 / 10	1.68	4
SCRL [3]	35 / 35	2.50	24
tRERL [4 - 6]	61 / 53	4.07	8
nRERL	61 / 0	2.18	6

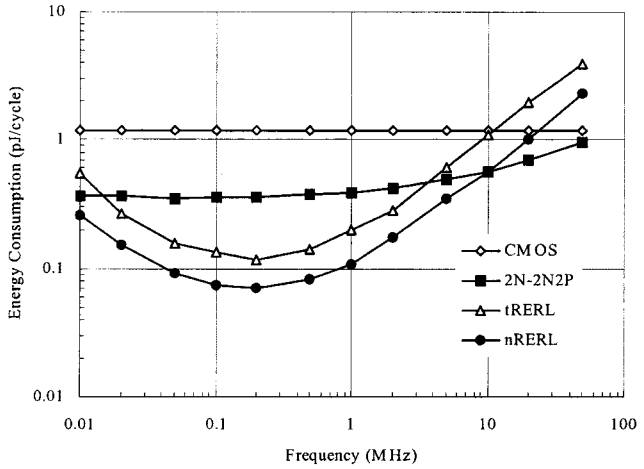


Fig. 10. Energy consumption in a full adder for the static CMOS circuit and three adiabatic circuits. These data were obtained from SPICE simulation.

implemented with nMOS network as shown in Fig. 9. In a complex nRERL gate, the time constant of the signal path increases rapidly. Therefore, its adiabatic loss increases sharply, which is proportional to the product of the time constant and the load capacitance. If the load capacitance is large, we can reduce energy dissipation by using simpler gates instead of complex gates.

As a logic function becomes complex, the circuit overhead required to keep reversibility is large. First, more garbage will be required to make a complex logic function reversible in general. Second, each garbage bit in a complex logic function must be kept until it is not required to recover the energy of other nodes. It is because we partition a complex logic function into several simpler ones and combine them via parallelism and cascading. Furthermore, it is not obvious how to minimize the garbage information in a complex reversible logic.

To reduce the overhead of reversible logic, we propose to break the reversibility of the circuit [5] by using an irreversible function and a self-energy-recovering circuit (SERC) to recover the energy supplied to a node, which is an input to the irreversible function. The circuit overhead due to the garbage information can be reduced with the SERC. Therefore, we can reduce the complexity of reversible logic by using the SERC without increasing energy consumption if the nonadiabatic loss in the SERC is less than the energy saved from the reduction in circuit overhead resulting from using the SERC. However, if

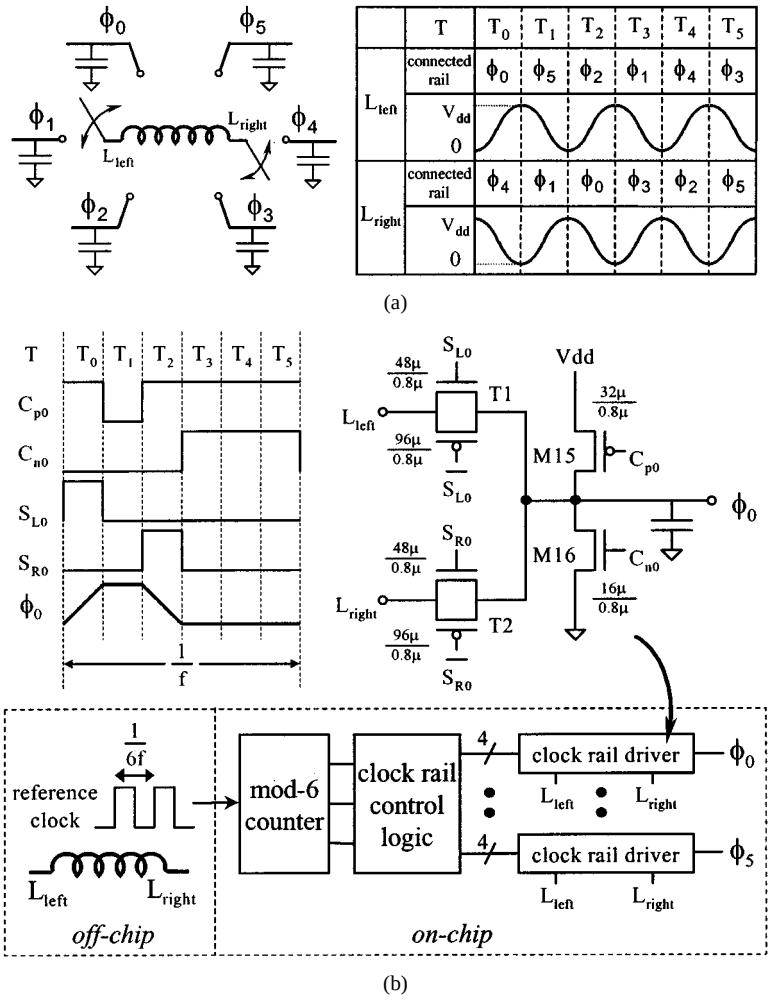


Fig. 11. (a) Switching order that indicates how the inductor terminals are connected to two out of six clock rails. (b) Clocked power generator and its control signals.

the operating speed is lower, the advantage of using the SERC is diminished.

C. Comparison with Other Logic Circuits

The circuit complexity of four adiabatic logic circuits and a static CMOS logic circuit was compared for a full adder (Table II). Both the number of transistors and the area in an nRERL full adder are about twice those in a static CMOS full adder. The number of clock rails required in nRERL is the minimum among the fully adiabatic circuits.

The energy consumption of the full adder was also compared for static CMOS logic, nRERL, tRERL [4]–[6], and 2N-2N2P [2] when the supply voltage is 5 V, as shown in Fig. 10. For all transistors in all the circuits, only the minimum-sized transistor of 1.4 μm/0.8 μm was used except for nRERL's bootstrapped switch, $\mathrm{M_B}$, which requires a size of 3.2 μm/0.8 μm in order to satisfy the full-swing condition. The minimum energy dissipated in the nRERL full adder was about 50% of that in the tRERL as both the turn-on resistance of a bootstrapped switch and the load capacitance were reduced in the nRERL circuit. The area of an nRERL full adder was about 60% less than that of the tRERL one.

IV. Clocked Power Generator

The 6-phase clocked power was generated with a small control logic circuit and an off-chip inductor. The clocked power generator (CPG) was efficient in energy consumption because the inductor connection is changed only when the inductor current is zero [5], [6]. Fig. 11(a) illustrates how the two nodes of an inductor are connected to two out of six clock rails, which is repeated in every six steps. Assume that initially L_{left} is at the ground state and L_{right} is at V_{dd}. During T_0, L_{left} and L_{right} are connected to ϕ_0 and ϕ_4, respectively, and then ϕ_0 swings from ground to V_{dd} and ϕ_4 swings from V_{dd} to ground simultaneously. During T_1, L_{left} and L_{right} are connected to ϕ_5 and ϕ_1, respectively, and ϕ_0 and ϕ_4 are clamped to V_{dd} and ground, respectively, to make their states truly high or low. Each unconnected clock rail is clamped to its own state.

The block diagram of the clocked power generator is shown in Fig. 11(b). Note that the frequency of the reference clock must be six times that of the generated 6-phase clock. A clock rail driver connects its corresponding clock rail to either terminal of the inductor via transmission gates T1 and T2 or clamps the rail to V_{dd} or ground via M15 or M16, respectively. Its control signals were generated with a mod-6 counter. The rail driver for ϕ_0 is also illustrated in Fig. 11(b).

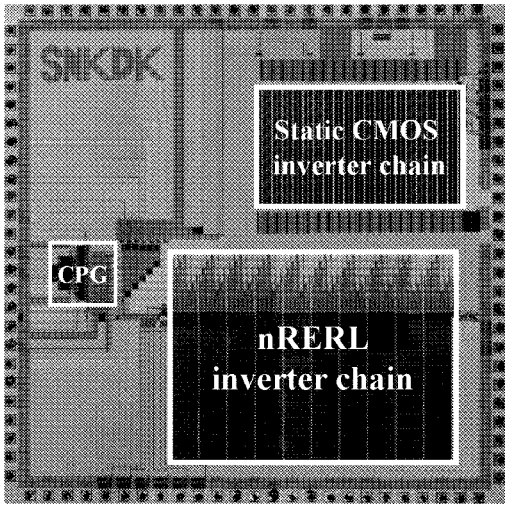


Fig. 12. Photomicrograph of the test chip.

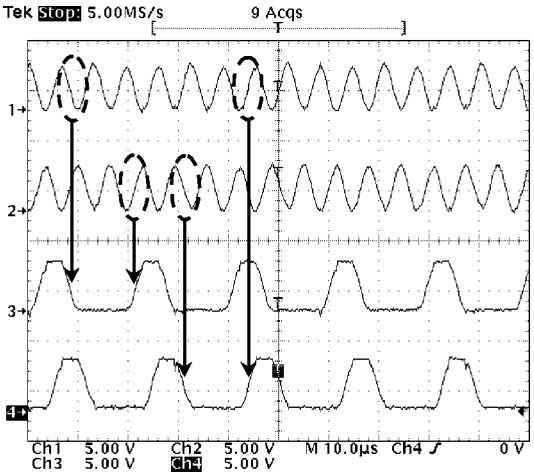


Fig. 13. Clock signal waveforms. Ch1: $L_{\rm left}$. Ch2: $L_{\rm right}$. Ch3: ϕ_1. Ch4: ϕ_2.

The CPG is divided into two parts: the rail drivers that change the inductor connection and the controller that generates the control signals of the rail drivers. The rail drivers consist of 12 transmission gates including T1 and T2 in Fig. 11(b), and their energy consumption is adiabatic. The controller was implemented using static CMOS circuits, and its energy consumption is nonadiabatic.

V. Experimental Results and Discussions

A test chip was fabricated with 0.8-μm double-metal n-well CMOS technology, which included a 2400-stage nRERL pipelined inverter chain with a CPG. The pipelined inverter chain is the same as a shift register because nRERL is dual-railed and micro-pipelined. The threshold voltages of nMOS and pMOS transistors are 0.74 and $-$0.90 V, respectively. Energy dissipation in the nRERL inverter chain and that in the CPG can be measured separately in the test chip. A static CMOS 2400-stage inverter chain is also included in the test chip to allow fair comparison. In the static CMOS inverter chain, a flip-flop is inserted at every six stages, which is required for synchronous operation. Inserting a flip-flop every six inverters is an arbitrary choice of ours. Therefore, energy dissipation in the static CMOS inverter chain and that in the pipeline flip-flops can also be measured separately to eliminate the effect of this arbitrariness.

Only minimum-sized devices ($W/L = 1.4\,\mu$m$/0.8\,\mu$m) were used for both nMOS and pMOS transistors in all circuits, except for the bootstrapped switch transistors and the transistors of the rail drivers in the CPG. The size of the bootstrapped switch transistor was $W/L = 6.0\ \mu$m$/0.8\ \mu$m, which was optimized for correct operation and minimal-energy dissipation at $V_{\rm dd} = 3.5$ V. These are shown in Fig. 5. The transistors in the rail drivers in the CPG are shown in Fig. 11. Fig. 12 shows a photomicrograph of the test chip. The areas of the nRERL inverter chain, the CPG, and the static CMOS inverter chain are 2.7×2.0 mm^2, 0.35×0.53 mm^2, and 2.0×1.4 mm^2, respectively. The area of the nRERL is approximately 1.9 times that for the inverter chain, excluding that of the CPG.

The measured waveforms of two clock rails generated with the clocked power generator are shown in Fig. 13. We confirmed the correct operation of the CPG only up to 5 MHz, with the reference clock of 30 MHz, which is the highest frequency that can be generated from our equipment. However, according to the SPICE simulation the maximum operating frequency was about 80 MHz with its corresponding reference clock of 480 MHz.

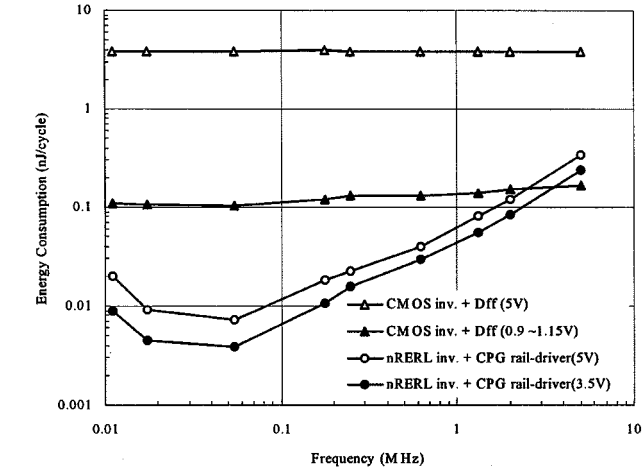
The measured data of energy dissipated in the 2400-stage inverter chain are shown in Fig. 14. In Fig. 14(a) and (b), the energy consumed of the CPG controller has been excluded. This loss, which is nonadiabatic loss, does not depend on either the operating frequency or complexity of the nRERL circuit. The energy dissipation of each circuit was measured at both $V_{\rm dd} = 5$ V and its optimized supply voltage. The theoretical lower limit of the supply voltage for the CMOS is 0.9, which was determined by the threshold voltage of the pMOS transistors. However, the optimized supply voltage of the static CMOS circuits for proper operation must be higher than 0.9 V if the operating frequency is higher than 1 MHz.

Energy consumption of the nRERL inverter chain with its CPG rail drivers was compared with that of the static CMOS inverter chain with synchronous flip-flops as a function of the operating frequency and supply voltage [Fig. 14(a)]. The input patterns were generated randomly. When the supply voltage of the two circuits was 5 V, the nRERL circuit consumed 0.19% of the dissipated energy of a static CMOS circuit at the optimal operating speed of 55 kHz. At very low operating frequencies, slower than 55 kHz, the consumed energy is increased because the leakage loss was dominant compared with the adiabatic loss. If the supply voltage of each circuit is optimized, the nRERL circuit consumed the minimum energy at $V_{\rm dd} = 3.5$ V at 55 kHz, which is 3.68% of the dissipated energy of a static CMOS circuit at $V_{\rm dd} = 0.9$ V.

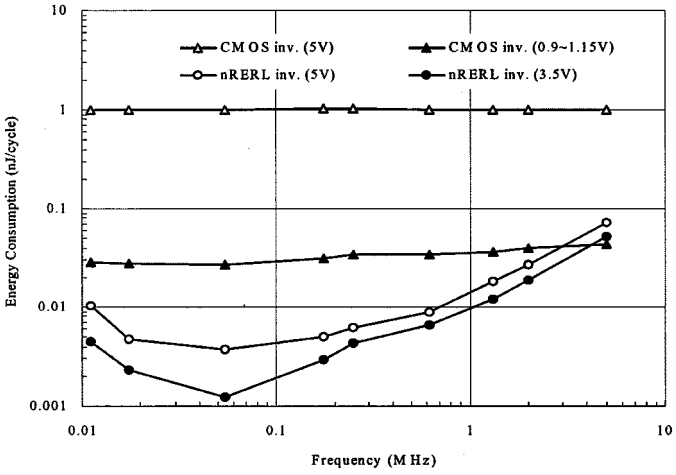
The energy consumption of the nRERL inverter chain was also measured excluding its CPG rail drivers, and then compared with that of the conventional CMOS inverter chain excluding flip-flops [Fig. 14(b)]. When $V_{\rm dd} = 5$ V, the nRERL circuit consumed 0.37% of the dissipated energy of a static CMOS circuit at 55 kHz. If the supply voltage of each circuit is optimized, the nRERL circuit consumed the minimum energy at $V_{\rm dd} = 3.5$ V

TABLE III
ENERGY CONSUMPTION OF THE INVERTER CHAINS MEASURED SEPARATELY FOR EACH COMPONENT AT THE OPTIMIZED SUPPLY VOLTAGE, WHICH IS SHOWN IN THE PARENTHESIS

Each circuit part \ Frequency		55 kHz	250 kHz	2 MHz
Static CMOS circuit	inverter chain	27.0 pJ/cycle (0.9 V)	33.8 pJ/cycle (1.0 V)	40.2 pJ/cycle (1.15 V)
	pipeline registers	76.5 pJ/cycle (0.9 V)	95.8 pJ/cycle (1.0 V)	113.9 pJ/cycle (1.15 V)
nRERL circuit	inverter chain	1.2 pJ/cycle (3.5 V)	4.3 pJ/cycle (3.5 V)	19.0 pJ/cycle (3.5 V)
	rail-drivers in CPG	2.6 pJ/cycle (3.5 V)	11.2 pJ/cycle (3.5 V)	64.9 pJ/cycle (3.5 V)
	controller in CPG	40.5 pJ/cycle (3.5 V)	40.5 pJ/cycle (3.5 V)	40.5 pJ/cycle (3.5 V)



(a)



(b)

Fig. 14. Energy consumption in a 2400-stage inverter chain for the static CMOS logic and the nRERL. (a) nRERL inverter chain with the CPG and the static CMOS inverter chain with pipeline registers. (b) nRERL inverter chain and static CMOS inverter chain. For each circuit, we measured it at $V_{\rm dd}$ of 5 V and its minimal-energy supply voltage, which was 3.5 V for nRERL and 0.9–1.15 V for the static CMOS logic. Energy consumed in the CPG for nRERL and that in the pipeline registers for the static CMOS logic were included in (a) but not in (b). Although the theoretical lower limit of the supply voltage for the CMOS is 0.9, which was determined by the threshold voltage of pMOS transistors, the minimum supply voltage for the static CMOS circuits must be higher than 0.9 V for proper operation if the operating frequency is higher than 1 MHz.

at 55 kHz, which is 4.50% of the dissipated energy of the CMOS version at $V_{\rm dd} = 0.9$ V.

The energy dissipated in the inverter chain and flip-flops was separately measured for the CMOS circuit at its optimal supply voltage. Similarly, the energy dissipation of the inverter chain, rail drivers, and the CPG controller separately for the nRERL inverter chain at its optimal supply voltage. The energy consumed in the CPG is compared with that in the nRERL inverter chain at three operating frequencies, as shown in Table III. The energy consumed in the CPG controller was 91.4% of the total energy dissipated in the nRERL circuit at 55 kHz as the complexity of the nRERL logic circuit was very low. However, this ratio is reduced substantially if the complexity of the nRERL circuit is higher. Therefore, more careful optimization of the CPG is required when the complexity of an nRERL logic circuit is lower. It is also important to reduce the power consumption in the controller part of the CPG, which is nonadiabatic loss, although it becomes less significant if the complexity of the nRERL circuit gets higher.

VI. CONCLUSION

We have introduced a new fully reversible adiabatic logic circuit, nRERL, with utilizing only nMOS transistors and a 6-phase clocked power, which achieves significant area savings by exploiting bootstrapped switches. We have explained how the bootstrapped switch is used to reduce nonadiabatic loss substantially and how its minimal-energy consumption is obtained by supply voltage scaling. We also described an energy-efficient CPG. However, it requires more careful optimization for the simpler nRERL circuits because of its nonadiabatic loss.

With simulations and evaluation of the test chip, we have confirmed that the proposed nRERL exhibits only adiabatic and leakage losses. A 2400-stage nRERL inverter chain consumed the minimum energy at $V_{\rm dd} = 3.5$ V at 55 kHz, where the adiabatic and leakage losses are about equal, which is only 4.50% of the dissipated energy of its corresponding CMOS circuit at $V_{\rm dd} = 0.9$ V.

In conclusion, nRERL is suitable for the energy-limited applications such as implanted devices because its energy consumption can be decreased down to the leakage-current level by reducing the operating frequency until adiabatic and leakage losses are equal. To make nRERL more competitive in the energy consumption, further research is required in how to reduce the leakage current and how to design a more efficient CPG. To this end, we are currently designing several complex circuits with nRERL such as a multiplier and a microprocessor.

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