NODE VOLTAGE DEPENDENT SUBTHRESHOLD LEAKAGE CURRENT CHARACTERISTICS OF DYNAMIC CIRCUITS

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Abstract – The subthreshold leakage current characteristics of domino logic circuits is evaluated in this paper. The strong dependence of the subthreshold leakage current on the node voltages is discussed. In a standard low threshold voltage domino logic circuit with stacked pull-down devices, a charged state rather than a discharge state of the dynamic node is preferred for lower leakage current. Alternatively, the subthreshold leakage current of a dual threshold voltage domino logic circuit is significantly reduced provided that the dynamic node is discharged.

A dual threshold voltage circuit has degraded noise immunity characteristics as compared to a standard low threshold voltage circuit. Both keeper and output inverter sizing are necessary to compensate for this degradation in noise immunity. An alternative dual threshold voltage domino circuit technique employing a low threshold voltage keeper for enhanced noise immunity is also considered in this paper. Under similar noise immunity conditions as compared to a standard low threshold voltage domino logic circuit, the savings in subthreshold leakage current offered by a dual threshold voltage circuit technique with a high threshold voltage keeper is significantly higher than the savings offered by a dual threshold voltage circuit technique with a low threshold voltage keeper.

1. INTRODUCTION

Subthreshold leakage power is expected to dominate the total power consumption of a CMOS circuit in the near future [1]-[8]. Energy efficient circuit techniques aimed at lowering leakage currents are, therefore, highly desirable. The dynamic node voltage dependent asymmetry of the subthreshold leakage current characteristics of dual threshold voltage domino gates was first noted by Kao [3]. Based on this asymmetry, several circuit techniques to place dual threshold voltage domino logic circuits into a low leakage state have been proposed in [3]-[6] and [9].

A quantitative study of the subthreshold leakage current characteristics of standard low threshold voltage (low-V_t) or dual threshold voltage (dual-V_t) domino logic circuits, however, has to date not been described in the literature. The node voltage dependent subthreshold leakage current characteristics of domino logic circuits are examined in this paper. The subthreshold leakage current of a domino logic circuit can vary dramatically with the voltage state of the dynamic and output nodes. Different subthreshold leakage current conduction paths which exist depending upon whether the dynamic node is charged or discharged are identified. It is shown that a discharged dynamic node is preferable for reducing leakage current in a dual-V_t circuit. Alternatively, a charged dynamic node is preferred for lower subthreshold leakage energy in a standard low-V_t domino logic circuit with stacked pull-down devices, such as an AND gate.

Noise immunity issues in dual-V_t domino logic circuits have been ignored in [3]. Provided that a dual-V_t CMOS technology is employed, the noise immunity of domino logic circuits can be significantly weakened, degrading reliability. A brief discussion of noise immunity related issues in dual-V_t domino circuits is provided in [4]. A dual-V_t domino logic circuit technique based on low-V_t keeper transistors is proposed to maintain a similar noise immunity as compared to standard low-V_t domino logic circuits [4].

A discussion of the effect of dual-V_t CMOS technologies on the noise immunity characteristics of domino logic circuits is provided in this paper. Two different dual-V_t domino logic circuit techniques to maintain similar noise immunity as compared to standard low-V_t circuits are evaluated. Both keeper and output inverter sizing is required in a dual-V_t domino logic circuit with a high threshold voltage (high-V_t) keeper transistor in order to provide similar noise immunity as compared to a standard low-V_t domino logic circuit. As an alternative technique, a dual-V_t circuit technique based on low-V_t keeper transistors is also considered in this paper. Under similar noise immunity conditions as compared to standard low-V_t domino logic circuits, the savings in subthreshold leakage energy offered by the dual-V_t circuit technique with a high-V_t keeper is 5.7 to 10.9 times higher as compared to the savings offered by the dual-V_t circuit technique with a low-V_t keeper.

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Under similar noise immunity conditions, the subthreshold leakage current of dual-V_t domino logic circuits with a high-V_t keeper at a low dynamic node voltage is 224 to 235 times smaller as compared to low-V_t domino logic circuits with a low dynamic node voltage. Alternatively, as compared to low-V_t domino logic circuits with a high dynamic node voltage, the subthreshold leakage current of dual-V_t domino logic circuits with a high-V_t keeper at a low dynamic node voltage is 89 to 3079 times smaller.

The node voltage state dependent subthreshold leakage current characteristics of various domino logic circuits is described in Section 2. The effect of a dual-V_t CMOS technology on the noise immunity characteristics of domino logic circuits is discussed in Section 3. The active mode delay and power dissipation of dual-V_t domino logic circuits are presented in Section 4. Some conclusions are offered in Section 5.

2. STATE DEPENDENT SUBTHRESHOLD LEAKAGE CURRENT CHARACTERISTICS

A dual-V_t domino logic circuit is shown in Fig. 1. The high-V_t transistors are represented in Fig. 1 by a thick line in the channel region. The critical signal transitions that determine the delay of a domino logic circuit occur along the evaluation path. In a dual-V_t domino circuit, therefore, all of the transistors that can be activated during the evaluation phase have a low-V_t. The precharge phase transitions are typically not critical for the speed of a domino logic circuit. In order to exploit the excessive slack of the precharge paths, those transistors that are active during the precharge phase have a high-V_t.

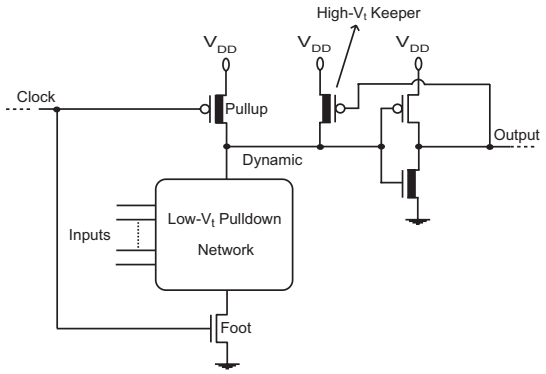

Fig. 1. A dual-V_t domino logic circuit.

The node voltage dependence of the subthreshold leakage current characteristics of various dual-V_t and low-V_t domino logic circuits is evaluated in this section, assuming a 0.18 µm CMOS technology ($V_{tnlow} = |V_{tplow}|$ = 200 mV, $V_{tnhigh} = |V_{tphigh}|$ = 500 mV, and T = 110°C). The variation of the subthreshold current conduction paths with the node voltages in a low-V_t and dual-V_t domino logic circuit are shown in Figs. 2 and 3, respectively.

Clock gating is an effective method for lowering the dynamic switching power in the unused portions of an integrated circuit. Moreover, when the clock is gated high, the pull-up transistor is turned off, ensuring that no short-circuit current conduction path exists between the power supply and ground (provided that the inputs are high). In this paper, therefore, it is assumed that the clock is gated high in an idle domino logic circuit. The dynamic node is cyclically charged every clock period. Therefore, provided that the inputs are low after the clocks are gated, the dynamic node is maintained high during the idle mode, as illustrated in Figs. 2a and 3a. Alternatively, provided that the inputs are high after the clocks are gated, the dynamic node is discharged through the pull-down network transistors and the output transitions high, as shown in Figs. 2b and 3b. The subthreshold leakage current of a domino logic circuit varies dramatically between these two different states of the dynamic and output nodes, as shown in Fig. 4.

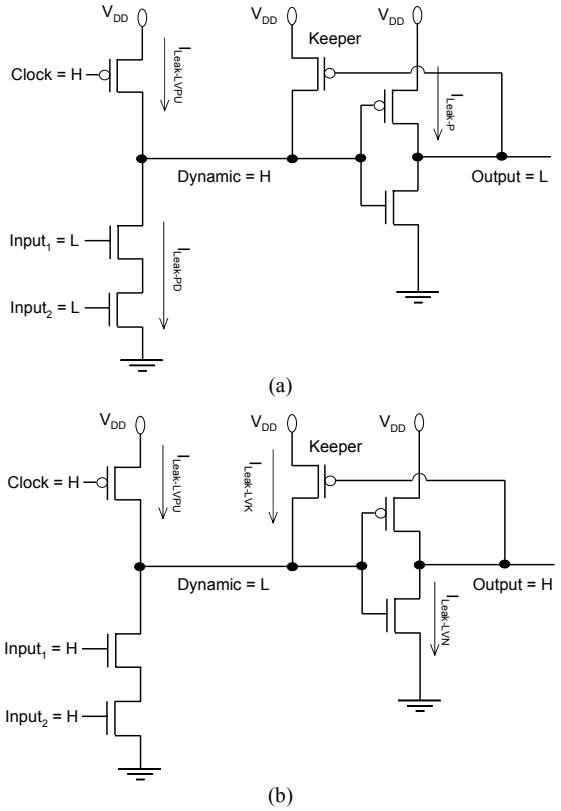

Fig. 2. Variation of the subthreshold leakage current conduction paths with the state of the dynamic and output nodes in a two input standard low-V_t domino AND gate. (a) High (H) dynamic node voltage state. (b) Low (L) dynamic node voltage state. LVK: Low-V_t keeper transistor. LVPU: Low-V_t pull-up transistor. LVN: Low-V_t NMOS transistor.

When the dynamic node is high (the inputs are low), the total subthreshold leakage current of a domino gate is

$$I_{subthreshold-H} = I_{Leak-PD} + I_{Leak-P}, \qquad (1)$$

where $I_{Leak\text{-}PD}$ and $I_{Leak\text{-}P}$ are the subthreshold leakage currents through the low-V_t pull-down and output inverter pull-up transistors, respectively. Alternatively, when the dynamic node is low (the inputs are high), the total subthreshold leakage current of a low-V_t domino gate is

$$I_{subthreshold-L} = I_{Leak-LVPU} + I_{Leak-LVK} + I_{Leak-LVN}, \quad (2)$$

where $I_{Leak\text{-}LVPU}$, $I_{Leak\text{-}LVK}$, and $I_{Leak\text{-}LVN}$ are the subthreshold leakage currents through the low-V_t pull-up, keeper, and output inverter pull-down transistors, respectively.

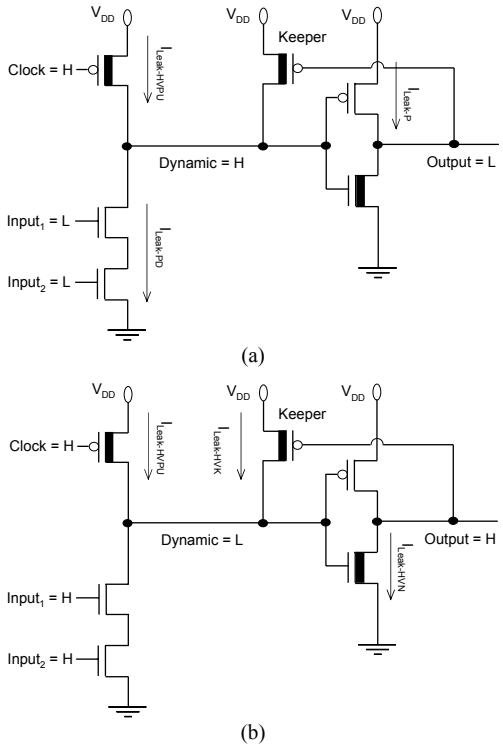

Fig. 3. Variation of the subthreshold leakage current conduction paths with the node voltages in a two input dual-V_t domino AND gate. (a) High (H) dynamic node voltage. (b) Low (L) dynamic node voltage. HVK: High-V_t keeper transistor. HVPU: High-V_t pull-up transistor. HVN: High-V_t NMOS transistor.

The subthreshold leakage current through a stack of transistors is orders of magnitude smaller than the subthreshold leakage current through a single transistor [7]. When the inputs are low (the dynamic node is high), $I_{leak\text{-}PD}$ decreases as more stacked devices are added to the pull-down network. Similarly, as the number of parallel pull-down paths is reduced, I_{leak_PD} decreases. Alternatively, when the inputs are high (the dynamic node is low), the subthreshold leakage current through the pull-up transistor increases as more stacked devices or parallel discharge paths are added to the pull-down network (due to the increasing width of the pull-up transistor required to drive the increased parasitic capacitance at the dynamic node). $I_{subthreshold\text{-}L}$ is higher than $I_{subthreshold\text{-}H}$ for a two input low-V_t AND gate. As more stacked devices are added to an AND gate, $I_{subthreshold\text{-}H}$ decreases while $I_{subthreshold\text{-}L}$ further increases. For a low-V_t domino AND gate, therefore, a high dynamic node voltage is preferred for producing a lower subthreshold leakage current. Alternatively, $I_{subthreshold\text{-}H}$ is higher than $I_{subthreshold\text{-}L}$ for a two input OR gate. As more parallel discharge paths are added to the pull-down network, both $I_{subthreshold\text{-}H}$ and $I_{subthreshold\text{-}L}$ increase. Since the increase in $I_{subthreshold\text{-}L}$ is smaller than the increase in $I_{subthreshold\text{-}H}$, a low dynamic node voltage is preferred for reduced subthreshold leakage current in wide fan-in OR types of gates.

As shown in Fig. 4, a low dynamic node voltage state produces a 2.8 to 13.2 times smaller subthreshold leakage current as compared to a high dynamic node voltage state in a low-V_t domino circuit with parallel pull-down network paths, such as two, four, and eight input OR gates and a 16-bit multiplexer. Alternatively, in low-V_t domino logic circuits with stacked pull-down network transistors, such as two, four, six, and eight input AND gates, a low dynamic node voltage state produces a 13.3% (AND2) to 153% (AND8) higher subthreshold leakage current as compared to a high dynamic node voltage state.

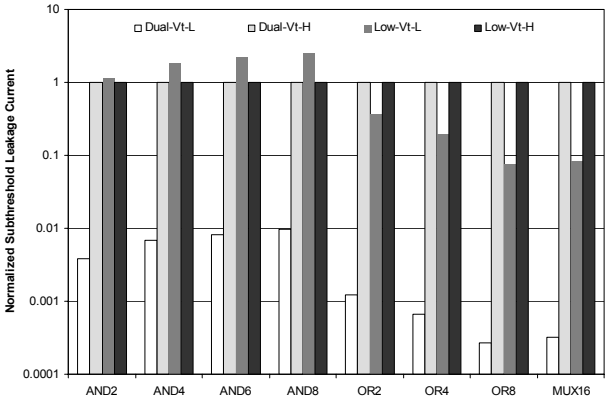

Fig. 4. Comparison of the subthreshold leakage current of low-V_t and dual-V_t domino logic circuits for the two states of the dynamic node. The leakage current of each gate is normalized to the leakage current of the corresponding low-V_t gate with a high (H) dynamic node voltage. L: low dynamic node voltage. AND2, AND4, AND6, and AND8: 2, 4, 6, and 8 input, respectively, domino AND gates. OR2, OR4, and OR8: 2, 4, and 8 input, respectively, domino OR gates. MUX16: 16-bit domino multiplexer.

While the subthreshold leakage current characteristics of low-V_t and dual-V_t circuits are similar for a high dynamic node voltage state, the subthreshold leakage current characteristics of the two circuit techniques are dramatically different for a low dynamic node voltage state. When the inputs are high and the dynamic node is low, the total subthreshold leakage current of a dual-V_t domino gate is

$$I_{subthreshold-L} = I_{Leak-HVPU} + I_{Leak-HVK} + I_{Leak-HVN}, \quad (3)$$

where $I_{Leak\text{-}HVPU}$, $I_{Leak\text{-}HVK}$, and $I_{Leak\text{-}HVN}$ are the subthreshold leakage currents through the high-V_t pull-up, keeper, and output inverter NMOS pull-down transistors, respectively. $I_{Leak\text{-}HVPU}$, $I_{Leak\text{-}HVK}$, and $I_{Leak\text{-}HVN}$ are orders of magnitude smaller than $I_{Leak\text{-}LVPU}$, $I_{Leak\text{-}LVK}$, and $I_{Leak\text{-}LVN}$, respectively. Therefore, provided that the dynamic node is discharged in a domino logic circuit, the subthreshold leakage current can be significantly reduced by employing a dual-V_t CMOS technology, as shown in Fig. 3. The subthreshold leakage current of dual-V_t domino logic circuits with a low dynamic node voltage is 257 (MUX16) to 293 times (AND2, OR2, and OR4) smaller as compared to low-V_t domino logic circuits with a low dynamic node voltage. Alternatively, as compared to low-V_t domino logic circuits with a high dynamic node voltage, the subthreshold leakage current of dual-V_t domino logic circuits with a low dynamic node voltage is 103 (AND8) to 3719 times (OR8) smaller.

3. NOISE IMMUNITY

The noise immunity of low-V_t and dual-V_t domino logic circuits is evaluated in this section. The noise immunity criterion used in this paper is similar to the criterion described in [8]. The noise margin is the voltage amplitude of the DC noise signal applied to the inputs that produces a signal with the same amplitude at the output of a domino logic circuit, assuming a 1 GHz clock with a 50% duty cycle.

The degradation in noise immunity due to employing dual-V_t transistors is illustrated in Fig. 5. The drain current of a high-V_t keeper transistor is reduced as compared to a low-V_t keeper transistor with the same physical size. A dual-V_t domino logic circuit with a high-V_t keeper transistor, therefore, has lower noise immunity as compared to a standard low threshold voltage domino logic circuit. As illustrated in Fig. 5, the noise immunity of a dual-V_t domino logic circuit with a high-V_t keeper transistor (HVK) is reduced by 10% (MUX16) to 12.6% (AND2 and OR2) as compared to a low-V_t domino logic circuit with the same size transistors.

The degradation in the noise immunity characteristics in a dual-V_t circuit can be compensated by employing a low-V_t keeper transistor rather than a high-V_t keeper transistor. The noise immunity characteristics of dual-V_t domino logic circuits with a low-V_t keeper transistor (LVK) are illustrated in Fig. 5. Replacing a high-V_t keeper transistor with a low-V_t keeper transistor, as shown in Fig. 5, is not sufficient to fully compensate for the noise immunity degradation of a dual-V_t domino logic circuit. The noise immunity depends not only on the physical size and threshold voltage of the keeper transistor but also on the gain of the output inverter. Since the low-V_t NMOS pull-down transistor inside the output inverter of a low-V_t domino logic circuit is replaced by a high-V_t transistor in a dual-V_t domino logic circuit (see Fig. 3), the high-to-low gain of the output inverter is reduced, further degrading the noise immunity. The noise immunity of a dual-V_t domino logic circuit with a low-V_t keeper transistor is 3.8% (AND4) to 6.3% (MUX16) lower as compared to a low-V_t domino logic circuit with the same size transistors, as shown in Fig. 5.

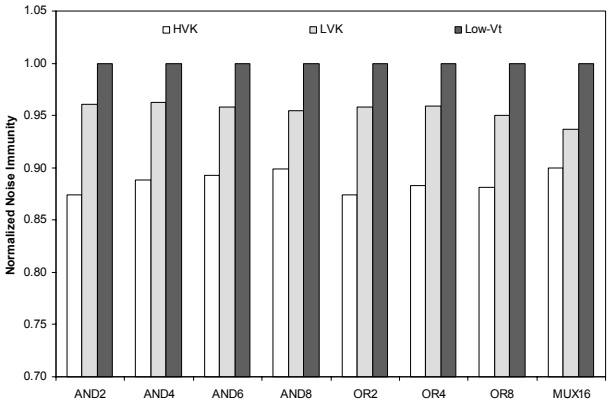

Fig. 5. Comparison of the noise immunity of low-V_t and dual-V_t domino logic circuits with the same size transistors. The noise margin of each gate is normalized to the noise margin of the corresponding low-V_t gate. HVK: high-V_t keeper. LVK: low-V_t keeper.

One circuit technique for maintaining the same noise immunity as compared to a low-V_t circuit is to employ a low-V_t keeper while increasing the size of the high-V_t pull-down transistor within the output inverter, thereby enhancing the high-to-low output gain and noise immunity. Another circuit technique to compensate the degradation in noise immunity is to increase the width of the high-V_t keeper and the high-V_t NMOS pull-down transistor within the output inverter. In this paper, both techniques are applied to domino logic circuits to enhance noise immunity. A comparison of the subthreshold leakage current characteristics of dual-V_t domino with a high-V_t keeper (dual-V_t-HVK), dual-V_t domino with a low-V_t keeper (dual-V_t-LVK), and low-V_t domino logic circuit techniques while providing similar noise immunity characteristics is shown in Fig. 6.

Increasing the physical size of the keeper and the pull-down transistor within the output inverter increases both $I_{Leak\text{-}HVK}$ and $I_{Leak\text{-}HVN}$, thereby degrading the reduction in subthreshold leakage current achieved at a low dynamic node voltage state. As shown in Fig. 6, under similar noise immunity conditions, the subthreshold leakage current of dual-V_t domino logic circuits with a high-V_t keeper and a low dynamic node voltage is 224 (AND8) to 235 times (MUX16) smaller as compared to low-V_t domino logic circuits with a low dynamic node voltage. Alternatively, as compared to low-V_t domino logic circuits with a high dynamic node voltage, the subthreshold leakage current of dual-V_t domino logic

circuits with a high-V_t keeper and a low dynamic node voltage is 89 (AND8) to 3079 times (OR8) smaller.

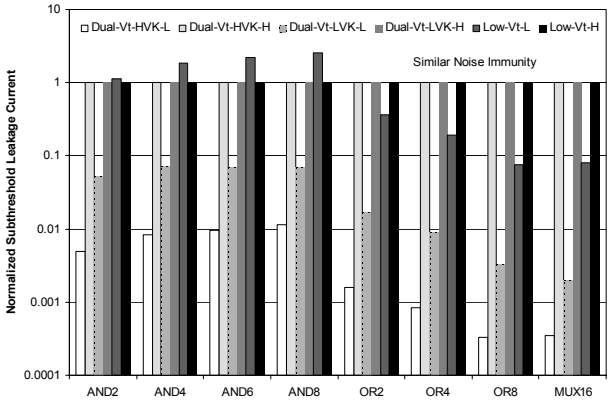

Fig. 6. Comparison of the subthreshold leakage current of low-V_t and dual-V_t domino logic circuits for the two states of the dynamic node (under similar noise immunity conditions). The leakage current of each gate is normalized to the leakage current of the corresponding low-V_t gate with a high dynamic node voltage (H). L: low dynamic node voltage. Dual-V_t-HVK: dual-V_t domino with high-V_t keeper. Dual-V_t-LVK: dual-V_t domino with low-V_t keeper. Low-Vt: standard low-V_t domino circuit.

For the high voltage state of the dynamic node, the subthreshold leakage current characteristics of dual-V_t domino circuits are similar to low-V_t circuits. When the dynamic node voltage is low, the subthreshold leakage current of a dual-V_t domino logic circuit is significantly increased, provided that a low-V_t keeper rather than a high-V_t keeper transistor is employed. The subthreshold leakage current conduction paths within a dual-V_t domino logic circuit with a low-V_t keeper at a low dynamic node voltage are shown in Fig. 7. When the dynamic node voltage is low, the total subthreshold leakage current of a dual-V_t domino gate with a low-V_t keeper is

$$I_{subthreshold-L} = I_{Leak-HVPU} + I_{Leak-LVK} + I_{Leak-HVN}, \quad (4)$$

where $I_{Leak\text{-}LVK}$ is the subthreshold leakage current through a low-V_t keeper transistor.

Under similar noise immunity conditions, the subthreshold leakage current of dual-V_t domino logic circuits with a low-V_t keeper at a low dynamic node voltage is 21 (AND2, OR2, and OR4) to 41 times (MUX16) smaller as compared to low-V_t domino logic circuits with a low dynamic node voltage. Alternatively, as compared to low-V_t domino logic circuits with a high dynamic node voltage, the subthreshold leakage current of dual-V_t domino logic circuits with a low-V_t keeper at a low dynamic node voltage is 14 (AND4, AND6, and AND8) to 503 times (MUX16) smaller. Since $I_{Leak\text{-}LVK}$ is higher than $I_{Leak\text{-}HVK}$, the subthreshold leakage current of dual-V_t domino circuits with a low-V_t keeper is 5.7 (MUX16) to 10.9 times (OR4) higher than the subthreshold leakage current of dual-V_t domino logic circuits with a high-V_t keeper, under similar noise immunity conditions.

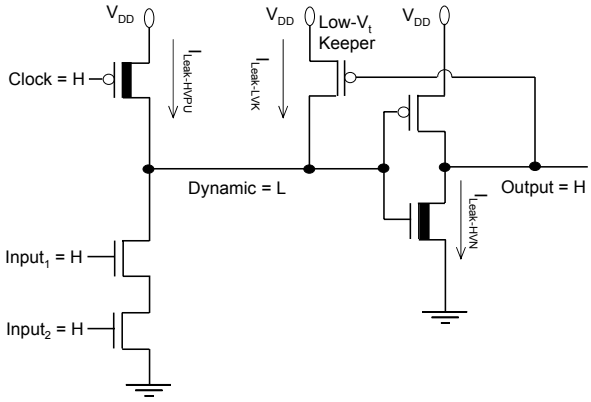

Fig. 7. Subthreshold leakage current conduction paths for the low (L) voltage state of the dynamic node in a dual-V_t domino AND gate with a low-V_t keeper. LVK: Low-V_t keeper transistor. HVPU: High-V_t pull-up transistor. HVN: High-V_t NMOS transistor.

4. POWER AND DELAY CHARACTERISTICS DURING THE ACTIVE MODE

The evaluation delay, precharge delay, and power consumption of dual-V_t and low-V_t domino logic circuits are evaluated in this section. The evaluation and precharge delay of example domino circuits are shown in Figs. 8 and 9, respectively. The power consumption characteristics of dual-V_t and low-V_t domino logic circuits are illustrated in Fig. 10.

As shown in Figs. 8 and 10, dual-V_t domino logic circuits have reduced evaluation delay and power consumption as compared to low-V_t domino logic circuits with the same size transistors. The enhancement in the delay and power characteristics is primarily due to the reduced contention current [1] of a high-V_t keeper transistor and the increased low-to-high gain of the output inverter.

In dual-V_t circuits, provided that the high-V_t keeper and the output inverter are sized to maintain a similar noise immunity (SNI) as compared to low-V_t circuits, except for the eight input AND gate, the evaluation delay is greater as compared to the low-V_t circuits. The degradation in the evaluation speed is less than 11.8% (OR4). The increase in the precharge delay of the dual-V_t domino circuits with high-V_t keepers is less than 23.4% (OR8) as compared to the low-V_t circuits. The increase in the active mode power consumption is less than 5.1% (AND2). For the six and eight input AND gates and the 16-bit multiplexer, the dual-V_t domino logic circuit technique reduces the power consumed during both the active and standby modes while providing a similar noise immunity as compared to the low-V_t circuit technique.

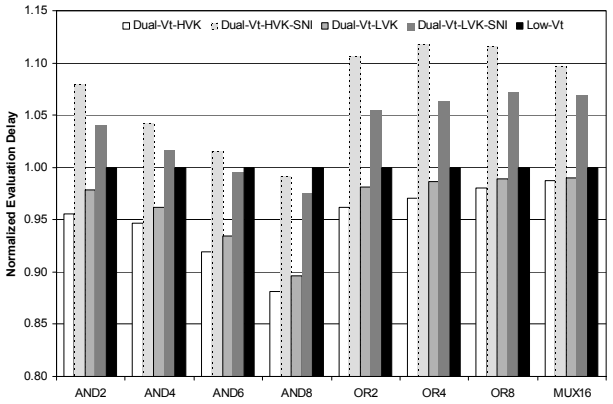

Fig. 8. Comparison of the evaluation delay of domino logic circuits. The evaluation delay of each gate is normalized to the delay of the corresponding low-V_t gate. SNI: same noise immunity.

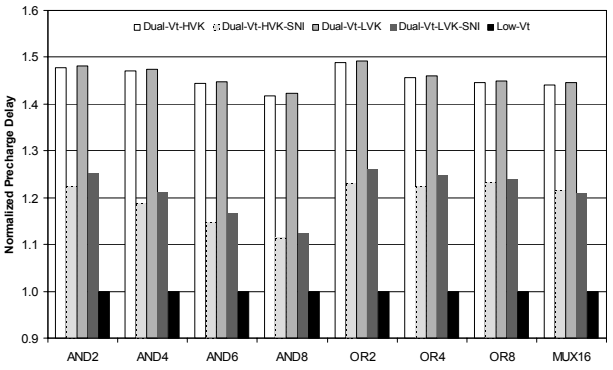

Fig. 9. Comparison of the precharge delay of domino logic circuits. The precharge delay of each gate is normalized to the precharge delay of the corresponding low-V_t gate. SNI: same noise immunity.

5. CONCLUSIONS

The node voltage dependent subthreshold leakage current characteristics of domino logic circuits are examined in this paper. A discharged dynamic node is preferred for reducing the leakage current in a dual-V_t domino logic circuit. Alternatively, a charged dynamic node is preferred for smaller subthreshold leakage energy in a standard low-V_t domino logic circuit with stacked pull-down devices, such as an AND gate.

Proper keeper and output inverter sizes are required in a dual-V_t domino logic circuit with a high-V_t keeper in order to maintain a similar noise immunity as compared to a standard low-V_t domino logic circuit. As an alternative dual-V_t domino technique for enhanced noise immunity, the effect of a low threshold voltage keeper transistor on the leakage current characteristics is also evaluated. Under similar noise immunity conditions as compared to standard low-V_t domino logic circuits, the savings in subthreshold leakage energy offered by dual-V_t domino circuits with a high-V_t keeper is 5.7 to 10.9 times greater as compared to the savings in leakage current offered by dual-V_t domino circuits with a low-V_t keeper.

Under similar noise immunity conditions, the subthreshold leakage current of dual-V_t domino logic circuits with a low dynamic node voltage is 224 to 235 times smaller as compared to low-V_t domino logic circuits with a low dynamic node voltage. Alternatively, as compared to low-V_t domino logic circuits with a high dynamic node voltage, the subthreshold leakage current of dual-V_t domino logic circuits with a low dynamic node voltage is 89 to 3079 times smaller. The degradation in the precharge and evaluation speed of dual-V_t domino circuits is less than 23.4% and 11.8%, respectively, as compared to standard low-V_t domino circuits. The increase in the active mode power consumption is less than 5.1%.

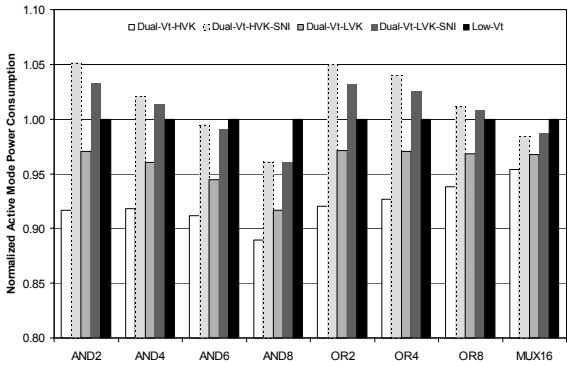

Fig. 10. Comparison of the power consumption of domino logic circuits during the active mode. The power consumed by each gate is normalized to the power consumption of the corresponding low-V_t gate. SNI: same noise immunity.

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