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Noise and Delay Uncertainty Studies for Coupled *RC* Interconnects

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Abstract

The performance of high-speed VLSI circuits is increasingly limited by interconnect coupling noise. In this paper we present a closed-form crosstalk noise model with accuracy comparable to that of SPICE for an arbitrary ramp input. We also develop a simplified delay model for estimating delays on coupled *RC* lines considering input slew times for both aggressor and victim lines. We then apply our model along with SPICE simulation to perform various studies of delay uncertainty in coupled interconnects. With respect to the effects of changing aggressor slew time on victim delay (i.e., *delay variation*), we observe that the victim delay is worst when the aggressor is switching very fast (e.g., step input). For local interconnects the delay variation (change in victim delay with varying input slew) can be as high as 70%. On the other hand, delay variation is around 10% for global interconnects. We also observe that the difference between minimum and maximum delay (i.e., *delay uncertainty*) decreases significantly as slew times are increased. Delay uncertainty on the victim wire is high for global wires as compared to local wires, a consequence of differing ratios of coupling to parallel-plate capacitance, and wire to load capacitance. We believe that our noise and delay analytical models form an effective basis for methodologies that lead to less over-design and guard-banding in high-performance system designs.

1 Introduction

Interconnects are an important performance limiting factor in today's high-speed and high-density VLSI designs. A major reason for this is the increasing importance of crosstalk between parallel *RC* interconnect lines [1] [7]. The crosstalk due to the capacitive coupling between lines increases as the average length of interconnects increases, as the density of interconnect routings increases, and as the switching speeds of devices increases. Coupling between signal lines is severe for deep-submicron designs where line-to-line capacitances are significant compared to line-to-substrate capacitances. Interconnect geometry in deep-submicron technologies is being aggressively scaled down for wiring densities, leading to high aspect ratios in metal lines. High-speed circuits (such as dynamic circuits and latches) are very sensitive to noise at both input and output nodes, which makes coupling an important issue. Even though it is possible to extract a detailed coupled *RC* network for all signal lines, the simulation of the entire *RC* network is computationally expensive. When the number of signal lines exceeds one million as it easily does in today's advanced microprocessors, SPICE simulations of each line are too inefficient to carry out. It is important to be able to quickly verify that the noise peak on sensitive nodes is below recommended threshold level to ensure acceptable signal integrity in limited design cycle times. Similarly, it is necessary to compute delay uncertainty (or variation) for all coupled lines in the design quickly and consider this margin in the static timing analysis.

Today's timing analysis tools employ a technique which takes the coupling capacitance to be some multiple of ground capacitance depending upon the switching conditions. A single effective capacitance value for the interconnect is computed for use in delay estimation. This is multiplied by a *switching factor*, which is taken to be slightly more than zero for a pair of lines switching in the same direction, and slightly less than two for a pair of lines switching in the opposite direction. The downside of this simple technique is that it can lead to highly optimistic or pessimistic estimates of delay. This motivates the development of more accurate predictors of coupling-induced delay based on coupling capacitance values and switching activity (slew times, offsets).

Several notable previous works model the effects of interconnect fringing and coupling capacitance on delay and crosstalk. [9] proposes a detailed noise analysis using full-chip parasitic extraction and model order reduction to compress parasitic data. This type of detailed noise analysis, which is done after physical design, is computationally expensive and identifies noise problems too late in the design cycle. The approach of [2] uses a detailed victim net analysis but applies an infinite ramp instead of a finite ramp as input to the aggressor net. To simplify the analysis further each coupling capacitor is replaced by a current source whose value is slew rate (i.e., slew rate of aggressor source voltage) times the coupling capacitance. It is implicitly assumed that the aggressor signal slope does not degrade downstream from the aggressor source. Hence, for longer lines this approach can produce either overestimated or underestimated peak noise values. Sakurai [10] solves partial differential equations for coupled *RC* lines to derive noise and delay expressions. However, driver modeling is not considered and the analysis is limited to step response. Kawaguchi and Sakurai [5] use the diffusion equation to analyze capacitively coupled interconnects, but also consider only the case of a step input. Different peak noise expressions are derived for various combinations of driver resistance to wire resistance ratio and load capacitance to wire capacitance ratio. [11] uses an *L* model for *RC* interconnects and obtain noise bounds for the case of a step input only. Also, their model does not take into account the interconnect resistance while deriving noise expressions. In addition, they make several assumptions while deriving the final expressions for the noise and delay. E.g., they assume $R_{driver} \ll R_{int}$ and $C_{load} \ll C_{int}$. Nakagawa et al. [6] use a L-model for interconnects to compute peak noise expressions under ramp inputs. However, they assume that peak noise always occurs after time $t \geq T_S$ where T_S is slew time at the output of aggressor driver. They derive the slew time at the output of aggressor driver as a function of input slew time of the driver, intrinsic gate delay, and gate load delay considering effective capacitance seen by the driver. Yee et al. [12] present simulation-based evidence that documents the magnitude of crosstalk-induced delay.

Contributions of This Work

In this paper, we present improved estimators for noise and delay phenomena due to coupling capacitance. The improved accuracy of our estimators, along with our analyses of delay variation and delay uncertainty, can (i) be useful in analyzing the sensitivity of circuit performance to various interconnect tuning parameters, and (ii) lead to less over-design and guard-banding at all stages of a performance-convergent synthesis and layout methodology for high-performance designs.

Our specific contributions are as follows. First, we use a lumped Π model for *RC* interconnects, which is more accurate than the *L* models used in [8] [11]; we also handle cases of different ramp inputs on the victim and aggressor lines. Second, we perform studies of both *delay variation* and *delay uncertainty* in local and global interconnects. *Delay variation* is defined to be the variation in a given line delay due to switching activity on neighboring line(s). Our studies show that change in slew time at the inputs of coupled lines has a big impact on delay

variation. For local interconnects the change in victim delay with respect to slew can be as high as 70%, while for global interconnects (long wires) the variation in delay is around 10%. *Delay uncertainty* is defined to be the difference between maximum (typically, aggressor(s) switching in opposite direction to victim) and minimum (typically, aggressor(s) switching in same direction) victim line delay over all possible cases of switching activity on neighboring aggressor line(s). Our studies indicate that delay uncertainty decreases rapidly as slew times are increased. Delay uncertainty also increases with the relative amount of coupling vs. grounded or load capacitance, and hence is more significant for global wires.

2 Delay Model for Coupled Interconnects

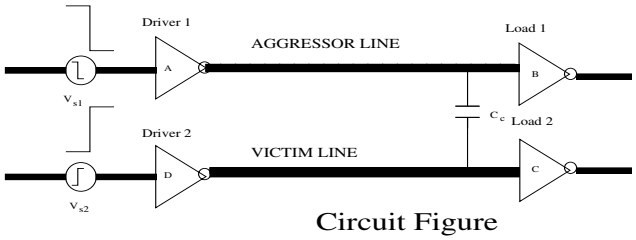

Figure 1: Two parallel coupled interconnects, with inverters as drivers and loads. This configuration is used for our analysis of peak noise on the victim, and delay on both aggressor and victim.

We consider two parallel coupled interconnects with drivers and loads attached, as shown in Figure 1. For the case when the victim line is quiet and aggressor line changes from 0 to VCC, the noise voltage is induced on victim line due to capacitive coupling. As a result of victim line resistance and the driver resistance, the induced voltage takes some time to decay in exponential form. If the induced voltage is high and if the induced voltage lasts longer (i.e., width of pulse) than a certain minimum then the destination gate (INV) generates a glitch and hence causes a logical error. For simplified analysis we use an equivalent circuit using Π model for the interconnects as shown in Figure 2. We analyze noise and delay at the end of the interconnects. Although for simplicity we consider just one aggressor line, our analyses extend easily to the case of more than one aggressor line for a given victim line. Our goal is to develop models to estimate delay on both aggressor and victim lines for three main cases: (i) victim line quiet, (ii) victim line active and switching in the opposite direction to the aggressor, and (iii) victim line active and switching in the same direction as the aggressor. The delay on victim line is worst-case when both aggressor and victim are switching in opposite directions, since the aggressor introduces charges in opposite direction to those on the victim. Similarly, the best-case delay on the victim line occurs when both aggressor and victim are switching in the same direction. Our approach below can be used to estimate the delays for all of these cases.

In this section, we apply the Π model for the interconnect and compute both the noise peak voltage and delay on the interconnects as shown in Figure 2. Our basic analysis approach is as follows:

- We use Figure 2 as the equivalent circuit for analysis purposes. Note that we have distributed the interconnect line capacitance in two parts (ground capacitance and coupling capacitance).
- We transform the time domain circuit equations to frequency domain using Laplace transforms, solve the equations, then convert the results back to the time domain.
- To find the noise voltage at the end of victim line, we must solve for $v_C(t)$, while to find the impact of crosstalk on delay, we must solve for $v_B(t)$. The nodal equations at nodes A, B, C and D in Figure 1 are given in (1).

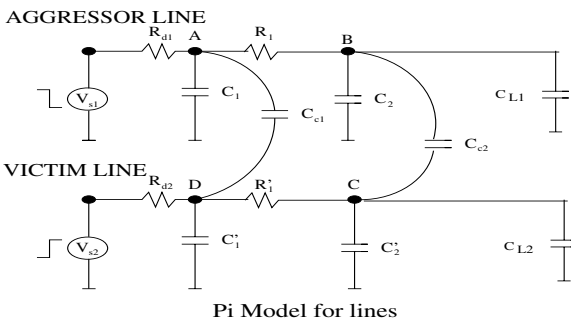

Figure 2: Equivalent circuit (using Π model for interconnect) for the configuration of Figure 1.

$$\begin{aligned} V_{S1} &= V_A + R_{d1}\left[V_A sC_1 + (V_A - V_D)sC_{C1} + V_B sC_2 \right. \\ &\quad \left. + (V_B - V_C)sC_{C2}\right] \\ V_A &= V_B + R_1\left[V_B sC_2 + (V_B - V_C)sC_{C2}\right] \\ V_{S2} &= V_D + R_{d2}\left[V_D sC_1' + (V_D - V_A)sC_{C1} + V_C sC_2' \right. \\ &\quad \left. + (V_C - V_B)sC_{C2}\right] \\ V_D &= V_C + R_1'\left[V_C sC_2' + (V_C - V_B)sC_{C2}\right] \end{aligned} \tag{1}$$

where R_{d1} and R_{d2} are driver on-resistances of aggressor and victim lines, R_1 and R_1' are total resistance of aggressor and victim lines, C_1 (C_2) and C_1' (C_2') are ground capacitances of aggressor and victim lines, and finally, C_{c1} and C_{c2} are coupling capacitances between aggressor and victim lines. We have included the load capacitances C_{L1} and C_{L2} in C_1' and C_2' respectively to simplify the nodal equations.

Effect of Victim and Aggressor Switching

In this section, we are interested in studying the variation of victim wire delay as a function of aggressor/victim line slew times. We analyze a general case of aggressor and victim lines switching when we have two different voltage sources attached to their inputs. So the slew times and the time offsets from origin of both voltage sources can be different. Solving the set of Equations (1) with different voltage sources V_{S1} and V_{S2} yields the following expressions for voltages at node B and C (after retaining terms with up to power of two in s):

$$V_C = V_{S2}\frac{(1 + a_1 s + a_2 s^2)}{(1 + b_1 s + b_2 s^2)} + V_{S1}\frac{(a_3 s + a_4 s^2)}{(1 + b_1 s + b_2 s^2)} \tag{2}$$

$$V_B = V_{S1}\frac{(1 + c_1 s + c_2 s^2)}{(1 + b_1 s + b_2 s^2)} + V_{S2}\frac{(c_3 s + c_4 s^2)}{(1 + b_1 s + b_2 s^2)} \tag{3}$$

where

$$\begin{aligned} a_1 &= R_1C_2 + R_1C_{C2} + R_{d1}C_1 + R_{d1}C_{C1} + R_{d1}C_2 + R_{d1}C_{C2} \\ a_2 &= R_{d1}C_1R_1C_{C2} + R_{d1}C_1R_1C_2 + R_{d1}C_{C1}R_1C_2 + R_{d1}C_{C1}R_1C_{C2} \\ &\quad + R_{d1}C_{C1}R_1'C_{C2} \\ a_3 &= R_{d2}C_{C1} + R_{d2}C_{C2} + R_1'C_{C2} \\ a_4 &= R_{d2}C_1'R_1'C_{C2} + R_{d2}C_{C1}R_1'C_{C2} + R_{d2}C_{C1}R_1C_2 + R_{d2}C_{C1}R_1C_{C2} \\ c_1 &= R_1'C_2' + R_1'C_{C2} + R_{d2}C_1' + R_{d2}C_{C1} + R_{d2}C_2' + R_{d2}C_{C2} \\ c_2 &= R_{d2}C_1'R_1'C_{C2} + R_{d2}C_1'R_1'C_2' + R_{d2}C_{C1}R_1'C_2' + R_{d2}C_{C1}R_1'C_{C2} \\ &\quad + R_{d2}C_{C1}R_1C_{C2} \\ c_4 &= R_{d1}C_1R_1C_{C2} + R_{d1}C_{C1}R_1C_{C2} + R_{d1}C_{C1}R_1'C_2' + R_{d1}C_{C1}R_1'C_{C2} \\ c_3 &= R_{d1}C_{C1} + R_{d1}C_{C2} + R_1C_{C2} \end{aligned} \tag{4}$$

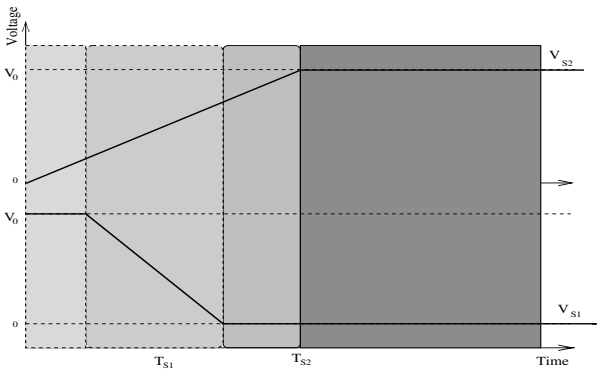

Figure 3: Different regimes to be considered for calculating delay due to coupling under ramp input on the victim and aggressor lines.

and the denominator terms b_1 and b_2 are given by

$$\begin{aligned} b_1 &= R'_1C_{C2} + R_{d2}C_{C2} + R_{d2}C_{C1} + R'_1C'_2 + R_{d1}C_{C1} + R_{d1}C_{C2} + R_1C_{C2} \\ &\quad + R_{d2}C'_1 + R_{d1}C_1 + R_{d2}C'_2 + R_1C_2 + R_{d1}C_2 \\ b_2 &= R_{d2}C'_1R'_1C_{C2} + R_{d2}C_{C1}R'_1C_{C2} + R_{d2}C_{C1}R_1C_{C2} + R_{d2}C_{C1}R_1C_2 \\ &\quad + R_{d1}C_2R'_1C_{C2} + R_{d1}C_2R_{d2}C'_1 + R_{d1}C_2R_{d2}C_{C1} + R_{d1}C_2R_{d2}C'_2 \\ &\quad + R_{d1}C_2R_{d2}C_{C2} + R_{d1}C_1R'_1C'_2 + R_{d1}C_1R'_1C_{C2} + R_{d1}C_1R_{d2}C'_1 \\ &\quad + R_{d1}C_1R_{d2}C_{C1} + R_{d1}C_1R_{d2}C'_2 + R_{d1}C_1R_{d2}C_{C2} + R_{d2}C'_1R'_1C'_2 \\ &\quad + R_1C_2R'_1C'_2 + R_1C_2R'_1C_{C2} + R_1C_2R_{d2}C'_1 + R_{d2}C_{C1}R'_1C'_2 \\ &\quad + R_{d1}C_1R_1C_2 + R_{d1}C_1R_1C_{C2} + R_{d1}C_{C1}R_1C_2 + R_{d1}C_{C1}R_1C_{C2} \\ &\quad + R_{d1}C_{C1}R'_1C'_2 + R_{d1}C_{C1}R'_1C_{C2} + R_{d1}C_{C2}R'_1C'_2 + R_{d1}C_{C2}R_{d2}C'_1 \\ &\quad + R_{d1}C_{C2}R_{d2}C'_2 + R_{d1}C_{C1}R_{d2}C'_1 + R_{d1}C_{C1}R_{d2}C'_2 + R_1C_2R_{d2}C'_2 \\ &\quad + R_1C_2R_{d2}C_{C2} + R_1C_{C2}R'_1C'_2 + R_1C_{C2}R_{d2}C'_1 + \\ &\quad R_1C_{C2}R_{d2}C'_2 + R_{d1}C_2R'_1C'_2 \end{aligned} \tag{5}$$

The transfer function $\frac{V_C}{V_{S2}}$ for victim line is a function of ratio of voltage sources $\frac{V_{S1}}{V_{S2}}$ and we try to express this ratio as a polynomial in s, i.e.,

$$\frac{V_C}{V_{S2}} = \frac{(a_{00} + a_{11}s + a_{22}s^2)}{(1 + b_1s + b_2s^2)}$$

Figure 3 shows the different possible regimes to consider for analyses. We consider two different ramp inputs with different slew times and zero offsets for simplicity for our analysis. The ramp input voltage at aggressor can be expressed as $V_{S1} = \frac{v_0}{s^2T_{S1}}$ for linear ramp region and $V_{S1} = \frac{v_0}{s^2T_{S1}}\left(1 - e^{-sT_{S1}}\right)$ for saturated ramp region [3]. Depending on the rising or falling ramp input the magnitude v_0 could be either positive or negative. We use a factor α to represent the sign of ramp inputs, i.e., for same-direction ramps $\alpha = 1$, for opposite-direction ramps $\alpha = -1$, and if one line is quiet and other is switching $\alpha = 0$. We consider the $\alpha \neq 0$ cases in this section and the case of $\alpha = 0$ in the next section, below. For linear ramps the ratio of voltage sources (i.e., for $t \leq \min(T_{S1}, T_{S2})$) is $\frac{T_{S2}}{T_{S1}}$. The corresponding coefficients of the coupled transfer function of the victim line are

$$a_{00} = 1, \quad a_{11} = a_1 + \alpha\frac{T_{S2}}{T_{S1}}a_3, \quad a_{22} = a_2 + \alpha\frac{T_{S2}}{T_{S1}}a_4 \tag{6}$$

For the region where a linear ramp and a saturated ramp overlap the ratio of voltage sources can be approximated as

$$\begin{aligned} \frac{V_{S1}}{V_{S2}} &= \alpha\left(T_{S2}s - \frac{T_{S1}T_{S2}}{2}s^2\right) && T_{S1} < t \leq T_{S2} \\ \frac{V_{S1}}{V_{S2}} &= \alpha\left(\frac{1}{T_{S1}}s^{-1} + \frac{T_{S2}}{2T_{S1}} + \frac{T_{S2}^2}{12T_{S1}}s\right) && T_{S2} < t \leq T_{S1} \end{aligned} \tag{7}$$

The corresponding coefficients of the coupled transfer function of the victim line are given for two cases. The coefficients for the case when $T_{S1} < t \leq T_{S2}$ are

$$a_{00} = 1, \quad a_{11} = a_1, \quad a_{22} = a_2 + \alpha T_{S2}a_3 \tag{8}$$

The coefficients for the case when $T_{S2} < t \leq T_{S1}$ are

$$\begin{aligned} a_{00} &= 1 + \alpha\frac{1}{T_{S1}}a_3 \\ a_{11} &= a_1 + \alpha\left(\frac{T_{S2}}{2T_{S1}}a_3 + \frac{1}{T_{S1}}a_4\right) \\ a_{22} &= a_2 + \alpha\left(\frac{T_{S2}}{2T_{S1}}a_4 + \frac{T_{S2}^2}{12T_{S1}}a_3\right) \end{aligned} \tag{9}$$

Finally, for the region of saturated ramps ratio of voltage sources with a first order approximation is $\frac{V_{S1}}{V_{S2}} = \alpha(1 + \frac{T_{S2} - T_{S1}}{2}s)$. The corresponding coefficients of the coupled transfer function of the victim line are

$$\begin{aligned} a_{00} &= 1, & a_{11} &= a_1 + \alpha a_3, \\ a_{22} &= a_2 + \alpha\left(\frac{T_{S2} - T_{S1}}{2}a_3 + a_4\right) \end{aligned} \tag{10}$$

Hence, the transfer function for the victim line can be expressed as[1]

$$\frac{V_C}{V_{S2}} = \frac{(a_{00} + a_{11}s + a_{22}s^2)}{(1 + b_1s + b_2s^2)} \tag{11}$$

Using partial fractions and inverse Laplace transforms allows us to convert the $V_C(s)$ in Equation (11) into a time-domain expression for ramp source of V_{S2}, i.e.,

$$v_C(t) = \begin{cases} \frac{v_0}{T_{S2}}\left(k_0 + k_1t + k_2e^{s_2t} + k_3e^{s_1t}\right) \\ \qquad t \leq T_{S1}, t \leq T_{S2} \text{ or if } T_{S1} < t \leq TS2 \\ \frac{v_0}{T_{S2}}\left[k_1T_{S2} + k_2\left(e^{s_2t} - e^{s_2(t-T_{S2})}\right) + k_3\left(e^{s_1t} - e^{s_1(t-T_{S2})}\right)\right] \\ \qquad t > T_{S1}, t > TS2 \text{ or if } T_{S2} < t \leq TS1 \end{cases} \tag{12}$$

where $k_0 = (-a_{00}b_1 + a_{11})$, $k_1 = a_{00}$,
$k_2 = \frac{1}{2b_2s_2 + b_1}\left(b_2s_2b_1a_{00} + a_{00}b_1^2 - a_{11}b_2s_2 - a_{11}b_1 - a_{00}b_2 + a_{22}\right)$,
$k_3 = -\frac{1}{2b_2s_2 + b_1}(-a_{00}b_2 + a_{22} - a_{00}b_2s_2b_1 + a_{11}b_2s_2)$, $s_2s_1 = \frac{1}{b_2}$,
and $s_2 + s_1 = -\frac{b_1}{b_2}$. We need to use appropriate a_{00}, a_{11}, a_{22} from Equations 6, 8, 9, and 10 depending on the range to which t belongs.

We now compute an analytical expression for delay using the above $v_C(t)$ expression. Let v_{th} be the threshold voltage of interest at which we would like to compute the delay. Since we are interested in delay relative to input ramp (V_{S2}) we need to subtract ramp input delay at that threshold, i.e., $v_{th}T_{S2}$, from the output response delay. Therefore, the victim wire delay (D_v) for both the linear and saturated ramp regions can be obtained as [3]

$$D_v = \begin{cases} \frac{1}{k_1}\left((1 - k_1)v_{th}T_{S2} - k_0 - k_3e^{s_1T_{AD}}\right) \\ \qquad t \leq T_{S1}, t \leq T_{S2} \text{ or if } T_{S1} < t \leq TS2 \\ (1 - v_{th})T_{S2} + \frac{1}{|s_1|}\left|\ln\left(\frac{k_3(1 - e^{-|s_1|T_{S2}})}{T_{S2}(1 - v_{th})}\right)\right| \\ \qquad t > T_{S1}, t > TS2 \text{ or if } T_{S2} < t \leq TS1 \end{cases} \tag{13}$$

where $T_{AD} = v_{th}T_{S2} + b_1$ is analytical delay approximation for ramp response.

[1] Similarly, the transfer function for the aggressor line can be expressed as $\frac{V_B}{V_{S1}} = \frac{(1 + c_{11}s + c_{22}s^2)}{(1 + b_1s + b_2s^2)}$ where coefficients c_{11} and c_{22} are functions of the ratio of ramp inputs and also depend on the type of ramps (linear or saturated, etc.). The time-domain expression for $v_B(t)$ can be derived in similarly to $v_C(t)$.

3 Peak Noise Estimation on Victim Line

The case of peak noise can be analyzed when the victim line is quiet at low voltage, while the aggressor line is switching from low to high. Therefore, $V_{S2} = 0$. Solving the Equations (1) with $V_{S2} = 0$ yields the following transfer function in frequency domain for noise at node C of the victim line (we approximate the solution to second moment only).

$$\frac{V_C}{V_{S1}} = \frac{a_3 s + a_4 s^2}{1 + b_1 s + b_2 s^2} \tag{14}$$

where coefficients a_i's and b_i's are given by Equations (5) and (4). We now compute the time-domain solutions voltage on both victim and aggressor lines by considering step and ramp inputs at the input of the aggressor line. The expression for ramp input in transform domain is $V_{S1} = \frac{v_0}{s^2 T_S}\left(1 - e^{-sT_S}\right)$ and as before we assume the victim line is quiet, i.e., $V_{S2} = 0$. Then the voltage at node C of the victim line in the transform domain can be written as

$$V_C(s) = \frac{v_0(1 - e^{-sT_S})}{T_S b_2}\left[\frac{k_0}{s} + \frac{k_1}{s - s_1} + \frac{k_2}{s - s_2}\right]$$

The corresponding time-domain expression is given by

$$v_C(t) = \begin{cases} \frac{v_0}{b_2 T_S}\left(k_0 + k_1 e^{s_1 t} + k_2 e^{s_2 t}\right) & t \le T_S \\ \frac{v_0}{b_2 T_S}\left[k_1\left(e^{s_1 t} - e^{s_1(t-T_S)}\right) + k_2\left(e^{s_2 t} - e^{s_2(t-T_S)}\right)\right] & t > T_S \end{cases} \tag{15}$$

where $k_0 = a_3 b_2$, $k_1 = -\frac{b_2(a_4 + s_2 b_2 a_3)}{2 s_2 b_2 + b_1}$, $k_2 = \frac{b_2(-s_2 b_2 a_3 - a_3 b_1 + a_4)}{2 s_2 b_2 + b_1}$, $s_1 s_2 = \frac{1}{b_2}$, and $s_1 + s_2 = -\frac{b_1}{b_2}$. Similarly, we can compute the voltage at node B of the aggressor line using the equations given in previous section. The voltage $v_C(t)$ represents noise on victim line due to the input switching on the aggressor line. To find the peak noise for this configuration, we differentiate Equation (15) with respect to t and set the derivative to zero. The time at which peak noise is reached is

$$\begin{aligned} t_{peak1} &= \left(\frac{1}{s_2 - s_1}\right)\ln\left(-\frac{k_1 s_1}{k_2 s_2}\right) && 0 \le t_{peak1} \le T_S \\ t_{peak2} &= \left(\frac{1}{s_2 - s_1}\right)\ln\left\{\left(-\frac{k_1 s_1}{k_2 s_2}\right)\left(\frac{1 - e^{-s_1 T_S}}{1 - e^{-s_2 T_S}}\right)\right\} && t_{peak2} > T_S \end{aligned} \tag{16}$$

from which peak noise voltage can be computed by substituting t_{peak} values into Equation (15), with $v_C(t_{peak}) = \max\left\{v_C(t_{peak1}), v_C(t_{peak2})\right\}$. Similarly, for step input at the aggressor line the time to reach peak noise is given by

$$t_{peak} = \left(\frac{1}{s_2 - s_1}\right)\ln\left(-\frac{k_1 s_1}{k_2 s_2}\right) \tag{17}$$

and the corresponding peak noise for step input is expressed as

$$v_C(t_{peak}) = \frac{v_0}{b_2}\left(k_1 e^{s_1 t_{peak}} + k_2 e^{s_2 t_{peak}}\right) \tag{18}$$

Even though the above discussion was computing peak noise for two coupled lines we can extend our approach for the case of multiple aggressor lines effecting a single victim line. We think that each aggressor and victim line (overlap section of the lines) can be analyzed independently to compute noise peaks and from the super-position principle of voltage we can add up all the noise peaks for each pair to compute the total noise peak value.

Cases	width (in μm)	spacing (in μm)	length (in μm)	R_{int} (in Ω)	C_{gnd} (in fF)	C_{coup} (in fF)
1	0.49	0.46	1000	122.9	63.2	115.02
2	0.49	0.46	5000	614.32	315.77	575.03
3	1.00	0.46	10000	605.63	983.97	1187.03
4	0.49	1.30	1000	122.9	109.3	46.2

Table 1: Interconnect parameters used in various SPICE simulations (C_L = 153 fF due to inverter gate capacitance for all cases).

4 Simulation Results

To validate our new analyses, we have considered two adjacent M3 interconnects used in a real microprocessor design for 0.25 μm CMOS technology. We assume identical interconnects are driven by identical inverters of size (56,28) μm, and also assume that the loads at the end of the lines are identically sized inverters. We study various configurations of interconnect length, width, and spacing as shown in Table 1. The context for this experimentation is to discover how close our Π models compare to SPICE simulations for delay estimation. We note that all models proposed above are extremely efficient to evaluate (despite sometimes long expressions) and runtimes are negligible for all models, particularly when compared to SPICE runtimes. The above obtained analytical equations for voltage on victim and aggressor lines are useful in computing noise, delay and/or delay uncertainty and how it changes with respect to input slew time, coupling capacitance, etc.

Cases	$T_S = 0\ ps$				$T_S = 100\ ps$	
	SPICE	$L_{[11]}$	[5]	Π_{Our}	SPICE	Π_{Our}
1	0.080	0.174	0.174	0.088	0.060	0.060
2	0.210	0.275	0.275	0.184	0.209	0.183
3	0.221	0.255	0.255	0.183	0.210	0.183
4	0.037	0.075	0.075	0.037	0.026	0.024

Cases	$T_S = 200\ ps$		$T_S = 400\ ps$	
	SPICE	Π_{Our}	SPICE	Π_{Our}
1	0.035	0.035	0.018	0.017
2	0.200	0.181	0.198	0.173
3	0.202	0.183	0.199	0.181
4	0.012	0.010	0.007	0.007

Table 2: Normalized peak noise values for different input slew times for the two coupled interconnect configuration under various models.

We now express the circuit parameters of the models Figure 2 in terms of the interconnect parameters given in Table 1. For the L interconnect model, we consider $C_1' = C_1 = C_{gnd} + C_L$ and $C_{c1} = C_{coup}$, while for the Π interconnect model, $C_1' = C_1 = C_{gnd}/2$, $C_2' = C_2 = C_{gnd}/2 + C_L$ and $C_{c1} = Cc2 = C_{coup}/2$. The load capacitance due to the inverter gate capacitance is $C_{L1} = C_{L2} = 153\ fF$.

4.1 Peak Noise Results

We simulate the coupled interconnects by using different input slew times ranging from 0ps to 400ps for the driving inverters. We first compute the noise peaks for all four test cases under different slew times using SPICE simulation and our Π model as shown in Table 2. For the Π model the noise peak (Π_{Our}) is computed using Equation (18) for step input and using Equation (15) for ramp input (Section 3). The noise values presented in the table are normalized to the supply voltage. Peak normalized noise values in Tables 2 for step input are also compared with the two existing models of [5] and [11], as well as with SPICE simulation results. The $L_{[11]}$ values are the peak noise values obtained using the formula of [11]. For [5], we take the noise formula of Kawaguchi and Sakurai [5] for the 2-line case when both the victim

and aggressor lines are switching in opposite directions, and divide it by two to obtain the noise peak when only the aggressor is switching. Our results for the Π interconnect model as shown in Table 2 are within 13% of the values derived by SPICE results for peak noise. Also, our new noise estimators are substantially more accurate than previous models of [11] [5]; this implies less need for overdesign and guardbanding.

Cases	$T_S = 0$ *ps*		$T_S = 100$ *ps*	
	SPICE	Π_{Our}	SPICE	Π_{Our}
1	24	25	32	33
2	405	377	408	379
3	835	769	839	769
4	22	21	30	29
	$T_S = 200$ *ps*		$T_S = 400$ *ps*	
1	35	35	38	37
2	411	381	422	389
3	842	771	847	775
4	32	31	33	31

Table 3: Comparison of victim line interconnect delay for 50% threshold delay (in *ps*) using SPICE and our Π model for the case when the aggressor line switching opposite to the victim line. We assume identical slew time for both lines.

Cases	$T_S = 0$ *ps*		$T_S = 100$ *ps*	
	SPICE	Π_{Our}	SPICE	Π_{Our}
1	16	15	20	21
2	138	133	142	135
3	293	271	296	272
4	18	17	24	25
	$T_S = 200$ *ps*		$T_S = 400$ *ps*	
1	23	23	25	23
2	149	141	169	163
3	300	276	314	287
4	25	25	26	25

Table 4: Comparison of victim line interconnect delay for 50% threshold delay (in *ps*) using SPICE and our Π model for the case when the aggressor line switching in the same direction as the victim line. We again use identical slew time for both lines.

4.2 Delay Uncertainty and Delay Variation

Recall that the delay uncertainty of any line is defined to be the maximum difference in line delay due to any variation in switching conditions of neighboring lines. The maximum delay of any wire occurs when both coupled lines are switching in opposite direction with identical slew times of the signals arriving at the input of the lines. Similarly, the minimum delay of the wire occurs when both are switching in same direction and again with with identical slew times of input signal. This type of analysis to compute delay and/or delay uncertainty on an aggressor/victim line is also very useful for placement and routing tools to make correct decisions. We now study the variation of delay uncertainty with respect to slew times and coupling capacitance.

We simulate the coupled interconnects by using different input slew times ranging from 0ps to 400ps for the driving inverters. Table 3 shows a comparison of interconnect delays on the victim line computed using SPICE and our Π model for the case when both victim and aggressor line are switching in opposite directions. We use the 50% threshold to compute the interconnect delay from the output of the driver to the next inverter input. This case yields pessimistic or worst-case interconnect delay values between the two coupled interconnects. From Table 3 we see that our Π model delays are close to the SPICE-computed values. Similarly, Table 4 gives a comparison of interconnect delay on the victim line for the case when victim and aggressor are switching in same direction. This case yields optimistic or best-case interconnect delay values between the two coupled interconnects. Figure 4 plots delay uncertainty values from Tables 3 and 4 for different slew times such that both lines have same slew ($T_{S1} = T_{S2}$). Again, our Pi-Model results are close to SPICE results. This plot shows that delay remains constant under various slew values as long as $T_{S1} = T_{S2}$.

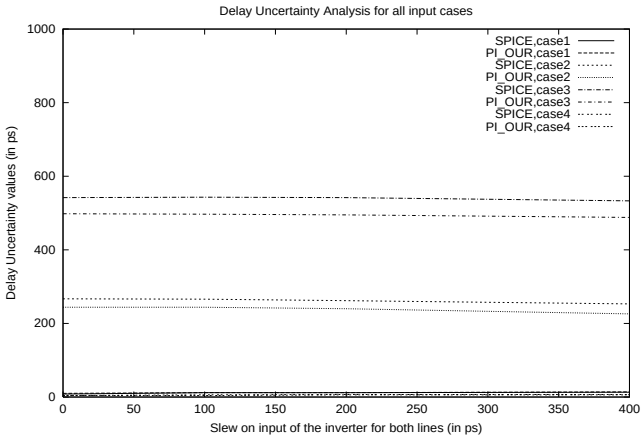

Figure 4: Plot of delay uncertainty for victim line (difference of worst case and best case delays) as obtained from Tables 3 and 4 for different slew times using Pi-Model and Spice simulations. This plot shows that delay remains constant for various slew values such that $T_{S1} = T_{S2}$.

T_{S1}	Case 1				Case 2			
	Best Case		Worst Case		Best Case		Worst Case	
	Our	Spice	Our	Spice	Our	Spice	Our	Spice
100	27	12	31	54	123	142	423	459
200	17	17	39	43	119	148	421	458
400	23	23	37	38	129	165	419	456
500	25	24	35	35	147	172	415	454
600	26	25	35	34	165	177	417	450
700	27	26	33	33	179	183	415	445
900	29	28	33	31	199	192	379	422
1000	30	29	31	30	205	196	379	410

Table 5: Victim line delay values for different slew times on the aggressor line. The slew on the victim line was 400ps for Case 1 and 700ps for Case 2.

We have also studied delay variation, i.e., the impact of change in slew time of coupled lines on the delay of victim/aggressor lines. For this analysis we keep the victim line slew constant (say at 400ps) and vary aggressor slew from 0 to 1000ps. A complete set of results for this experiment using both SPICE and our analytical approach is given in Table 5. We study both the cases when lines are switching in the same

Ratio C_{coup}/C_{gnd}	Case 1 (ps)		Case 2 (ps)	
	Our	Spice	Our	Spice
0.25	31	32	309	332
0.55	33	34	337	362
1.00	35	35	363	391
1.82	37	36	389	420
4.00	39	39	417	451

Table 6: Delay values for different coupling capacitances between the victim and the aggressor lines. The slew time is 400ps for both lines.

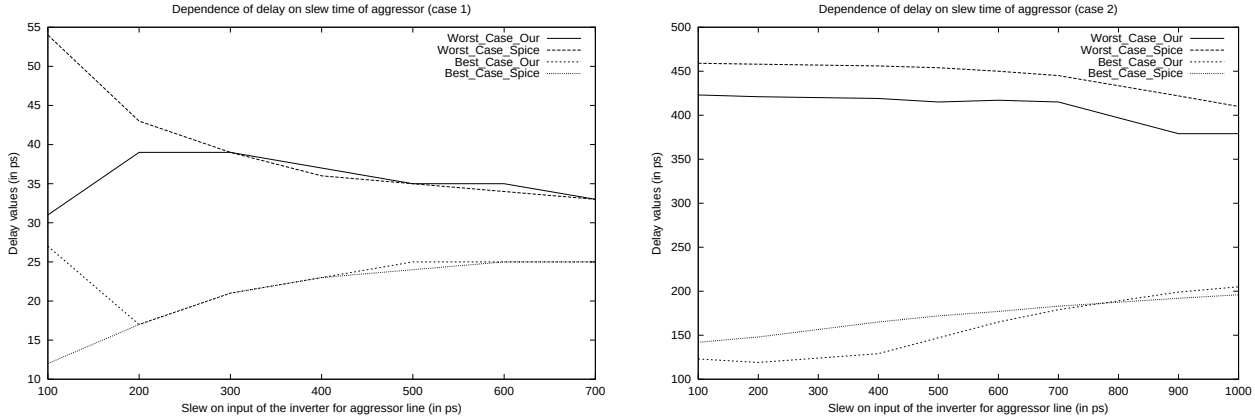

Figure 5: Plot of delay values for different slew times on the aggressor line while fixing the slew on victim line to 400ps for case 1 and 700ps for case 2. Delay values are also given in Table 5. Our Π model results are close to SPICE for slew times above 200ps. Worst case delay decreases as slew time of aggressor line is increased.

direction (best case) and in the opposite direction (worst case); our results are within 15% of SPICE results as shown in Figure 5. For local (short wires) interconnects the change in delay with respect to slew could be as high as 70%. In contrast for global interconnects (long wires) the delay variation is around 10%. (Our Π model results are close to SPICE for slew times above 200ps, and we are currently investigating the sources of error with respect to SPICE for smaller slew times.) The worst delay occurs on the victim line when the aggressor line is switching very fast (i.e., step input). Hence, delay calculation tools need to consider this worst-case corner for coupled interconnects.

Finally, Table 6 gives best- and worst-case victim line delays for various ratios of coupling capacitance to ground capacitance (parallel-plate capacitance). We notice that as the ratio of coupling capacitance to ground capacitance increases the worst case delay increases, and that this increase is significant for global wires (Ex: Case 2 in Table 6). For local wires the increase in delay with coupling capacitance to ground capacitance ratio is less. As expected, minimizing delay uncertainty and delay variation requires interconnect design such that less coupling capacitance is seen for global wires.

5 Conclusions

In conclusion, we have analyzed the accuracy and applicability of new, simple closed-form models for computing crosstalk noise and coupled line delay for deep-submicron interconnects. Specifically, we have derived analytical expressions for victim wire delay and studied the impact on delay due to aggressor wire input, for both the step input and ramp input regimes. Our approach extends easily to other modes of simultaneous switching, phase offsets, etc. We have also studied the impact on victim line delay of varying aggressor slew times and coupling-to-ground capacitance ratios. The approaches described in our paper potentially form the basis of a set of analytical tools to estimate noise peaks and delay uncertainty effects early in the ASIC physical implementation flow.

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