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NOISE IMMUNITY OF THE FIBONACCI COUNTER WITH THE FRACTAL DECODER DEVICE FOR TELECOMMUNICATION SYSTEMS

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The paper presents the improved method of noise immune Fibonacci counting in the minimal form of representation. The method was tested and investigated in the developed noise immune pulse counter based on a minimal form of Fibonacci code with a fractal decoding device. The proposed device, which is simulated in the NI Multisim software, possesses a homogenous structure, increased noise immunity, performance and detection of bit errors in the process of its operation.

Keywords: *Fibonacci code, fractal decoding device, minimal form, noise immunity, pulse counter, telecommunication systems.*

1. INTRODUCTION

Digital devices are determined by the structural characteristics of components of these devices, the improvement of which remains topical in our time. These devices can be implemented based on noise immunity number systems, among which the Fibonacci number system is distinguished [1]–[14].

The advantage of using noise immune number systems in digital devices is that the introduction of natural redundancy takes place at the stage of choosing the form of information representation. This allows for end-to-end control over the transmission and processing of information in digital devices. In addition, the use of noise immune number systems allows, in some cases, synthesising digital devices and components more noise immune and high-speed than using conventional binary number systems [6]–[9]. The feature of digital devices operating by noise immune number systems is that the redundancy necessary for detecting errors is evenly distributed in the structures of the digital scheme. Additional control schemes in them are either not used at all or are used with minimal hardware costs [10]–[14].

Decoders and pulse counters are the components of digital devices. The

counters, without decoding, synthesised based on the noise immunity number systems have high noise immunity but do not have the ability of decoding, which is necessary for their practical application.

Today, interest in Fibonacci codes is growing, as evidenced by a number of publications [1], [2], [10]–[14]. In this paper, we used the Fibonacci code in the minimal form of representation to build a high-speed noise immune counter with the fractal decoder device. This allows corresponding digital devices to be noise immune in other forms of the Fibonacci code representation. The noise immunity of pulse counter based on the minimal form of the Fibonacci code with a fractal decoding device can be used in high-speed telecommunication systems for collection and transmission of information. The use of Fibonacci codes in the telecommunication systems for collecting and transmitting information significantly increases the noise immunity and speed of information transfer. The device in the form of the Fibonacci counter with decoding also refers to automation and computing devices and can be used in systems of discrete information processing as a noise immune counter, pulse distributor, and the noise immune information coding device. The goal of the research is achieved through the introduction of new design features that provide efficient decoding of the counter states.

2. THE FIBONACCI CODE IN THE MINIMAL FORM OF REPRESENTATION

The Fibonacci numbers are the following sequence: 0, 1, 1, 2, 3, 5, 8, 13… F_n. Each number in it, starting with the third, is defined as the sum of the two previous elements: $F_n = F_{n-1} + F_{n-2}$, $F_1 = F_2 = 1$. In this paper, investigation of the Fibonacci code in a minimal form of representation is performed. Fibonacci code in the minimal form of representation by the following numerical function: $N = a_n F_n + a_{n-1} F_{n-1} + ... + a_i F_i + ... + a_1 F_1$, where $a_i \in \{01\}$ is the binary digit of the *i*-th bit of the positional representation of the number; *n* is the code length; F_i is the weight of the *i*-th bit, which equals the *i*-th Fibonacci number [4]. The appearance of such combinations indicates the presence of errors. Table 1 shows, for example, the Fibonacci code for *n* = 5, where *n* – the code length.

Table 1

The Fibonacci Code for the Code Length *n*=5

No.	The Fibonacci code					No.	The Fibonacci code				
	8	**5**	**3**	**2**	**1**		**8**	**5**	**3**	**2**	**1**
0	0	**0**	**0**	**0**	**0**	**8**	1	**0**	**0**	**0**	**0**
1	0	**0**	**0**	**0**	**1**	**9**	1	**0**	**0**	**0**	**1**
2	0	**0**	**0**	**1**	**0**	**10**	1	**0**	**0**	**1**	**0**
3	0	**0**	**1**	**0**	**0**	**11**	1	**0**	**1**	**0**	**0**
4	0	**0**	**1**	**0**	**1**	**12**	1	**0**	**1**	**0**	**1**
5	0	1	0	0	0						
6	0	1	0	0	1						
7	0	1	0	1	0						

The characteristic feature of the Fibonacci code in the minimal form of representation is that it does not contain two consecutive units. Thus, the code combination 11 is forbidden for the Fibonacci code in the minimal form of representation [4].

3. THE METHOD OF NOISE IMMUNITY OF THE FIBONACCI COUNTING

Based on the Fibonacci number system, the method of counting possesses increased high speed, noise immunity and simplicity [1]. The advantage of the method is the absence of operations of the Fibonacci number transition from the minimal form to the maximal form and back, as is the case in the number of existing methods for counting Fibonacci numbers, which increases counting speed [1], [2].

The working principle of the noise immune Fibonacci counter is based on finding two bits with two 0 in the Fibonacci number, when counting from right to left, and then setting the first bit to 1, while converting the low-order bits to zero [5], [14]. For example, if the Fibonacci number 01001000 in the minimal form is 26, then, in accordance with the proposed method, the next number equal to 01001001 is 27.

The method of the noise immune counting of Fibonacci numbers consists of the following sequential steps:

1. The counting begins with code combinations containing zeros.
2. The lower-order bit of the code combination containing 0 is converted to 1.
3. Then 1 is converted to 0, and 1 is put in front of 0.
4. The lower-order bit of those containing two consecutive zeros, with the counting from right to left, 0 converted to 1. The lower-order bits, standing to the right of 1, are converted to 0.
5. If there is one zero in front of the high-order bit unit of the code combination, and there are not two zeros standing next to each other, then the zero before the high-order unit is converted to 1. All other low-order bits convert to 0.
6. The counting goes until the Fibonacci code combination appears, in which between units there is only one zero, and in front of the high-order bit 1, there is not more than one zero.
7. The appearance of two consecutive units in the Fibonacci code combination is a sign of an error.

For example, the 5-digit counting using the above method is shown in Table 1. The counting in this case begins with the initial code combination 00000, consisting of bits containing zeros. Then, the low-order bit is converted to 1. As a result, the combination 00001 is obtained. Since only zeros are in front of this 1, it is converted to 0 in the next step of the method, and 1 is put in front of the resulting 0, which results in the code combination 00010. In front of 1 there are only zeros, it follows that in the next step of the method 1 is converted to 0, and 0 in front is converted to 1, which results in the code combination 00100. Since in the lower bits – zero, then in

the next step of the method 1 is converted to 0, which results in the code combination 00101.

The presence of one zero between the zero bit and second bit results in the next 1 entered to the fourth bit. In this case, all bits to the right of the third bit reset to 0, which results in the code combination 01000. Then the counting process continues until there is one zero between the units in the Fibonacci number, and zero or one in the most significant bit is 10101.

The method allows applying the simple and effective algorithm of detecting errors such as transitions 0 to 1, since the method is based on the sign of the absence of two or more adjacent 1. Based on this method, the noise immune, high-speed Fibonacci counter is implemented [14]. Figure 1 shows the method of noise immune counting of Fibonacci numbers.

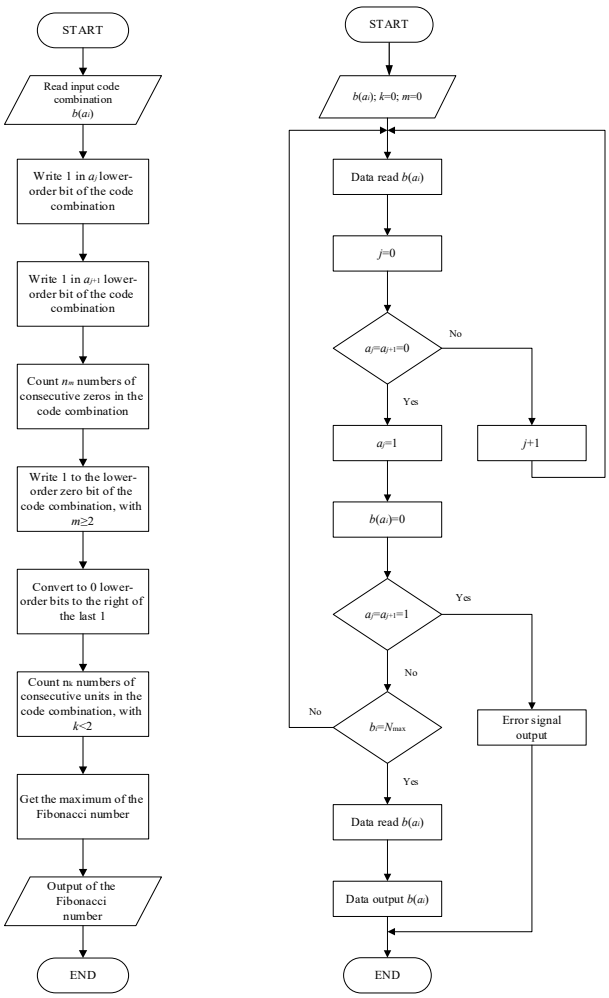

Fig. 1. (a) General block diagram of noise immune counting of Fibonacci numbers;
(b) Block scheme of noise immune counting of Fibonacci numbers, where $b(a_j) = a_j \ldots a_0$ – Fibonacci code sequence; m – a number of zeros in the code combination;
k – a number of units in the code combination; N_{max} – maximal of the Fibonacci number.

4. EVALUATION OF NOISE IMMUNITY OF THE FIBONACCI CODE

The share of errors detected by the noise immune code is determined by the equation (1) [1]:

$$D = 1 - \frac{M}{N}, \qquad (1)$$

where M is the number of allowed code combinations; N is the number of all code combinations equal to 2^n.

Table 2 shows the share of detected errors D of the Fibonacci code for n = 10, 15, 20, 25, 30, 40, where the n is code length.

Table 2

The Share of Detected Errors *D* of the Fibonacci Code

n	*D*	*n*	*D*
10	0.859	25	0.994
15	0.951	30	0.998
20	0.983	40	0.999

The share of the detected errors of the Fibonacci code from the code length n is shown in Fig. 2.

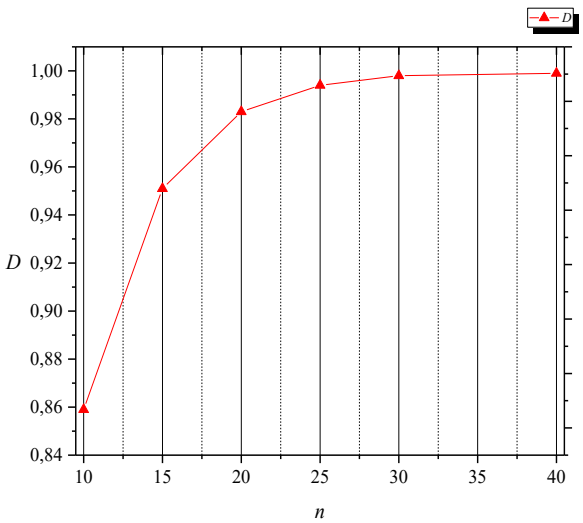

Fig. 2. The share of the detected errors by the Fibonacci code if different code lengths n are used.

From Fig. 2 it follows that the share of the detected errors by the Fibonacci code with increasing n tends to 1.

5. DEVELOPMENT OF HIGH-SPEED NOISE IMMUNE COUNTER WITH FRACTAL DECODING DEVICE

The functional diagram of the high-speed counter based on the minimal form of the Fibonacci code with the fractal decoder device for $n = 5$ is shown in Fig. 3. The Fibonacci fractal decoder device consists of switching device 1, containing $2n$ elements AND 1.1 - AND 1.10, a decoding block 2 consisting of elements NOT 2.1, OR 2.1, NOR 2.2, OR 2.3. The structure of the fractal decoder consists of linear decoders: Decoder 1 (DC1) and Decoder 2 (DC2). The linear decoder DC1 consists of n-1 inputs and n outputs. The linear decoder DC2 consists of n inputs and n-2 outputs. The structure of high-speed noise immune pulse counter consists of control unit 3, containing the element OR 3.1 and elements AND 3.1 - AND 3.4. The disposition unit 4 consists of elements AND 4.1 - AND 4.4 with inverters at the inputs. The analysis unit 5 consists of elements AND 5.1 - AND 5.4. The register 6 contains flip-flops TT 6.1 - TT 6.5 and elements AND 6.1 - AND 6.5. The counter zero-setting unit 7 consists of the elements OR 7.1 - OR 7.4. The high-speed pulse counter based on Fibonacci codes works as follows. In the initial position, flip-flop of register 6 is set to zero. The first clock pulse sets the first flip-flop TT 6.1 to 1 and prohibits the passage of signal to the flip-flops TT 6.2 - TT 6.5.

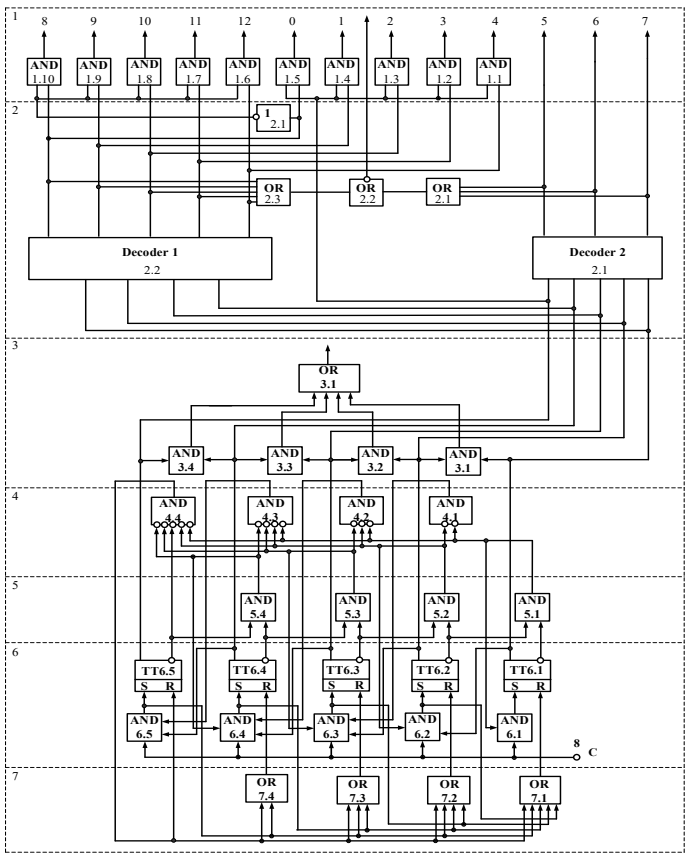

Fig. 3. Functional diagram of the high-speed noise immune counter with the fractal decoder device.

The second clock pulse sets the first flip-flop TT 6.2 to 1 by the enabling signal from the direct output of the first flip-flop TT 6.1. The flip-flop TT 6.1 is set to 0 by the counter zero-setting unit 7.

The third clock pulse sets to 1 the third flip-flop TT 6.3, since the enabling signals are supplied from the disposition unit 4, the analysis unit 5 and the second flip-flop TT 6.2. The first and second flip-flops TT 6.1 - TT 6.2 are set to zero by the counter zero-setting unit 7.

The fourth clock pulse sets the flip-flop TT 6.1 to 1, while the flip-flop TT 6.3 is also in 1 by signal from the disposition unit 4. This procedure is repeated until the code combination is obtained, in which there is one zero between two units [14]. The high-speed Fibonacci counter operates in accordance with Table 1.

In the initial position, all flip-flops of register 6 are set to zero, which corresponds to code combination 00000. The first clock pulse sets the flip-flop TT 6.1 to 1, through the first input of the element AND 6.1, to which the signal arrives from the bus 8. The signal 1 from the output of the element AND 5.1 of the analysis unit 5 arrives at the second input of the element AND 6.1, thus the following code combination 00001 is obtained.

The flip-flops TT 6.2 - TT 6.5 are set to zero, since zero signals from the outputs of other elements arrive at the inputs of the elements AND 6.2 - AND 6.5. The presence of 1 in the low-order bit and zeros in the remaining bits gives the possibility of recording 1 to the second bit.

The second clock pulse sets the flip-flop TT 6.2 to 1. The signal 1 from the direct output of the flip-flop TT 6.1 arrives at the first input of the element AND 6.2. The signal 1 from the output of the element AND 5.2 of the analysis unit 5 arrives at the third input of the element AND 6.2. Two ones from the inverse outputs of the flip-flops TT 6.1, TT 6.3 of the register 6 arrive at the inputs of the element AND 5.2. Zero signals from the elements AND 6.3 - AND 6.5 of the register 6 and the element AND 4.4 of the disposition unit arrive at the inputs of the OR 7.1 element, since the flip-flops TT 6.3 - TT 6.5 are set to zero. As a result, the single signal appears at the direct output of the flip-flop TT 6.2. Thus, the code combination 00010 is obtained.

The third clock pulse sets the flip-flop TT 6.3 to 1. The signal from the direct output of the flip-flop TT 6.2 arrives at the second input of the element AND 6.3. The signal from the output of the element AND 5.3 of the analysis unit arrives at the fourth input of the element AND 6.3, since 1 arrives at the input AND 5.3 from the inverse outputs of the flip-flops TT 6.3 and TT 6.4. The signal 1 from the output of the element AND 4.1 of the disposition unit 4 arrives at the first input of the element AND 6.3, since the zero signal arrives at the first input AND 6.2, which is the output of the direct flip-flop TT 6.1. As a result of the inverse outputs of the flip-flops TT 6.1 and TT 6.2, the zero signal arrives at the element AND 5.1 of the analysis unit 5. From the output of the element AND 5.1, the signal arrives at the elements NOT, after the signal arrives at the element AND 4.1. At the same time, from the output of the element AND 6.3, the signal 1 arrives at the first input of the element OR 7.2 and from its output at the second input of the element OR 7.1 of the counter zero-setting unit 7, the output of which is connected to the reset input of flip-flop TT 6.1. Thus, the flip-flops TT 6.1 and TT 6.2 are set to zero. Thus, the code combination 00100 is obtained [14].

The fourth clock pulse sets the flip-flops TT 6.1 and TT 6.3 of the register 6 to 1. The signal 1 from the bus 8 arrives at the first input of the element AND 6.1. The signal 1 from the output of the element AND 5.1 of the analysis unit 5 arrives at the second input of the element AND 6.1. Thus, the flip-flop TT 6.1 is set to 1. The signal 1 from the inverse output of the flip-flop TT 6.1 arrives at the first input of the element AND 5.1 of the analysis unit 5.

Zero arrives at the second input of the element AND 5.1 from the inverse output of the flip-flop TT 6.2. The signal 0 from the TT 6.1 arrives at the first input of the element AND 5.1. The signal 0 from the output of the element AND 5.1 arrives at the first input of the element NOT of the disposition unit 4.

Zero arrives at the second input of the element NOT of the disposition unit 4 from the output of the element AND 5.2, after which the signal arrives at the element AND 4.1 from the output of the element AND 4.1. The signal of 1 arrives at the first input of the element AND 6.3, as the input elements AND 4.1 are inverters. The flip-flop TT 6.2 is set to 0 by the signal from the output of the element AND 5.2. Thus, the code combination 00101 is obtained. The logic waveforms of the operation of each of the incoming blocks in the device are shown in Fig. 4.

The counting continues until the maximum of the Fibonacci number 10101 is obtained. After the appearance of the maximum Fibonacci number, the counting ends, the register is set to 0, after which a new counting cycle begins [14].

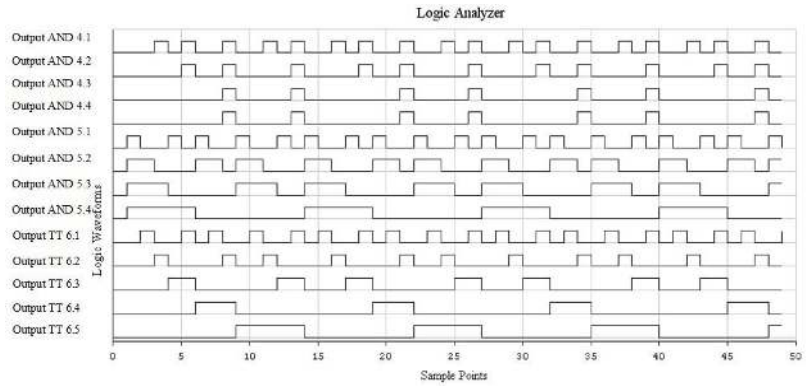

Fig. 4. The logic waveforms of the high-speed counter based on the minimal form of the Fibonacci code.

The device contains the 2-input elements AND 3.1 - AND 3.4 of the control unit 3 for analysing the correct operation of the counter, the outputs of which are connected by the 4-input element OR 3.1, and the inputs are connected to the direct outputs of two adjacent flip-flops. If an error occurs as a result of counting, which is characterised by the appearance of two adjacent units in the Fibonacci bits, then signal 1 appears at one of the elements AND 3.1 - AND 3.4 and an error signal appears at the output of the element OR 3.1 [14].

The presence of parallel chains of transfer signals in the disposition unit 4 and the counter zero-setting unit 7 significantly increases the speed of the Fibonacci counter, and the use of the code Fibonacci based on the device determines its advantage over binary counters by the noise immunity criterion.

The decoding using the fractal decoder device is as follows: 4 low-order bits of the first five Fibonacci bits are repeated in five numbers at the end of Table 1. The difference between these groups of bits is the presence of zero or one in the high-order bit, which characterises fractal structure of Fibonacci code [15].

At the initial position, one of the code combinations shown in Table 1 goes to the inputs of the first and second decoder DC 2.1, DC 2.2. The first decoder DC 2.1 decodes the code combinations corresponding to the numbers 0–4 and 8–12 in Table 1, the second decoder DC 2.2 decodes the code combinations corresponding to the numbers 5–7 in Table 1. When the combination of 0–4 or 8–12 arrives at the DC1, signal 1 appears at one of the elements AND 1.1–AND 1.10 of switching device 1.

If the counter is in state 00001, which corresponds to signal 1 at the output of the element AND 1.4 of switching device 1, all other outputs of switching device 1 are set to 0, which is the result of decoding. Other code combinations are decoded by the usual method [15]. If, as a result of decoding, an error occurs, which is characterised by the appearance of two units that are next to each other in the Fibonacci bits, then signal 1 arrives at the element OR 2.2, which indicates the presence of errors. The operation of noise immune high-speed Fibonacci counter with the fractal decoder device is simulated in the NI Multisim simulation and analysis system.

6. CONCLUSIONS

In this paper, the method of noise immunity of the Fibonacci counting in the minimal form of presentation has been improved. The authors of the paper have also developed the noise immune pulse counter with fractal decoding based on the minimal form of the Fibonacci code. This device possesses a homogeneous structure, as well as increased noise immunity due to the detection of bit errors in the operation. The operation of the noise immune high-speed Fibonacci counter with the fractal decoder device has been simulated in the NI Multisim software. The proposed noise immune pulse counter can be used in high-speed telecommunication systems for the transmission of information in very noisy channels. The use of Fibonacci codes in telecommunication systems for collecting and transmitting information significantly increases the noise immunity and speed of information transfer. The device such as the Fibonacci counter with decoding also refers to automation and computing devices and can be used in systems of discrete information processing as a noise immune counter, pulse distributor and noise immune information coding device. The goal of the research is achieved through the introduction of new design features that provide the decoding of the counter. The research will be continued in the future with the implementation of the Fibonacci counter using the fractal decoder device in the field-programmable gate array.

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FIBONAČI SKAITĪTĀJA TROKŠŅNOTURĪBA AR FRAKTĀLU DEKODĒTĀJA IERĪCI TELEKOMUNIKĀCIJU SISTĒMĀM

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K o p s a v i l k u m s

Pētījumā parādīta uzlabota metode, kas domāta trokšņnoturīgai Fibonači skaitīšanai minimālā reprezentācijas formā. Metode tika testēta un izpētīta izveidotajā trokšņnoturīgā impulsu skaitītājā, kurā pamatā ir minimālas formas Fibonači kods ar fraktālu dekodētāja ierīci. Piedāvātajai ierīcei, kas ir simulēta NI Multisim programmatūrā, piemīt homogēna struktūra, paaugstināta trokšņnoturība, veiktspēja, kā arī bitu kļūdu uztveršana darbības procesā.

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