Noise Modeling for RF CMOS Circuit Simulation

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Invited Paper

***Abstract*—The RF noise in 0.18-μm CMOS technology has been measured and modeled. In contrast to some other groups, we find only a moderate enhancement of the drain current noise for short-channel MOSFETs. The gate current noise on the other hand is more significantly enhanced, which is explained by the effects of the gate resistance. The experimental results are modeled with a non-quasi-static RF model, based on channel segmentation, which is capable of predicting both drain and gate current noise accurately. Experimental evidence is shown for two additional noise mechanisms: 1) avalanche noise associated with the avalanche current from drain to bulk and 2) shot noise in the direct-tunneling gate leakage current. Additionally, we show low-frequency noise measurements, which strongly point toward an explanation of the $1/f$ noise based on carrier trapping, not only in n-channel MOSFETs, but also in p-channel MOSFETs.**

***Index Terms*—$1/f$ noise, avalanche noise, compact modeling, flicker noise, induced flicker noise, induced gate noise, MOSFET, noise, RF CMOS, shot noise, thermal noise.**

I. Introduction

THE EVER-CONTINUING downscaling of CMOS technologies has resulted in a strong improvement in the RF performance of MOS devices [1], [2]. Consequently, CMOS has become a viable option for analog RF applications and RF systems-on-chip. For the application of modern CMOS technologies in low-noise RF circuits, accurate modeling of noise is a prerequisite.

In MOSFETs, there are two major sources of noise: $1/f$ noise and thermal noise. The $1/f$ noise in the drain current of a MOSFET is not only important in analog circuits (e.g., operational amplifiers), but also in RF circuits, where it increases the phase noise of, e.g., voltage-controlled oscillators (VCOs). In Section II, we will briefly discuss the issue of $1/f$ noise modeling for circuit simulation.

Next, in Section III, we turn to the main topic of this paper, which is thermal noise in MOSFETs. Thermal noise is due to the random thermal motion of charge carriers. It not only manifests itself in the drain current noise spectrum, but, due to the capacitive coupling between channel and gate, also in the gate current noise spectrum. The latter effect is known as "induced gate noise." In Section III, we will present a large number of measurements and a model that is able to *predict* the thermal noise in the drain current, induced gate noise, as well as their correlation.

Finally, in Section IV, the noise mechanisms that will play a role in MOS devices with leaky gate dielectrics are briefly reviewed.

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II. $1/f$ Noise

A. Introduction to $1/f$ Noise

At low frequencies, $1/f$ noise is the dominant source of noise in MOS devices. Here, we use the term "$1/f$ noise" for all low-frequency noise in excess of the thermal noise background. Typically, $1/f$ noise in MOSFETs has a spectrum with a slope that varies between ~ -0.7 and ~ -1.3 on a double-log plot.

The MOSFET $1/f$ noise does not only have an impact on low-frequency applications. Due to upconversion, it also has a serious impact on RF CMOS circuits such as VCOs, where it causes a significant increase of the phase noise [3]. Therefore, a good $1/f$ noise model is an important ingredient of an RF design kit.

Many different theories have been proposed to explain the physical origin of $1/f$ noise in MOSFETs [4], [5]. These can be categorized in three major types.

1) Carrier Number Fluctuation Theory: In this theory, originally due to McWorther [6], the $1/f$ noise is attributed to the trapping and detrapping of charge carriers in traps located in the gate dielectric. Every single trap leads to a Lorentzian noise power spectrum. In case of a uniform spatial trap distribution, the Lorentzian spectra add up to give a $1/f$ spectrum. The carrier number fluctuation theory has been successful in modeling the observed $1/f$ noise in n-channel devices, where the input-referred $1/f$ noise, defined by

$$S_{\mathrm{Vgate}} \equiv \frac{S_{I_{\mathrm{D}}}}{g_{\mathrm{m}}^2} \tag{1}$$

is almost independent of V_{GS}. In the above equation, $S_{I_{\mathrm{D}}}$ is the drain current noise spectral density and g_{m} the transconductance.

2) Mobility Fluctuation Theory: The Hooge model, on the other hand [7], attributes the $1/f$ noise to bulk mobility fluctuations caused by phonon scattering. In contrast to the carrier number fluctuation theory, the Hooge model is more suc-

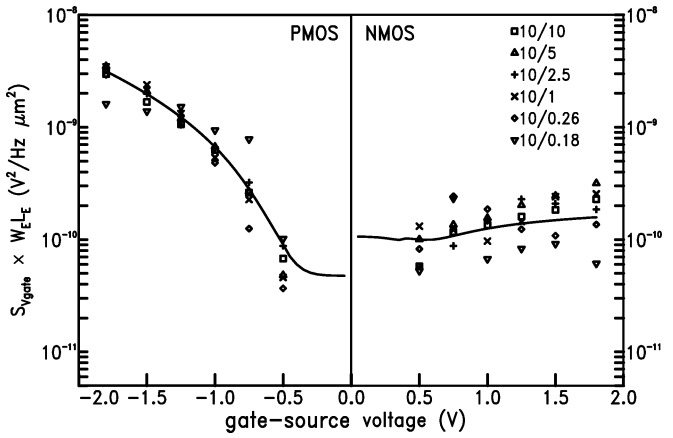

Fig. 1. Input-referred $1/f$ noise in 0.18-μm technology, multiplied by the effective device area, plotted versus gate–source voltage for several geometries, and for n- and p-channels. Note the striking difference in $V_{\rm GS}$ dependence for n-channels and p-channels. The unified $1/f$ noise model is used here to fit the data. For clarity, only the model curves for the 10/10 devices are shown. Curves for the other geometries are very similar.

cessful in describing the observed $1/f$ noise in p-channel devices, where the input-referred $1/f$ noise is found to be strongly dependent on $V_{\rm GS}$.

3) Unified $1/f$ Noise Model: Recently, a unified model has been proposed that can describe both the measured $1/f$ noise characteristics of n- and p-channel devices using a single model [8]–[11]. The unified model is *not,* as one may think, a combination of the number fluctuation theory and the Hooge mobility fluctuation theory. Instead, it extends the carrier number fluctuation theory to include the Coulomb scattering of free charge carriers at trapped oxide charge. As a consequence, not only the *number* of charge carriers in the channel, but also their mobility fluctuates. Because these mobility fluctuations have the same origin as the number fluctuations (i.e., trapping and detrapping of charge carriers in the oxide), they are correlated. The unified model is very successful in describing the measured noise in both n-channel and p-channel devices (see Fig. 1) and is therefore called "unified $1/f$ noise model." The unified $1/f$ noise model is used in many of today's compact MOSFET models, such as BSIM3, BSIM4, MOS Model 9, and MOS Model 11. Vandamme and Vandamme, however, have argued that the Coulomb scattering effect is far too weak to explain the p-channel data [12].

Although there is a growing consensus in the literature about the explanation of $1/f$ noise in n-channel MOSFETs in terms of carrier number fluctuations, a lot of controversy still exists about the origin of $1/f$ noise in p-channel devices. In this work, we will show experimental evidence that strongly supports the picture that $1/f$ noise in p-channels, just like in n-channels, arises from trapping and detrapping of charge carriers in the gate oxide. These experiments are difficult to reconcile with explanations in terms of bulk mobility fluctuations.

B. Experimental Results

Low-frequency noise measurements in the frequency range from 10 Hz to 10 kHz have all been carried out on-wafer with a BTA 9812A noise measurement system. The devices were measured in saturation ($V_{\rm ds} = V_{\rm dd} = 1.8$ V) as a function of the gate–source voltage drive $V_{\rm GS}$. The devices discussed here were all manufactured in the same 0.18-μm CMOS technology that is used in our study of thermal noise (see Section III). We focus here on the p-channel devices, which are of the surface-channel type.

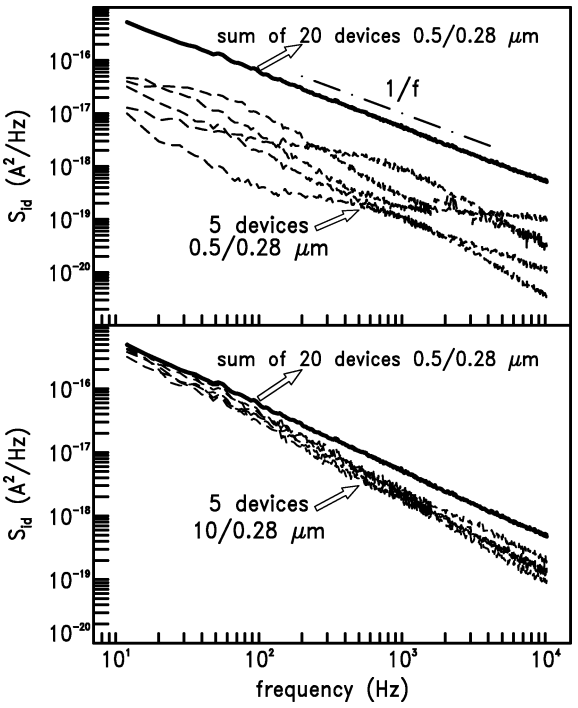

Fig. 2. (Top) dashed lines are examples of low-frequency noise spectra for a number of 0.5/0.28-μm p-channel devices with the same layout, but located on different positions on the wafer. The thick solid line is the sum of 20 of these spectra. The dash–dotted line gives $1/f$ slope for comparison. (Bottom) dashed lines are examples of low-frequency noise spectra for a number of 10/0.28-μm devices with the same layout, but located on different positions on the wafer. Thick solid line is the same as in upper frame.

In the upper frame of Fig. 2, the low-frequency noise spectra of several 0.5/0.28-μm p-channel devices with the same layout, but located on different positions on the wafer, are shown (the notation 0.5/0.28 μm stands for $W = 0.5$ μm and $L = 0.28$ μm). We observe a rather large sample-to-sample spread. Moreover, the shape of the spectra also varies strongly from sample to sample, and strongly deviates from the $1/f$ shape. Instead, distinct humps are observed.

Next, when we add up the noise spectra of 20 of such 0.5/0.28-μm devices, located on different positions on our wafer. The resulting noise spectrum is very close to $1/f$.

It is now interesting to compare this sum of 20 individual spectra of $W = 0.5$ μm devices with the spectrum of a single device with the same channel length, but with a width of $W = 20\times 0.5 = 10$ μm. This comparison is shown in the lower frame of Fig. 2. For these wider devices, compared to the narrow-channel case, the relative sample-to-sample spread is much less, the shape of the spectra varies much less, and the spectra are much closer to $1/f$. Moreover, we see that the summed spectra of our 20 narrow devices agree quite well with the spectra measured for the wide devices, in particular in the range from 10 to 1000 Hz.

C. Discussion

The above experiments clearly show that the microscopic noise sources causing $1/f$-like noise in p-channel MOSFETs do *not* have a $1/f$ spectrum. Moreover, the experiments reveal that the $1/f$ spectrum, as observed in large-area p-channel devices, is the sum of many differently shaped spectra, which are very similar to the Lorentzian noise spectra which are thought to be the microscopic noise sources in both the number fluctuation theory and the unified noise model. The experimental results, shown here for p-channels, are very similar to results already known for n-channels [13]. Therefore, we believe that an explanation of MOSFET $1/f$ noise must be based on number fluctuation theory for n- as well as for p-channels. The Hooge bulk mobility fluctuation model, on the other hand, seems to be difficult to reconcile with the experiments presented here, because it does not explain the shape of the narrow-channel noise spectra, as well as their large statistical spread.

Besides the similarities between n- and p-channel $1/f$ noise, emphasized above, there are also differences between the two. For instance, the $V_{\rm GS}$ dependence is strikingly different (see Fig. 1) and so is the oxide thickness dependence [14]. Therefore, it is evident that the number fluctuation theory must be extended to achieve a good description for both n- and p-channels. Thus, either the arguments of [12] against the unified noise model must be proven wrong or an alternative extension of the number fluctuation theory should be devised. In this context, an interesting direction is found in [15], where it is shown that the inclusion of inversion layer quantization yields the experimentally observed $V_{\rm GS}$ dependence of the $1/f$ noise both for n- and for p-channels. Another option is to take into account the dependence of trap density on Fermi-level, as in [16]. This dependence is often neglected in compact models based on number fluctuation theory.

III. Thermal Noise

A. Introduction to Thermal Noise

At RF frequencies, the MOSFET $1/f$ noise becomes negligible and thermal noise is the dominant source of noise. Thermal noise of deep-submicrometer MOSFETs has received considerable attention lately, which is mainly triggered by publications that report a severe enhancement of the thermal noise with respect to long-channel theory [17]–[21]. In the earliest of these publications [17], thermal noise was found to be enhanced by a factor up to 12 in n-channel devices with 0.7-μm gate length and hot electrons were proposed to explain these results. More recently, Klein [18], [19] reported very similar enhancements of the drain current thermal noise in devices with 0.65-μm gate length and proposed a model which invokes heating of the charge carriers in the inversion channel to explain the experiments. For the induced gate noise, an even more dramatic enhancement factor as large as 30 was found by Knoblinger [20] for a 0.25-μm gate-length n-channel MOSFET.

Evidently, the reported noise enhancements would seriously limit the viability of RF CMOS and a detailed study is called for. Therefore, in this paper, we perform an extensive study of the RF noise in 0.18-μm RF CMOS technology. We will present a large number of experimental results and an RF MOSFET model that is capable of *predicting* the drain current noise $S_{I_{\rm D}}$, the gate current noise $S_{I_{\rm G}}$, as well as their correlation coefficient c (for a precise definition of these quantities, please refer to [22] and [23]). This work forms an extension to an earlier study [24] that focused on drain current thermal noise only, and that was carried at much lower frequency (248 MHz) than the present study (1 GHz $< f <$ 10 GHz).

B. Drain Current Thermal Noise Model

The drain current thermal noise in MOSFETs is calculated by the well-known Klaassen–Prins equation [25]

$$S_{I_{\rm D}}(f) = \frac{1}{I_{\rm D}\cdot L_{\rm elec}^2}\cdot\int_{V_{\rm SB}}^{V_{\rm DB}} 4\cdot k_{\rm B}\cdot T\cdot g(V)^2\cdot {\rm d}V \qquad (2)$$

where $L_{\rm elec}$

$$L_{\rm elec} = L_{\rm E} - \Delta L_{\rm CLM} \qquad (3)$$

is the electrical channel length of the MOSFET which includes the effect of channel length modulation $\Delta L_{\rm CLM}$, and $L_{\rm E}$ is the MOSFET effective channel length. The Klaassen–Prins equation formula was derived using the Langevin method. An alternative derivation, which is essentially the same but somewhat more transparent, has been given by Tsividis [26]. The underlying assumptions are that: 1) the charge carriers are in thermal equilibrium so that the voltage noise spectral density of a channel segment ${\rm d}x$ is given by the Nyquist expression $4k_{\rm B}T\cdot{\rm d}x/g(V)$, where $g(V)$ is the local channel conductance and 2) the noise sources of different channel segments are uncorrelated.

We evaluate (2) using our recently developed compact MOS model, named MOS Model 11 [27], [28]. This public-domain compact MOS model is based on a C^∞ continuous description of the surface potential throughout all MOSFET operating regions, including the increasingly important moderate inversion region. The details of the derivation of $S_{I_{\rm D}}$ are found in the Appendix.

The effect of *velocity saturation* in the channel region is included via the local channel conductance $g(V)$. The expression for velocity saturation is different for n- and p-channels, resulting also in different expressions for $S_{I_{\rm D}}$.

It was argued recently that the possible noise contribution of the *pinch-off region* is negligible [29]. In our model we also neglect this contribution, which will be corroborated by the experimental observation (cf. Section III-E1 and Fig. 12) that there is hardly any dependence of the noise on $V_{\rm DS}$ beyond the saturation voltage. What we do take into account, again in agreement with [29], is *channel length modulation*, i.e., the effect of the length of the pinch-off region on the electrical channel length $L_{\rm elec}$.

Finally, note that, in the weak inversion regime, the model expressions reduce to the shot noise expression $2\cdot q\cdot I_{\rm DS}$, as expected (see the Appendix).

C. Segmentation Model

1) Model Description: The analysis of our measurements is based on the nonquasi-static RF MOSFET model displayed in

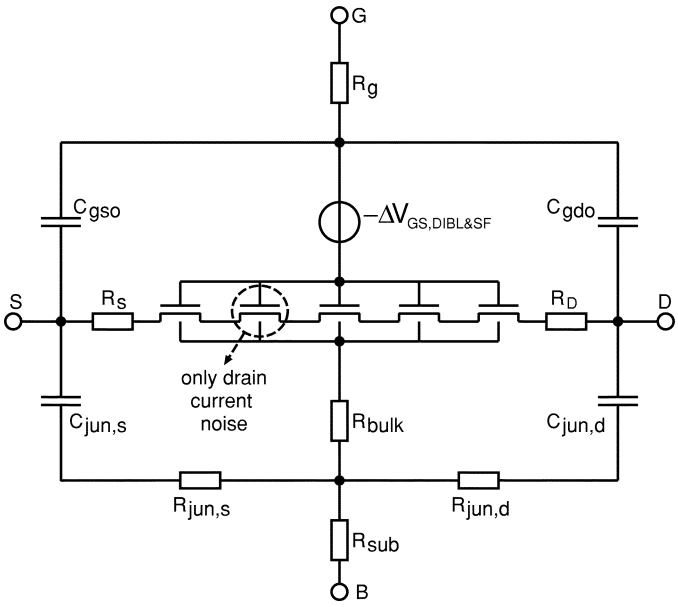

Fig. 3. Nonquasi-static RF CMOS model, consisting of five channel segments, and parasitic resistances and capacitances. Some short-channel effects are incorporated using the voltage-controlled voltage source in the gate lead. Every channel segment is equipped with a drain current noise source only. The phenomenon of induced gate noise comes out of the model naturally.

Fig. 3. The model is based on the concept of channel segmentation [26], [30], [31], where every channel segment is modeled by MOS Model 11. We stress however that the noise modeling approach described in this paper is not restricted to MOS Model 11, but can be applied to any quasi-static MOSFET model, e.g., BSIM3 or BSIM4 [33]. The ability of the channel segmentation model to describe the measured Y-parameters even in the NQS regime has been demonstrated in [31] for MOS Model 9, and in [32] for MOS Model 11.

In order to describe the RF noise correctly, every quasi-static channel segment is equipped with a drain current noise source only, i.e., the segments do *not* have a gate current noise source. The drain current noise of each channel segment is given by the equation discussed in the previous section, and the noise sources of the different channel segments are mutually uncorrelated.

The phenomenon of induced gate noise originates from this segmentation model naturally due to the distributed gate capacitance: because the noise voltages at the *internal* nodes of this compound model are nonzero, a noise current $\propto f$ flows from the channel into the gate terminal, corresponding to a noise current spectral density $S_{I_{\rm G}} \propto f^2$. In a single-segment model, in contrast, the induced gate noise does not come out naturally, because, by definition, the *external* gate, source, and drain nodes have zero noise voltage [22] when the noise is expressed in terms of $S_{I_{\rm D}}$, $S_{I_{\rm G}}$, and their correlation coefficient c. Therefore, when one only has a current noise source between the source and drain, zero noise current in the gate lead results. Thus, in single-segment or lumped models such as MOS Model 9, MOS Model 11, and BSIM, the induced gate noise has been added separately. In the present study, however, we have explicitly turned off the induced gate noise of the MOS Model 11 segments, so that they have a drain current noise source only.

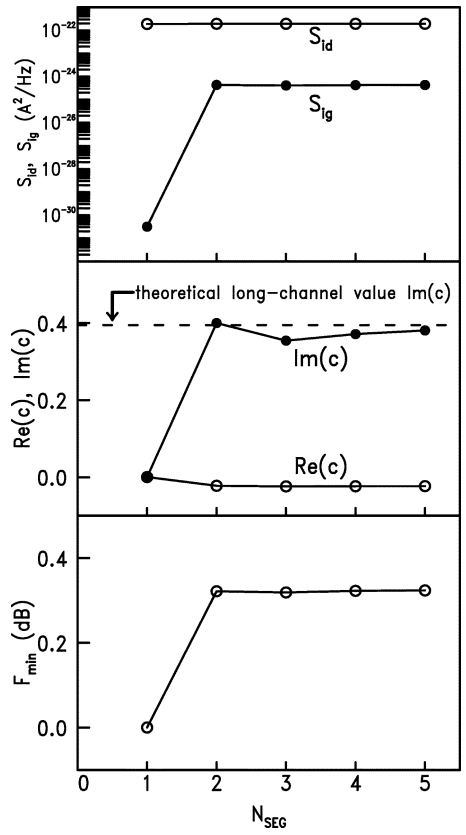

Fig. 4. Effect of the number of channel segments on the noise at $f = 0.1$ GHz for $L = 2$ μm. (Top) drain current noise and gate current noise spectral density. (Middle) real and imaginary parts of the correlation coefficient. (Bottom) minimum noise figure.

The effect of segmentation is illustrated in Fig. 4, where the drain current thermal noise ($S_{I_{\rm D}}$), the induced gate current noise ($S_{I_{\rm G}}$), and their complex correlation coefficient c are plotted as a function of the number of channel segments. It is seen that $S_{I_{\rm D}}$ is hardly dependent on $N_{\rm seg}$, which confirms the correctness of both the drain current noise model and the segmentation process. The induced gate noise $S_{I_{\rm G}}$, on the other hand, rapidly converges from almost 0 for a single-segment model to a nearly constant value for $N_{\rm seg} \geq 2$. The same holds for the correlation coefficient, which rapidly converges toward the theoretical long-channel limit $0.395j$ [23] and the minimum noise figure. In the remainder of this work, we keep the number of channel segments fixed to five, because this gives a good description of the MOSFET Y-parameters as well as the noise [32].

In contrast to expressions for $S_{I_{\rm G}}$ currently used in circuit design models [33], [27], our model has the advantages that: 1) it is not only valid in saturation, but in all MOSFET operating regimes; 2) it does not need correlated noise sources; 3) it automatically accounts for short-channel effects in $S_{I_{\rm G}}$ through the short-channel effects incorporated in the $S_{I_{\rm D}}$ expression; and 4) it is valid even in the NQS regime. Further note that there are *no* adjustable parameters to fit the noise data: all model parameters follow from dc and C–V measurements, except for the bulk resistance parameters, which follow from off-state Y-parameters (cf. Section III-C5).

2) Induced Flicker Noise: In the previous section, we saw how thermal noise ($\propto f^0$) in the inversion channel leads to in-

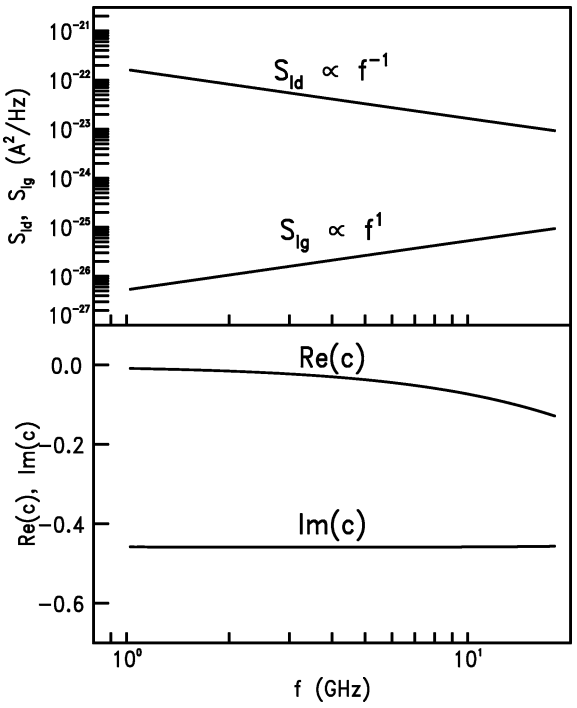

Fig. 5. Demonstration of the effect called "induced flicker noise" in a 0.18-μm n-channel biased at $V_{\rm GS} = 1$ V, and $V_{\rm DS} = 1.8$ V. All noise contributions, except the MOSFET $1/f$ noise, have been switched off in the model. (Top) it is seen that this leads to "induced flicker noise" in the gate current, proportional to f. (Bottom) the corresponding complex correlation coefficient is shown.

duced gate noise ($\propto f^2$) by the capacitive coupling between the channel and gate. It is instructive to note that, by the very same mechanism, $1/f$ or flicker noise will be induced in the gate terminal as well. In this case, the noise sources in the inversion channel are proportional to f^{-1}, and therefore the noise induced in the gate terminal is expected to be proportional to f. We propose to call this phenomenon "induced flicker noise" to distinguish it from the usual "induced gate noise" which is normally associated with thermal noise. (The term "induced $1/f$ noise" must be avoided because it would suggest the wrong frequency dependence of this type of noise.)

Just like "induced gate noise" of thermal origin, "induced flicker noise" originates from our segmentation approach naturally. This is illustrated in Fig. 5, which shows the results of a calculation in which the MOSFET segments only have $1/f$ noise. As expected, the "induced flicker noise" shows the expected $\propto f$ behavior. The correlation coefficient proves to be $-0.45j$ for this 0.18-μm n-channel MOSFET under consideration.

In practice, the phenomenon of "induced flicker noise" is not very important, because at frequencies so low that $1/f$ noise is dominant over thermal noise the capacitive coupling between channel and gate is extremely low. At those frequencies, the resulting "induced flicker noise" will be much too low to measure. At higher frequencies, it will be overwhelmed by traditional "induced gate noise" of thermal origin. Indeed, we will see in our analysis that "induced flicker noise" only contributes a few percent to the measured gate current noise at $f = 3$ GHz.

3) Gate Resistance Noise: A noise contribution that may not be overlooked is the thermal noise of the gate resistance [34], [35]. In our compound model the effects of this noise source are automatically accounted for by the circuit simulator. It is instructive, however, to consider these effects here separately.

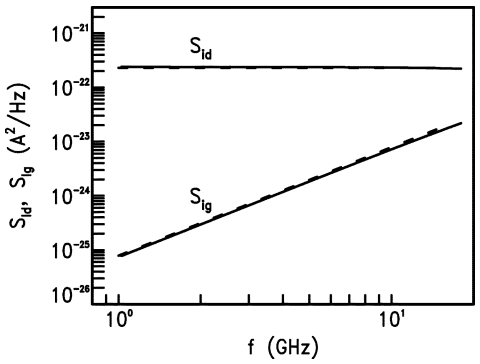

Fig. 6. Solid lines: noise contributions of the gate resistance, as simulated using the compound model of Fig. 3, with all other noise contributions switched off. Not only a white drain current noise contribution, but also a f^2 gate current noise contribution emanates from the compound model. The dashed lines are calculated with the approximate equations (4) and (5). The device length is $L = 0.18$ μm.

First, the voltage noise across the gate resistance is, like any other ac signal, amplified to the drain, leading to an additional drain current noise

$$S_{I_{\rm D}} = 4k_{\rm B}TR_{\rm g}g_{\rm m}^2. \tag{4}$$

What was not recognized in [34] and [35] is that the voltage noise across the gate resistance also gives rise to a noise current in the gate, in first-order approximation given by

$$S_{I_{\rm G}} = 4k_{\rm B}TR_{\rm g}\omega^2C_{\rm gg}^2. \tag{5}$$

This will turn out to be a major contributor to the measured gate current noise in short-channel devices. Note that it has exactly the same frequency dependence ($\propto f^2$) as the induced gate noise from the intrinsic device. Of course, the contributions of the gate resistance to drain current and gate current noise are correlated. The correlation coefficient is purely imaginary: $c = 1.0j$.

When the gate resistance, as in our model, is accounted for as a separate element in a compound model, all these effects are accounted for naturally by the circuit simulator, which contains thermal noise sources for all explicit resistors. This is shown in Fig. 6, where we have performed a simulation of a 0.18-μm n-channel MOSFET with all noise sources, except the gate resistance noise, set to zero. The simulation results (solid lines) are shown to agree well with (4) and (5), given by the dashed lines.

In our model, the gate resistance consists of several parts: the resistance of the vias between metal1 and silicided polysilicon, the effective resistance of the silicide, and the contact resistance between silicide and polysilicon [36]. For a single polysilicon gate finger, connected on both sides, we have

$$R_{\rm gate} = \frac{1}{12}\rho_{\square,\,\rm sil}\frac{W}{L} + \frac{1}{2}\rho_{\square,\,\rm sil}\frac{W_{\rm ext}}{L} + \frac{1}{2}\frac{R_{\rm via}}{N_{\rm via}} + \frac{\rho_{\rm con}}{W\cdot L} \tag{6}$$

where $\rho_{\square,\,\rm sil}$ is the silicide sheet resistance, $R_{\rm via}$ is the resistance of a metal1-to-polysilicon via, $N_{\rm via}$ is the number of such

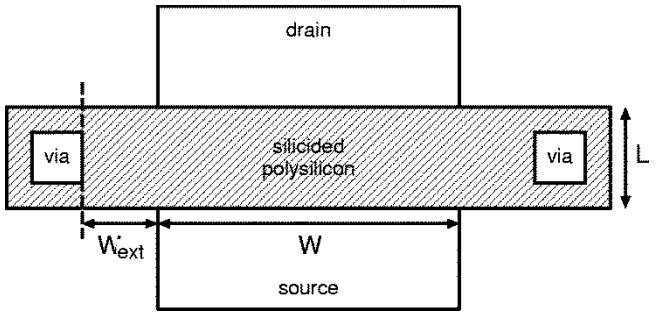

Fig. 7. Schematic layout of a single gate finger, showing the meaning of W, $W_{\rm ext}$, and L in (6).

vias, $\rho_{\rm con}$ is the silicide-to-polysilicon specific contact resistance, and the meanings of W, L, and $W_{\rm ext}$ are depicted in Fig. 7.

4) Noise From Other Parasitic Resistances: Besides the noise from the gate resistance, the other parasitic resistances also produce thermal noise. The role of thermal noise of the bulk resistance has been emphasized by [37] and [38] and is taken into account by the circuit simulator when our compound model (Fig. 3) is used. Similarly, the thermal noise of the source/drain series resistances are accounted for. Their relative importance will be discussed below.

5) Parameter Extraction: The MOS Model 11 parameters, such as gain factor, body factor, flatband voltage, source/drain series resistance, and mobility reduction coefficients, are extracted from standard dc and low-frequency *C–V* measurements. The detailed extraction procedure can be found in [27].

Only for the extraction of bulk resistance parameters S-parameter measurements are required. These are taken in the off-state ($V_{\rm GS} = 0$ V) as described in [39].

For the calculation of the effective gate resistance with (6), we need to know the silicide sheet resistance $\rho_{\square,\,\rm sil}$, the silicide-to-polysilicon specific contact resistance $\rho_{\rm con}$, and the resistance $R_{\rm via}$ of a metal1-to-polysilicon via.

The frequency independence of the silicide sheet resistance has been verified using S-parameter measurements on dedicated test structures (see Fig. 8). It was found that $\rho_{\square,\,\rm sil}$ is equal to 4 Ω/sq., except for the 0.18-μm device where the sheet resistance is 9 Ω/sq., probably due to incomplete silicidation. Having verified the frequency independency of the silicide sheet resistance, means that one can rely on dc measurements of this resistance just as well.

The silicide-to-polysilicon specific contact resistance $\rho_{\rm con}$ is 25 $\Omega \cdot \mu$m^2 [36], and $R_{\rm via}$ was found to be 22 Ω.

Finally, note that there are no parameters adjusted to fit the noise measurements. The only MOS Model 11 parameter that can be used to adjust the noise is $N_{\rm T}$, which is set to its theoretical value $4k_{\rm B}T$.

D. Experimental Details and Deembedding

Noise measurements are performed on a commercially available RF CMOS technology with an 0.18-μm minimum feature size. This technology shows an $f_{\rm T}$ of 70 GHz and an $f_{\rm max}$ as high as 150 GHz [40]. This world-record $f_{\rm max}$ was achieved

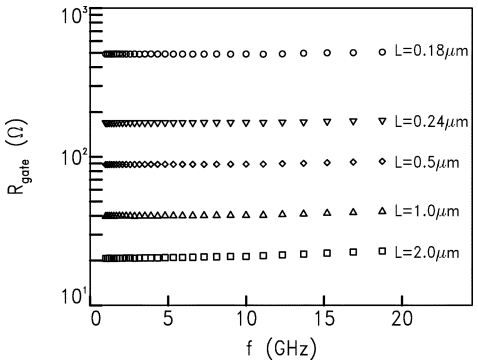

Fig. 8. Gate resistance versus frequency as measured on dedicated test structures ($W = 10$ μm). The sheet resistance is 4 Ω/sq., except for the 0.18-μm device where the sheet resistance is 9 Ω/sq., due to incomplete silicidation. Gate lengths are $L = 2$ μm ($\square$), $L = 1$ μm ($\triangle$), $L = 0.5$ μm ($\diamond$), and $L = 0.24$ μm ($\triangledown$), and $L = 0.18$ μm ($\circ$).

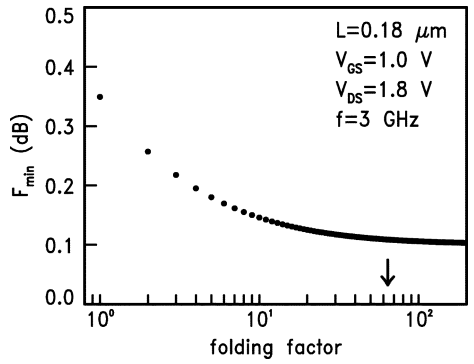

Fig. 9. Layout optimization using the model described in this paper. The minimum noise figure at 3 GHz is calculated as a function of the folding factor, for an n-channel device with a 0.18-μm gate length and a total width of 192 μm, biased at $V_{\rm GS} = 1$ V and $V_{\rm DS} = 1.8$ V. The arrow indicates the folding factor of 64 that we used, which corresponds to a 3-μm finger width.

by careful layout optimization, reducing the effective gate resistance to a minimum using folding and double-sided connection of the gate.

This same layout optimization also leads to attractive noise figures [40]. In Fig. 9, we calculate the minimum noise figure of a 0.18-μm n-channel device as a function of the folding factor. The total device width is kept constant at 192 μm. By folding the device, the effective gate resistance is considerably reduced, and therefore the minimum noise figure is reduced considerably as well. Based on Fig. 9, we have chosen a folding factor of 64, corresponding to a finger width of 3 μm. Further reduction of finger width does not lead to a much lower minimum noise figure (see Fig. 9).

The RF noise figure measurements were taken over frequency and versus bias voltage using an HP8970 noise figure test-set for a limited number of precharacterized source and load impedances which provided stable device operation over the entire gain bandwidth of our devices. The addition of a separate low-noise amplifier to our system reduces its noise figure to 2.4 dB up to 18 GHz. S-parameters are simultaneously measured using an HP8510C network analyzer. The amount of gate and drain current thermal noise and their correlation is derived in two steps. First the noise added by the input and output stages

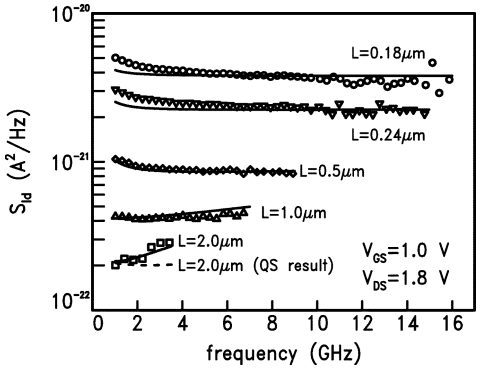

Fig. 10. Drain current thermal noise versus frequency for a series of n-channel devices with $L = 2$ μm (□), $L = 1$ μm (△), $L = 0.5$ μm (◇), $L = 0.24$ μm (▽), and $L = 0.18$ μm (○). The devices are biased at $V_{\rm GS} = 1$ V and $V_{\rm DS} = 1.8$ V. Solid lines are model predictions. The dashed line is the result of a quasi-static model for the $L = 2$ μm device.

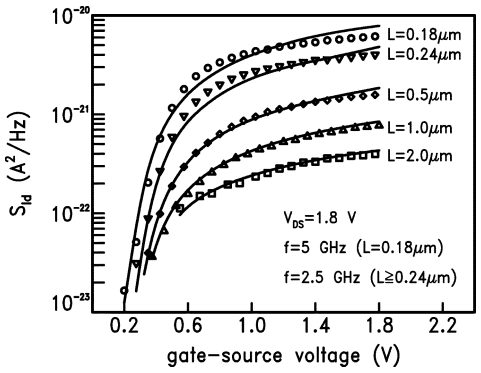

Fig. 11. Drain current thermal noise versus $V_{\rm GS}$ for the same devices as in Fig. 10. The devices are biased at $V_{\rm DS} = 1.8$ V. Solid lines are model predictions. All curves are taken at 2.5 GHz, except for the $L = 0.18$–μm curve, which was taken at 5 GHz.

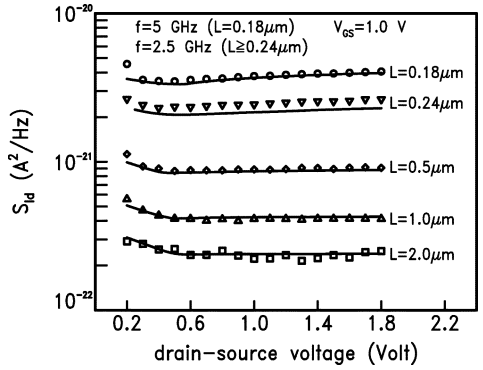

Fig. 12. Drain current thermal noise versus $V_{\rm DS}$ for the same devices as in Fig. 10. The devices are biased at $V_{\rm GS} = 1.0$ V. Solid lines are model predictions. All curves are taken at 2.5 GHz, except for the $L = 0.18$–μm curve, which was taken at 5 GHz.

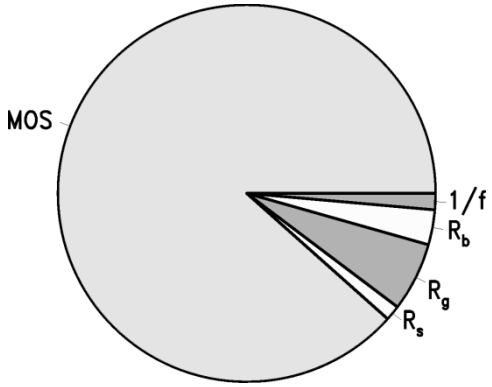

Fig. 13. Contributions to simulated drain current thermal noise of $L = 0.18$ μm device at $f = 3$ GHz. The device is biased at $V_{\rm GS} = 1$ V and $V_{\rm DS} = 1.8$ V.

is corrected for, and the noise parameters like minimum noise figure, noise resistance, and optimum source impedance are extracted [41]. For the subsequent Y- and noise parameter de-embedding, a conversion to the correlation matrix representation of noisy two-ports is made [42]. The transistor Y-parameters and noise current sources are then derived using S-parameter measurements performed on "open" and "short" dummy structures along the lines of [41]–[43].

E. Results

1) Drain Current Noise: The measured and modeled drain current noise of various n-channel geometries is plotted as a function of frequency, gate voltage, and drain voltage in Figs. 10–12, respectively. It is observed that our model gives an excellent prediction of the drain current noise both for the long and short-channel geometries, confirming our conclusions in [24]: in sharp contrast to [17]–[19], we do *not* observe large enhancements of thermal noise in short-channel MOSFETs. Relatively small discrepancies (up to ∼20%) are found at lower frequencies for the short channels and are not understood at present. Possibly, a more refined description of gate or bulk parasitics may explain the effect.

An interesting phenomenon is observed in the $L = 2$–μm curves: the noise is seen to increase with frequency. This phenomenon is due to nonquasi-static effects, which are automatically accounted for by our segmentation approach. Using a single-segment model, the simulation yields a white noise spectrum and underestimates the measured noise (dashed line in Fig. 10).

Note also that there is hardly any dependence of the noise on $V_{\rm DS}$ in saturation (see Fig. 12). This an experimental confirmation that the noise contribution of the pinch-off region may be neglected, as we have done in our model. The very small dependence of the noise on $V_{\rm DS}$ for the shortest devices is due to the channel length modulation effect, included in our model.

The various contributions to the modeled drain current noise of the 0.18-μm device at 3 GHz are indicated in Fig. 13. It is seen that the major part (88%) is due to the intrinsic thermal noise of the MOSFET. The relatively small contribution of the gate resistance is due to the careful device layout optimization (narrow fingers and double-sided contacting of the gate). Moreover, we observe that there are small contributions of the bulk resistance, the source resistance, and some $1/f$ noise.

Drain current thermal noise is often represented using the so-called "white noise gamma factor" γ, defined by the equation

$$S_{I_{\rm D}} = 4k_{\rm B}Tg_{\rm do}\gamma \tag{7}$$

where $g_{\rm do}$ is the MOSFET output conductance at zero drain–source bias. The theoretical long-channel value of γ is $\gamma = 2/3$. In Fig. 14, both measured and modeled γ factors

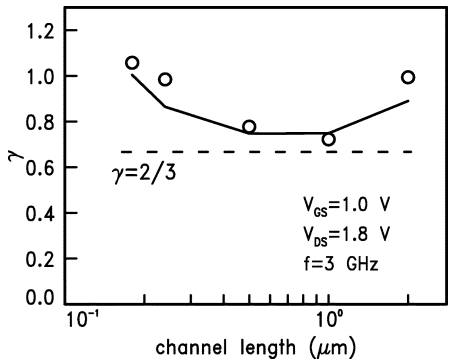

Fig. 14. White noise gamma factor versus gate length at 3 GHz, at a bias of $V_{\rm GS} = 1$ V and $V_{\rm DS} = 1.8$ V. Markers represent measured values, and the solid lines are model predictions.

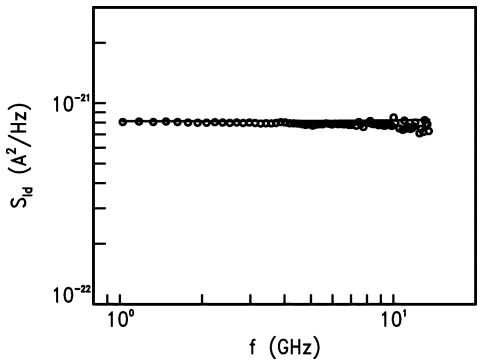

Fig. 15. Drain current thermal noise versus frequency for a p-channel device with $L = 0.18$ μm. The device is biased at $|V_{\rm GS}| = 1$ V, $|V_{\rm DS}| = 1.8$ V, and $|V_{\rm BS}| = 0$ V. The solid line represents model prediction.

are plotted for $f = 3$ GHz. At intermediate channel lengths, γ is close to the classical $\gamma = 2/3$. Shorter channels show a small enhancement of γ, which is partly due to thermal noise of parasitic resistances (see Fig. 13) and partly due to short channel effects such as velocity saturation and channel length modulation [29]. The increase of γ for longer channel lengths is due to the nonquasi-static effect. This follows from inspection of Fig. 10, where the quasi-static model (dashed line) is seen to give less noise than the nonquasi-static model (solid line) for the $L = 2$ μm device.

The drain current noise of our 0.18-μm p-channel device is plotted versus frequency in Fig. 15 and versus bias in Fig. 16. Also, for the p-channels, our model gives an excellent prediction of the measurements.

2) Avalanche Noise: In the above, we observed that the measured drain current noise is independent of drain voltage when the device is biased in saturation. This situation changes when we increase the drain voltage far above the supply voltage of this technology, $V_{\rm dd} = 1.8$ V. In that case, weak avalanche comes into play. In the upper frame of Fig. 17, the multiplication factor $M \equiv I_{\rm D}/I_{\rm S}$ is plotted versus drain voltage. At $V_{\rm DS} = 3$ V, the multiplication factor has increased from 1.00 to 1.03. The corresponding increase in drain current noise is much more spectacular and amounts to a factor of $\sim$2. This sharp increase in drain current noise is explained when we include the noise associated with the weak avalanche current from drain to bulk. This noise

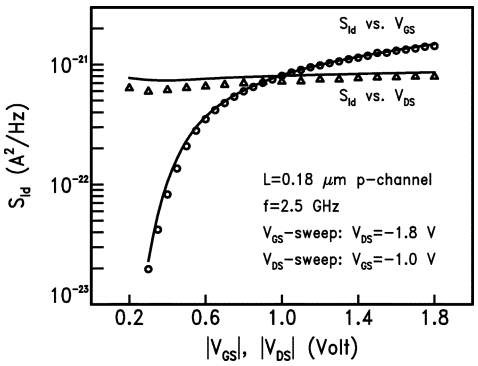

Fig. 16. Drain current thermal noise versus $|V_{\rm GS}|$ ($|V_{\rm DS}| = 1.8$ V) and versus $|V_{\rm DS}|$ ($|V_{\rm GS}| = 1$ V) for a p-channel device with $L = 0.18$ μm. Solid lines are model predictions.

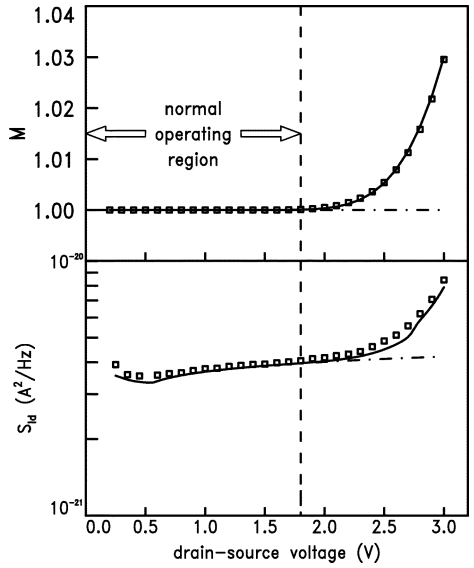

Fig. 17. (Top) multiplication factor and (bottom) drain current thermal noise versus $V_{\rm DS}$, for an $L = 0.18$ μm n-channel device, biased at $V_{\rm GS} = 1.0$ V. The drain voltage is intentionally swept far beyond the supply voltage to make the effects of the weak avalanche current visible. Dashed lines: model without avalanche multiplication. Solid lines: model with avalanche multiplication and the noise associated to it.

contribution has been treated theoretically by van der Ziel and Chenette [44], who found

$$S_{I_{\rm D}} = M^2 S_{\rm is} + 2qI_{\rm S}M(M-1). \tag{8}$$

The first term in this equation is the trivial multiplication of the thermal noise generated in the channel (i.e., the source current noise $S_{\rm is}$). The second term is the actual noise contribution of the weak avalanche current itself ($I_{\rm B}$), which can be rewritten as $2qI_{\rm B}M$. Therefore, (8) is equivalent to

$$S_{\rm ib} = (M-1)^2 S_{\rm is} + 2qI_{\rm B}M. \tag{9}$$

In our model, we have added this noise current source [see (9)] between drain and bulk. This yields the solid line in the lower frame of Fig. 17, which fits the data excellently. To the best of our knowledge, this is the first experimental verification of the van der Ziel–Chenette equation for avalanche noise in a MOSFET.

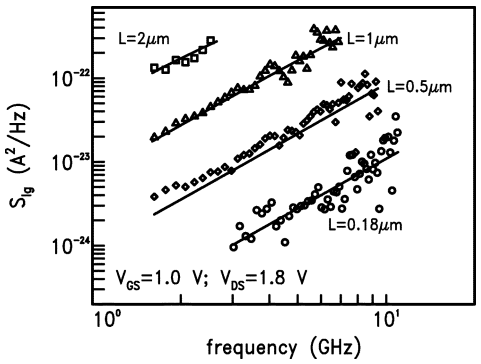

Fig. 18. Gate current noise versus frequency for a series of n-channel devices with $L = 2\ \mu$m (□), $L = 1\ \mu$m (△), $L = 0.5\ \mu$m (◇), and $L = 0.18\ \mu$m (○). The $L = 0.24\ \mu$m device is skipped here for clarity of the figure. The devices are biased at $V_{\rm GS} = 1$ V, and $V_{\rm DS} = 1.8$ V. Solid lines are model predictions with noisy $R_{\rm gate}$. Dashed line is model prediction for $L = 0.18\ \mu$m calculated with an additional 0.5-Ω contact resistance.

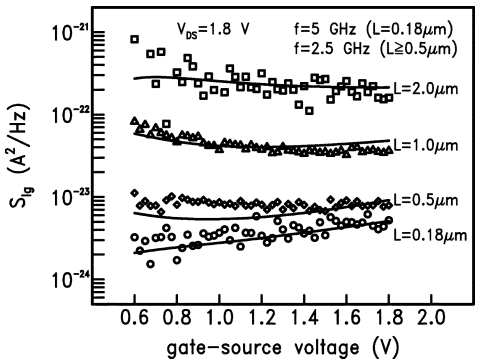

Fig. 19. Gate current noise as a function of gate voltage for the same devices as in Fig. 18. The devices are biased at $V_{\rm DS} = 1.8$ V. Solid lines are model predictions. All curves are taken at 2.5 GHz, except for the $L = 0.18\ \mu$m curve, which was taken at 5 GHz.

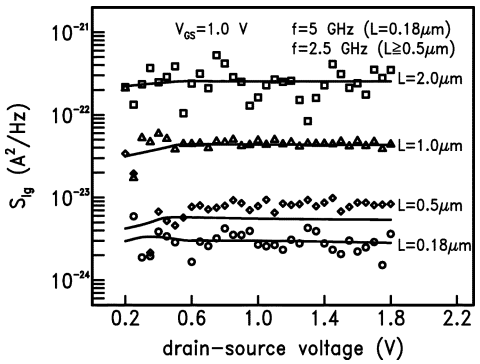

Fig. 20. Gate current noise as a function of drain voltage for the same devices as in Fig. 18. The devices are biased at $V_{\rm GS} = 1.0$ V. Solid lines are model predictions. All curves are taken at 2.5 GHz, except for the $L = 0.18\ \mu$m curve, which was taken at 5 GHz.

Evidently, the avalanche noise does not play a significant role in practical use of 0.18 μm technology: we have to increase the drain voltage far above the supply voltage of this technology to make the effect visible. The effect, however, may explain some of the anomalous results that were reported by Abidi [17]. Abidi found a γ value of 7.98 (a factor of 12 enhancement with respect to (w.r.t) the long-channel value) at a bias of $V_{\rm GS} = 1$ V and $V_{\rm DS} = 4$ V. From his output curves we estimate that $I_{\rm S} = 0.8$ mA, $g_{\rm do} = 2.5$ mS, and $M = 1.25$ (a distinguished roll-up of the $I_{\rm D}$ versus $V_{\rm DS}$ is visible in the curves). Using (8), it is readily derived in the case of avalanche that

$$\gamma = \frac{2}{3}M^2 - \frac{4}{3}(M-1) + \frac{2qI_{\rm S}M(M-1)}{4k_{\rm B}Tg_{\rm do}} \qquad (10)$$

which yields $\gamma = 2.7$ (a factor of four enhancement w.r.t. the long-channel value). Although this is still a factor of 3 lower than the $\gamma = 7.98$ found by Abidi, it shows that avalanche noise is indeed a significant contributor in his experiment, and partly explains his anomalous results.

3) Gate Current Noise: The measured and modeled gate current noise of various n-channel geometries is plotted as a function of frequency, gate voltage, and drain voltage in Figs. 18–20, respectively. Excellent agreement between measurements and model is observed. Anomalously large gate current noise, as reported in [20], is *not* found.

The various contributions to the modeled gate current noise at $f = 3$ GHz of the 0.18-μm transistor are indicated in Fig. 21. This gives a completely different picture than the corresponding plot for the drain current noise (see Fig. 13). Whereas the drain current noise is dominated by thermal noise of the intrinsic MOSFET, the induced gate noise of the intrinsic MOSFET only contributes 30% to the total gate current noise. The main contribution, 65%, stems from a parasitic resistance, namely the gate resistance. Remember that the effect of the gate resistance is not only a white noise contribution to the drain current noise, but also an f^2 contribution to the gate current noise, see (5).

As discussed before, our devices have been carefully designed to minimize the effective gate resistance (narrow fingers and double-sided contacting of the gate). This has reduced the effective silicide resistance in our devices to such an extent

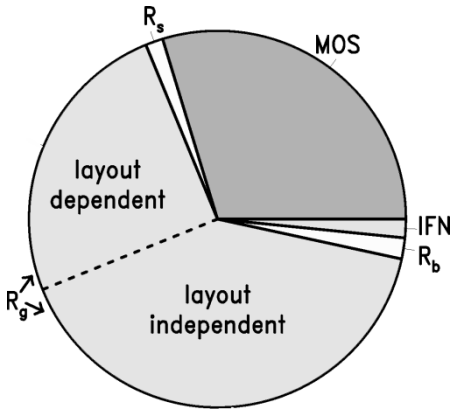

Fig. 21. Contributions to simulated gate current thermal noise of $L = 0.18\ \mu$m device at $f = 3$ GHz. The device is biased at $V_{\rm GS} = 1$ V, and $V_{\rm DS} = 1.8$ V. "IFN" stands for "induced flicker noise," which is discussed in Section III-C2, and only gives a minor contribution to the total noise.

that the effective gate resistance is now dominated by a contribution that *cannot* be influenced by device layout: the contact resistance between silicide and polysilicon. Therefore, further reduction of the finger width below 3 μm will not change the picture and we may draw the more general conclusion that *gate current noise in present-day short-channel MOSFETs is dominated by the noise associated to the parasitic gate resistance*.

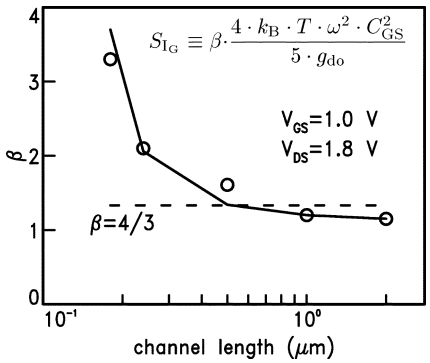

Fig. 22. Beta factor versus gate length at a bias of $V_{\rm GS} = 1$ V and $V_{\rm DS} = 1.8$ V. Markers represent measured values, and solid lines are model predictions.

Moreover, we observe that there are small contributions of the bulk resistance and the source resistance. Finally, note that induced flicker noise (see Section III-C2) only plays a minor role.

In analogy to the "white noise gamma factor" γ, which is often used to represent the amount of drain current thermal noise, the gate current noise is often represented using the so-called β-factor, defined by the equation

$$S_{I_{\rm G}} = 4k_{\rm B}Tg_{\rm g}\beta \tag{11}$$

where $g_{\rm g}$ is given by

$$g_{\rm g} = \frac{\omega^2 C_{\rm gs}^2}{5g_{\rm gdo}}. \tag{12}$$

The theoretical long-channel value of β is $\beta = 4/3$. In Fig. 22, both measured and modeled β factors are plotted for $f = 3$ GHz. At intermediate and long channel lengths, β is close to the classical $\beta = 4/3$. Shorter channels show a significant enhancement of β, due to the effect of the gate resistance, as discussed above.

In Fig. 23, the correlation coefficient between gate and drain current noise is plotted for a number of geometries. Although the general agreement is satisfactory, some differences in $\mathrm{Im}(c)$ between measurement and model are observed, which are a subject of further study. Note however that the measurement of the correlation coefficient for short-channel devices is at the limit of our present noise measurement setup. The precise determination of the correlation coefficient requires a more advanced measurement system than presently available to us. More specifically, a smaller bandwidth of the noise figure meter and less frequency offset between noise figure meter and network analyzer are required for this purpose.

Finally we show the gate current noise as a function of frequency of the short-channel PMOS device in Fig. 24. Just like in the n-channel case, an excellent agreement between model and measurements is observed. The corresponding correlation coefficient is plotted in Fig. 25. Just like in the n-channel case, there is a slight discrepancy in $\mathrm{Im}(c)$, which needs further investigation.

4) Noise Figure: Having verified our model in terms of $S_{I_{\rm D}}$, $S_{I_{\rm G}}$, and c, it is of interest to look at the noise figure, the quantity of interest for a circuit designer. In Figs. 26 and 27, the minimum noise figure and the 50-Ω noise figure are plotted versus frequency for a number of n-channel geometries. As expected, a close agreement between data and model prediction is seen. Further note that, for the 0.18-μm device, very attractive noise figures are encountered: in the 1–10-GHz range, the minimum noise figure remains below 1 dB. For a 50-Ω source impedance, the noise figure remains below 2 dB in this range. Both minimum and 50-Ω noise figures will even become better in future CMOS technologies (see [45]).

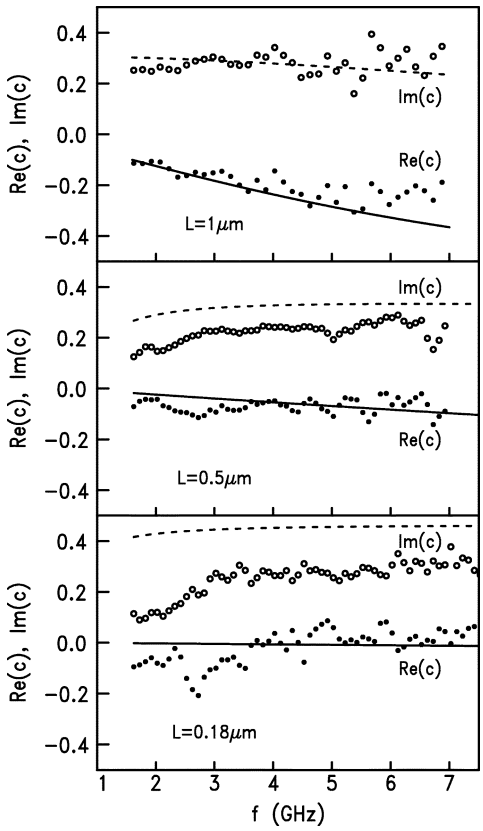

Fig. 23. Measurements of the real (open symbols) and imaginary (filled symbols) parts of the correlation coefficient as a function of frequency for a number of n-channel geometries, at a bias of $V_{\rm GS} = 1$ V and $V_{\rm DS} = 1.8$ V. Dashed and solid lines are model predictions of the real and imaginary parts of the correlation coefficient, respectively.

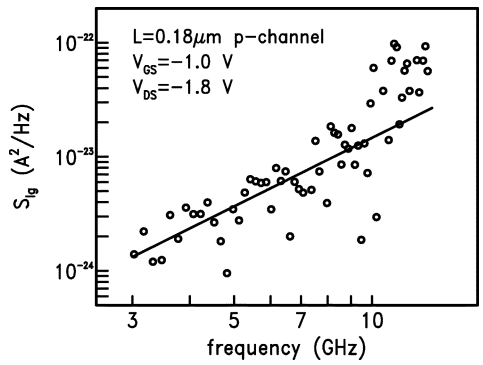

Fig. 24. Induced gate current noise versus frequency for a p-channel device with $L = 0.18$ μm. The device is biased at $|V_{\rm GS}| = 1$ V and $|V_{\rm DS}| = 1.8$ V. Solid line is model prediction.

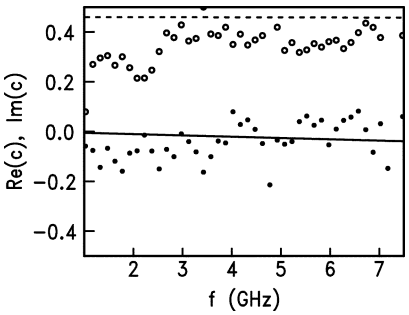

Fig. 25. Measurements of the real (open symbols) and imaginary (filled symbols) parts of the correlation coefficient as a function of frequency for a 0.18-μm p-channel, biased at $|V_{\rm GS}| = 1$ V, and $|V_{\rm DS}| = 1.8$ V. Dashed and solid lines are model predictions of the real and imaginary parts of the correlation coefficient, respectively.

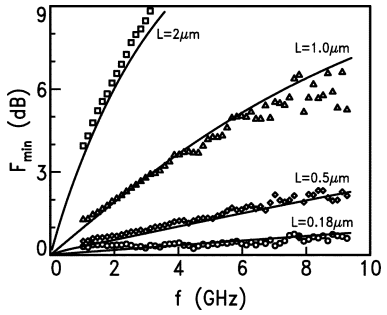

Fig. 26. Minimum noise figure versus frequency for a number of n-channel geometries. The bias is $V_{\rm GS} = 1$ V, and $V_{\rm DS} = 1.8$ V. Symbols represent measurements, and lines represent model predictions.

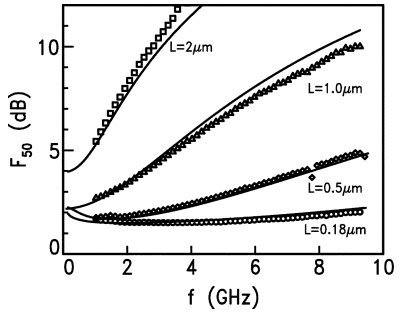

Fig. 27. The 50-Ω noise figure versus frequency for a number of n-channel geometries. The bias is $V_{\rm GS} = 1$ V, and $V_{\rm DS} = 1.8$ V. Symbols represent measurements, and lines represent model predictions.

F. Discussion

We have shown a modeling approach, based on the channel segmentation approach, which is able to predict the MOSFET thermal noise to a high degree of accuracy. Our main conclusion is that classical noise modeling approach [25], [23] is still valid, if short-channel effects such as velocity saturation and channel length modulation are properly accounted for, as well as the parasitic resistances that surround the intrinsic MOSFET. Therefore, it is very unlikely that carrier heating, invoked by several authors to explain their anomalous results [17]–[19], plays a significant role.

This conclusion is well in line with other recent work, e.g., by Jamal Deen [29] and by Brederlow [46]. The interesting question remains, of course, what causes the anomalous noise enhancements observed by other authors [17]–[20]. This is a question that we can only partly answer. As far as Abidi's results [17] are concerned, we already saw in Section III-E2 that they can be partly explained by avalanche noise. Knoblinger's results [20] on gate current noise are most likely due to improper deembedding of the gate resistance: we have shown in Section III-E3 that gate current noise in short-channel MOSFETs is dominated by the gate current noise, even in the case of optimized device layouts. In suboptimal layouts, the induced gate noise of the intrinsic MOSFET is overwhelmed by the gate resistance noise. A slight underestimation of the gate resistance (neglection of the channel length dependence of the silicide sheet resistance or neglection of the silicide-to-polysilicon contact resistance [36]) may therefore lead to a giant overestimation of the induced gate noise of the intrinsic MOSFET.

IV. Additional Noise Sources in Technologies With Leaky Gate Oxides

A. Introduction

Our investigations so far have been restricted to a 0.18-μm CMOS technology, in which gate leakage can be neglected. It is well known, however, that in technologies beyond 0.18 μm gate leakage becomes more important due to direct tunneling of charge carriers through the gate dielectric. In the context of this work, the interesting question arises of what the impact of gate leakage on the noise will be. In this section, we will investigate this question in a 100-nm CMOS technology. In this investigation, we use a set of dc structures, for which MOS Model 11 parameters have been determined. Since gate leakage is covered by MOS Model 11 [47], [27], this allows us to explore its effects on the noise behavior of MOSFETs with leaky gate dielectrics.

B. Shot Noise of the Gate Leakage Current

Since gate leakage current is the result of quantum-mechanical direct tunneling process, it is expected [23] that MOSFETs with a leaky gate dielectric will show a shot noise contribution in the gate current

$$S_{I_{\rm G}} = 2 \cdot q \cdot I_{\rm G}. \tag{13}$$

In order to verify (13) experimentally, we have performed low-frequency noise measurements on a large-area transistor in 100-nm technology using a BTA low-frequency noise measurement system. An example of a noise spectrum of the gate current is shown in Fig. 28. Apart from low-frequency noise, discussed below in Section IV-C, the spectrum also exhibits a white noise contribution. For a number of bias conditions, we determined this white noise contribution using a curve fit to the data, with both low-frequency noise and a white contribution (see Fig. 28). Subsequently, the fitted white noise level is plotted against the dc gate current in Fig. 29. The theoretical expression (13) is seen to give an excellent prediction of the observed white noise levels, clearly demonstrating the presence of shot noise in the gate leakage current.

To assess the importance of this effect, we have added it to our RF model of Fig. 3 and calculated the resulting gate current noise spectrum for a number of channel lengths. The result is shown in Fig. 30. It is seen that shot noise, giving a frequency-independent contribution to $S_{I_{\rm G}}$, significantly enhances

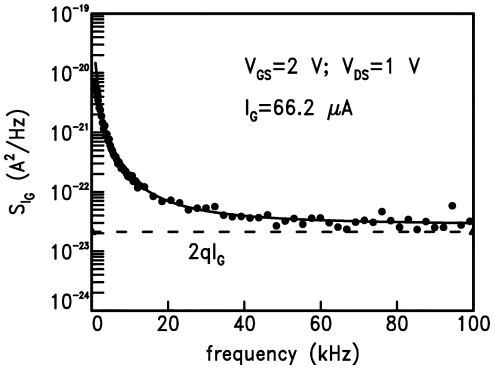

Fig. 28. Low-frequency gate current noise spectrum of a 10/10-μm MOSFET processed in 100-nm technology with a 1.5-nm EOT. Markers: measurements; solid line: fit to the data with LF-noise and white contribution; dashed line: expected shot noise level.

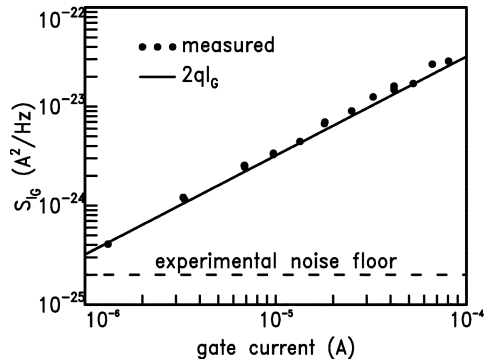

Fig. 29. Markers: white noise contribution to the gate current noise as a function of measured gate current. $V_{\rm DS} = 1$ V and $V_{\rm GS}$ is varied. Solid line: expected shot noise $2qI_{\rm G}$.

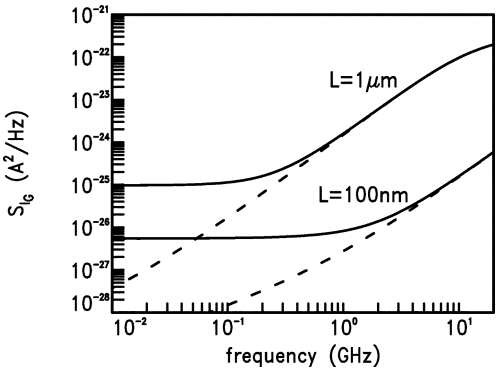

Fig. 30. Simulated gate current noise spectra of a 1-μm and a 100-nm MOSFET processed in a 100-nm technology with a 1.5-nm EOT. The devices are biased at $V_{\rm DS} = V_{\rm GS} = 1$ V. Dashed lines are calculated without shot noise. Solid lines are calculated with shot noise.

$S_{I_{\rm G}}$, in particular at sub-GHz frequencies. For the 100-nm device, it is observed that $S_{I_{\rm G}}$ is dominated by induced gate noise and gate resistance noise (both giving f^2 dependence) when the frequency is above $\sim$1 GHz. Thus, the impact of shot noise of the gate current seems to be very limited for typical RF CMOS frequencies which operate at a few gigahertz. For more conventional analog CMOS applications, however, shot noise of the gate current may affect the circuit performance. In particular, when the MOSFET is used as a capacitor, the source and drain are tied together, and the shot noise of the gate current will be the dominant noise source.

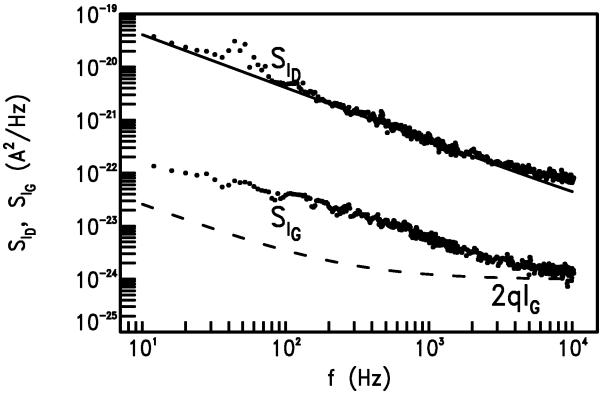

Fig. 31. Drain current and gate current low-frequency noise spectra of a 10/10-μm MOSFET processed in a 100-nm technology with a 1.5-nm EOT. The device is biased at $V_{\rm DS} = V_{\rm GS} = 1$ V. The dashed line is prediction of our segmentation model, including shot noise of the gate leakage current.

C. $1/f$ Noise of the Gate Current

Several authors have observed $1/f$ noise in the gate current [48]–[50]. Alers [48] has attributed this to the phenomenon of trap-assisted tunneling. However, in oxides whose leakage is dominated by direct tunneling, it is not clear how the observed low-frequency noise must be explained.

We have performed low-frequency noise measurements on a 10/10-μm n-channel MOSFET processed in 100-nm CMOS technology. In addition to the usual $1/f$ noise in the drain current, we also observe a low-frequency noise contribution to the gate current noise. An example is shown in Fig. 31. The solid line in the picture gives the modeled drain current noise, which has been adjusted to fit the data. Next, we calculate the low-frequency gate current noise using the segmentation model of Fig. 3, which has been extended with shot noise. This gives the dashed line in Fig. 31. It is seen that, besides the shot noise contribution that we have added to the model explicitly, also a low-frequency noise contribution emanates from the model. This is due to an effect which is very similar to the well-known induced gate noise in MOSFETs. The latter is caused by the capacitive coupling between channel and gate. In leaky dielectrics, however, there also exists a dc coupling between channel and gate, which gives rise to a replica of the drain current noise spectrum in the gate terminal. This mechanism acts both on the $1/f$ noise and the thermal noise of the conducting channel, giving rise to $1/f$ and a white contribution in the gate terminal, respectively. However, the mechanism, as described above, is not sufficient to describe the measured low-frequency gate current noise (see Fig. 31). One may think of several explanations. One possibility is that there may be a contribution of trap-assisted tunneling to the noise, although the current itself is dominated by direct tunneling. Another possibility is the modulation of the direct-tunneling probability by the Coulomb field of the traps that are thought to be responsible for drain current $1/f$ noise.

V. Conclusion

Let us summarize the conclusions of this paper briefly.

$1/f$ Noise: We have shown low-frequency noise measurements on a set of small-area p-channel MOSFETs strongly point toward an explanation of the $1/f$ noise based on carrier trapping.

Thermal Noise: Based on extensive measurement and analysis on both n- and p-channel devices, we find that there is only a moderate enhancement of drain current noise in 0.18-μm CMOS technology. We do find an enhancement of gate current noise, though not as dramatic as in [20]. The enhancement we find is explained by the gate current noise associated with the gate resistance. We have presented an RF model for circuit simulation, based on channel segmentation, which predicts both drain and gate current noise at RF frequencies, even in the nonquasi-static regime.

Avalanche Noise: When the drain–source voltage is raised far beyond the supply voltage, effects of weak avalanche become visible in the drain current as well as in the drain current noise. This behavior is well predicted by the avalanche noise equation developed by van der Ziel [44] and partly explains the often-cited anomalous results of Abidi [17].

Shot Noise Due to Gate Leakage: We have experimentally demonstrated the presence of shot noise in the direct-tunneling gate current in a 100-nm CMOS technology. We have shown that this shot noise will not affect RF design in this technology, but may have some impact on more traditional analog design.

$1/f$ *Noise in the Gate Current:* We have shown that $1/f$ noise in the gate current is expected because the dc coupling between channel and gate transfers $1/f$ noise from the inversion channel into the gate terminal. However, this is not enough to explain the magnitude of the gate current $1/f$ noise that is actually found in experiments. An explanation is still lacking.

APPENDIX

In this appendix, we derive the expression for the drain current noise valid for both long- and short-channel MOSFETs. The starting point is the Klaassen–Prins equation (2). In order to evaluate this equation, we first need to have an expression for $g(V)$.

The channel current $I_{\rm DS}$ in a MOSFET is given by

$$I_{\rm DS} = g(V) \cdot \frac{\partial V}{\partial x} \tag{14}$$

where V is the quasi-Fermi potential ranging from $V_{\rm SB}$ at the source side ($x = 0$) to $V_{\rm DB}$ at the drain side ($x = L$), and $g(V)$ is the local channel conductance given by

$$g(V) = -\mu(V) \cdot W \cdot Q_{\rm inv}(V). \tag{15}$$

Equation (14) can be rewritten in terms of drift and diffusion components

$$\begin{aligned} I_{\rm DS} &= g(\psi_{\rm s}) \cdot \frac{\partial \psi_{\rm s}}{\partial x} + \mu(\psi_{\rm s}) \cdot W \cdot \phi_{\rm T} \cdot \frac{\partial Q_{\rm inv}}{\partial x} \\ &= g(\psi_{\rm s}) \cdot \frac{\partial \psi_{\rm s}}{\partial x} \cdot \left(1 - \frac{\phi_{\rm T}}{Q_{\rm inv}} \cdot \frac{\partial Q_{\rm inv}}{\partial \psi_{\rm s}}\right) \end{aligned} \tag{16}$$

where $\phi_{\rm T}$ is the thermal voltage $k_{\rm B} \cdot T/q$, and $\psi_{\rm s}$ is the surface potential ranging from $\psi_{\rm s_0}$ to $\psi_{\rm s_L}$. This can be rewritten in a more convenient way as

$$I_{\rm DS} = g(\psi_{\rm s}) \cdot \frac{\partial \psi_{\rm s}}{\partial x} \cdot \frac{Q^*_{\rm inv}}{Q_{\rm inv}} \tag{17}$$

where $Q^*_{\rm inv} = Q_{\rm inv} - \phi_{\rm T} \cdot (\partial Q_{\rm inv}/\partial \psi_{\rm s})$. The inversion-layer charge density $Q_{\rm inv}$ depends on the surface potential and can be accurately approximated by

$$\begin{aligned} Q_{\rm inv}(\psi_{\rm s}) &= Q_{\rm inv}(\overline{\psi}) + \left.\frac{\partial Q_{\rm inv}}{\partial \psi_{\rm s}}\right|_{\psi_{\rm s}=\overline{\psi}} \cdot \left(\psi_{\rm s} - \overline{\psi}\right) \\ &= \overline{Q}_{\rm inv} - C_{\rm inv} \cdot \left(\psi_{\rm s} - \overline{\psi}\right) \end{aligned} \tag{18}$$

where $\overline{\psi}$ is the average surface potential $(\psi_{\rm s_0} + \psi_{\rm s_L})/2$.

For n-type MOSFETs, the carrier mobility $\mu(\psi_{\rm s})$, including velocity saturation, is given by [51]

$$\mu(\psi_{\rm s}) = \frac{\mu_{\rm eff}}{\sqrt{1 + \left(\frac{\mu_{\rm eff}}{v_{\rm sat}} \cdot \frac{\partial \psi_{\rm s}}{\partial x}\right)^2}} \tag{19}$$

where $\mu_{\rm eff}$ is the effective mobility including mobility reduction and $v_{\rm sat}$ is the saturation velocity limited by optical phonon scattering.

Solving $\partial \psi_{\rm s}/\partial x$ from (14), (15), and (19) yields an explicit expression

$$\frac{\partial \psi_{\rm s}}{\partial x} = \frac{I_{\rm DS}}{\sqrt{\mu^2_{\rm eff} \cdot W^2 \cdot Q^{*2}_{\rm inv} - \left(\frac{\mu_{\rm eff}}{v_{\rm sat}} \cdot I_{\rm DS}\right)^2}}. \tag{20}$$

Inserting the above equation into (19) and then the next into (15), $g(V)$ can be evaluated, resulting in

$$g(V) = \sqrt{\mu^2_{\rm eff} \cdot W^2 \cdot Q^{*^2}_{\rm inv} - \left(\frac{\mu_{\rm eff}}{v_{\rm sat}} \cdot I_{\rm DS}\right)^2} \cdot \frac{Q_{\rm inv}}{Q^*_{\rm inv}}. \tag{21}$$

Having derived the expression for $g(V)$, we are ready to evaluate the Klaassen–Prins equation (2). To perform the integration in (2), we need to find an analytical expression for $g^2(V) \cdot {\rm d}V$. Using (21) for $g(V)$ and (14) and (17) for ${\rm d}V$, we write

$$\begin{aligned} g^2(V) \cdot {\rm d}V &= g^2(\psi_{\rm s}) \cdot \frac{Q^*_{\rm inv}}{Q_{\rm inv}} \cdot {\rm d}\psi_{\rm s} \\ &= \left[\mu^2_{\rm eff} \cdot W^2 \cdot Q_{\rm inv} \cdot Q^*_{\rm inv} - \left(\frac{\mu_{\rm eff}}{v_{\rm sat}} \cdot I_{\rm DS}\right)^2 \cdot \frac{Q_{\rm inv}}{Q^*_{\rm inv}}\right] \cdot {\rm d}\psi_{\rm s}. \end{aligned} \tag{22}$$

The last term of the above equation is determined by the effect of velocity saturation and is thus only of importance in the strong inversion region, where drift current is dominant. Simplifying the influence of diffusion on the velocity saturation term, i.e., $Q_{\rm inv} \approx Q^*_{\rm inv}$, (22) can be approximated by

$$\begin{aligned} g^2(V) \cdot {\rm d}V &\approx \left[\mu^2_{\rm eff} \cdot W^2 \cdot Q_{\rm inv} \cdot Q^*_{\rm inv} - \left(\frac{\mu_{\rm eff}}{v_{\rm sat}} \cdot I_{\rm DS}\right)^2\right] \cdot {\rm d}\psi_{\rm s}. \end{aligned} \tag{23}$$

The integration in (2) can now be performed and yields

$$\begin{aligned} S_{\rm I_D} = \frac{4 \cdot k_{\rm B} \cdot T}{I_{\rm DS} \cdot L^2_{\rm elec}} \cdot \mu^2_{\rm eff} \cdot W^2 \cdot \Delta\psi \\ \cdot \left[\overline{Q}_{\rm inv} \cdot \overline{Q}^*_{\rm inv} + \frac{C^2_{\rm inv}}{12} \cdot \Delta\psi^2 - \left(\frac{I_{\rm DS}}{v_{\rm sat} \cdot W}\right)^2\right]. \end{aligned} \tag{24}$$

As expected, this equation reduces to the shot noise expression

$$S_{\mathrm{I_D}} = 2 \cdot q \cdot I_{\mathrm{DS}} \tag{25}$$

in weak inversion.

The above derivation for thermal noise holds for n-type MOSFETs. For p-type MOSFETs, a different expression for velocity saturation has to be used [51] as follows:

$$\mu(\psi_{\mathrm{s}}) = \frac{\mu_{\mathrm{eff}}}{\sqrt{1 + \frac{\left(\frac{\mu_{\mathrm{eff}}}{v_{\mathrm{c}}} \cdot \frac{\partial \psi_{\mathrm{s}}}{\partial x}\right)^2}{\sqrt{G^2 + \left(\frac{\mu_{\mathrm{eff}}}{v_{\mathrm{c}}} \cdot \frac{\partial \psi_{\mathrm{s}}}{\partial x}\right)^2}}}} \tag{26}$$

where v_{c} is a parameter corresponding to the velocity of the longitudinal acoustic phonons and G is an empirical parameter. Using (26) complicates the derivation of thermal noise, but it can be simplified by replacing $\mu_{\mathrm{eff}}/v_{\mathrm{sat}}$ in (19)–(24) by

$$\frac{\mu_{\mathrm{eff}}}{v_{\mathrm{c}}} \Bigg/ \left[G^2 + \left(\frac{\mu_{\mathrm{eff}}}{v_{\mathrm{c}}} \cdot \frac{\Delta\psi}{L}\right)^2\right]^{1/4}. \tag{27}$$

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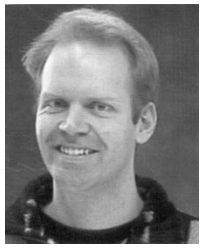

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