Noise Tolerant Low Voltage XOR-XNOR for Fast Arithmetic

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ABSTRACT

With scaling down to deep submicron and nanometer technologies, noise immunity is becoming a metric of the same importance as power, speed, and area. Smaller feature sizes, low voltage, and high frequency are the characteristics for deep submicron circuits. This paper proposes a low voltage noise tolerant XOR-XNOR gate with 8 transistors. The proposed gate has been implanted in an already existing (5-2) compressor cell to test its driving capability. The proposed gate is characterized and compared with those published ones for reliability and energy efficiency. The average noise threshold energy (ANTE) and the energy normalized ANTE metrics are used for quantifying the noise immunity and energy efficiency respectively. Results using 0.18μ CMOS technology and HSPICE for simulation show that the proposed XOR-XNOR circuit is more noise-immune and displays better power-delay product characteristics than the compared circuit. Also, the circuit proves to be faster in operation and works at all ranges of supply voltage starting from 0.6V to 3.3V.

Categories and Subject Descriptors

B.6.1 [Logic Design]: Design Styles – *combinational logic.*

General Terms Design, Reliability.

Keywords Deep submicron, nanometer technology, Noise tolerant, XOR-XNOR circuits, multipliers.

1. INTRODUCTION

The XOR and XNOR gates play the major role in various circuits especially circuits used for performing arithmetic operations like full adders, compressors, comparators, and so on [4]. An optimized design for XOR and XNOR gates is needed to benefit the performance of larger circuits that they are part of. What is meant by optimized design is to avoid any degradation on the output voltage, consume less power, having less delay, and be noise immune even with low voltage as in deep submicron technology. Another desired feature for the design of a combined XOR-XNOR cell is to have a small number of transistors to implement it [1] and the simultaneous generation of the two non-skewed outputs.

Several designs were proposed to realize the XOR function [5] using different logic styles. Two optimized designs are shown in Figure 1. The first design is based on utilizing the high functionality of pass-transistor logic style [9]. This circuit has a non-full voltage swing at the output node and is characterized by its low power consumption. This circuit has a limited deriving capability.

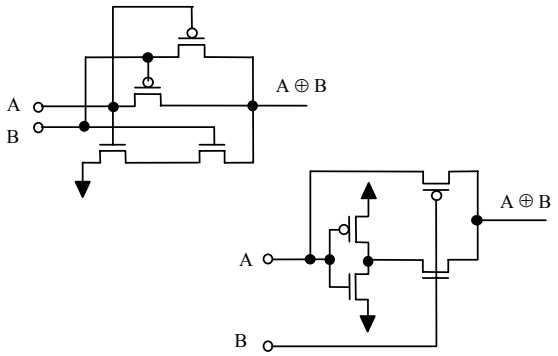

Figure 1. Two optimized implementations for the XOR function.

The second circuit is using static CMOS inverter in conjunction with a MUX circuit. The availability of the inverter gives signal level restoration and improves the deriving capability of the circuit, but extra power consumption is encountered.

Both the designs are plagued by the basic disadvantage of pass transistors i.e. bad output levels. These designs are unable to function properly when the supply voltage is scaled down as in nanometer technology. A 10-transistor design for producing XOR and its inverted output is shown in Figure 2. This circuit rectifies the flaws in the previous designs. The design is composed of two transmission gates and three static inverters. The circuit provides good output levels for all combination of inputs due to the functionality of the transmission-gate making it suitable of working at lower supply voltages. The driving capability of the circuit is also improved as it uses static inverters. The main disadvantage of the circuit is its power consumption due to the presence of the 3 static inverters. Also, the two output signals are heavily skewed in time.

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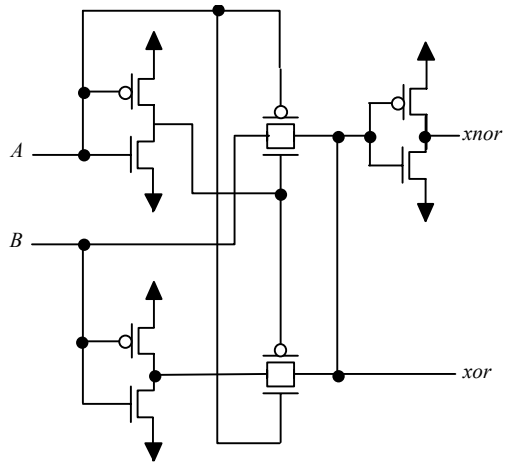


Figure 2. 10 transistor circuit for XOR-XNOR function.

To overcome the problem of skewed outputs an efficient design that combines the implementation of both the XOR and the XNOR functions in one circuit using only 6 transistors is presented in [1] (see Figure 3). The circuit has a single connection to Vdd and a single connection to Gnd with no direct connection between them. The existence of Vdd and Gnd connections give good driving capability to the circuit and the elimination of direct connections between them avoids the short circuit currents component.

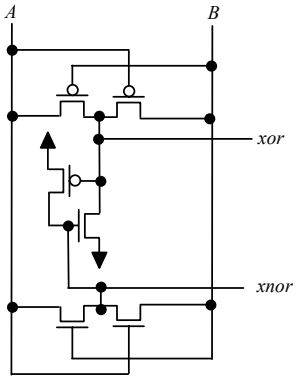


Figure 3. XOR-XNOR circuit by [1].

In large designs, multipliers have been a critical component dictating the overall circuit performance. In fast multipliers, partial products accumulation is implemented using a summation tree, called the Carry Save Adder (CSA) tree. Designs for CSA tree uses either full adders or compressors like the (4-2) compressors for interconnect regularity. High input compressors such as (5-2) and (6-2) have also been studied and reported in the literature. The XOR-XNOR and mutiplexer functions represent the core of the compressor cell according to the nature of the logic operation. The combined XOR-XNOR cell is used to drive the selection lines of the mutiplexer. The generation of XOR and XNOR simultaneously proves to be vital for this purpose. The two control signals, select and select bar, are required to reach the mux simultaneously to avoid glitches and decrease the power consumed by these glitches.

2. PROPOSED CIRCUIT

Here, we propose an efficient noise tolerant circuit design that is capable of producing XOR and XNOR simultaneously. The circuit is shown in Figure 4. In comparison with the design in Figure 2, the two outputs can be generated individually using the design units shown in Figure 5.

These units utilize only 3 transistors each as compared to the circuit in Figure 2, which uses 8 transistors for XOR and 10 transistors for XOR-XNOR. The design units produce bad logic levels for certain input combinations. This can be taken care off by the addition of a feedback loop as shown in Figure 4. The proposed design proves to be noise tolerant and provides a significant improvement in the power-delay product.

The output waveforms and the layouts of the individual units of proposed circuit, and the combined XOR-XNOR circuits are shown in Figure 6, Figure 7 respectively.

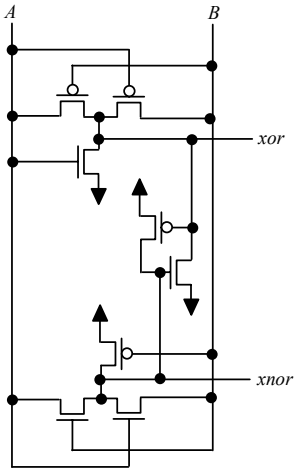


Figure 4. The proposed XOR-XNOR circuit

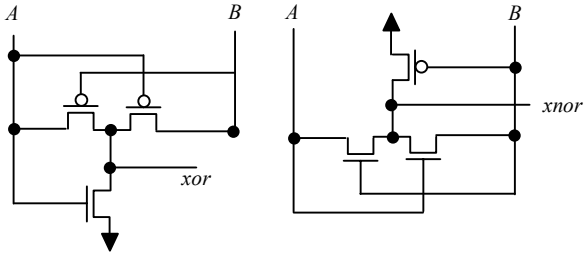
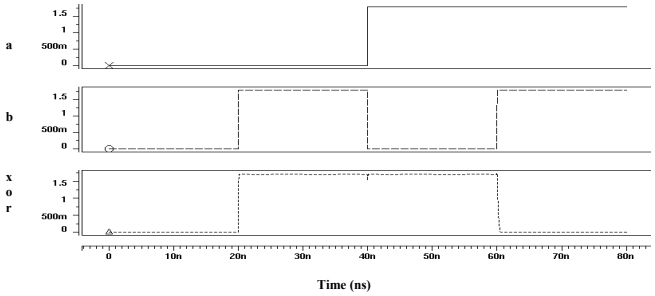
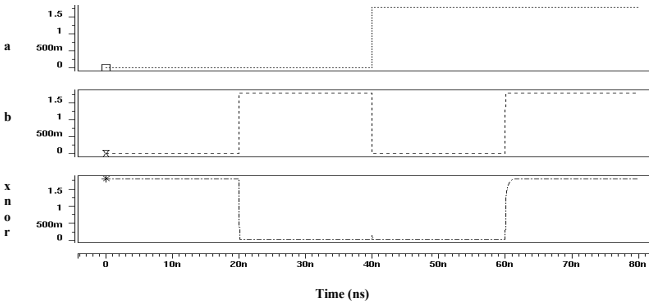


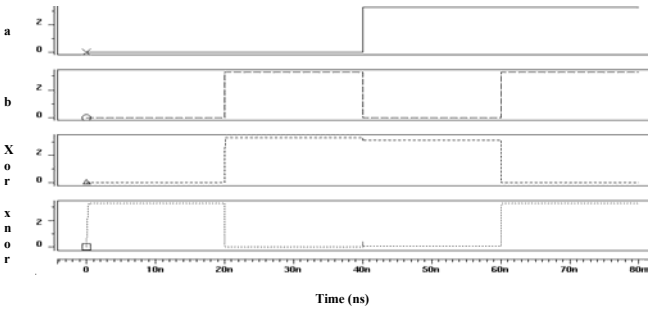
Figure 5. Individual units of the proposed XOR-XNOR circuit



(a) Output waveform of XOR unit of proposed circuit.



(b) Output waveform of XNOR unit of proposed circuit.



(d) Output waveform of the proposed circuit.

Figure 6. Output waveforms

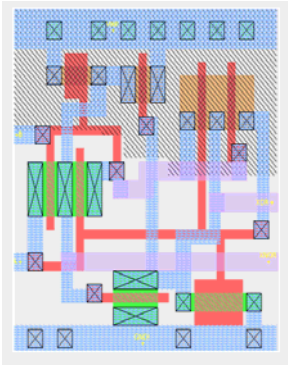


Figure 7. Layouts of the proposed circuit.

3. NOISE METRIC

In this paper, we use the noise immunity curves, NIC, [3] to measure the noise-tolerance of XOR-XNOR circuits. The noise immunity curve is The NIC of a digital gate is a locus of points (T_n, V_n) for which the gate just makes a logic error. All noise pulses below the NIC do not cause any errors. Hence, the higher the NIC of a gate, the less susceptible is the gate to noise.

For a quantitative value of noise immunity, a metric called *average noise threshold energy* (ANTE) is derived from the noise immunity curve. It is a measure that can be employed to compare the noise signature of various gates. This metric is given by:

$$ANTE = E(V^2_{noise} T_{noise})$$

where E( ) denotes the expectation operator. These noise metrics is widely implemented [7][8][10]. For simulation purposes, we generate a noise pulse using a noise injection circuit (NIC) [2]. The circuit basically is a tunable delay line to provide a noise pulse of the desired width and amplitude so as to produce a glitch in the output.

4. SIMULATION RESULTS

In this section, the performance of the proposed circuit is investigated. Noise-tolerance and circuit performance of the proposed XOR-XNOR are compared with the previously existing circuit shown in Figure 2. The reason that we picked this circuit for comparison is as stated before that it can operate at low supply voltage and has a good output levels.

The resulting noise immunity curves are shown in Figure 8. This figure shows that the NIC for the proposed XOR-XNOR is much higher than the compared one. As explained in the previous section, the higher the curve of the gate, the better noise-immune is the gate. This is because the safe area under the curve will be larger. Also, Table 1 shows the ANTE calculated from the NIC curve for both of the two circuits. The ANTE for the proposed circuit is 3.07 times better than the existing circuit under comparison.

Table 1. ANTE results

	Existing Circuit	Proposed Circuit
ANTE Value	14.043	43.162

The circuit performance of the two XOR-XNOR circuit configurations is evaluated in terms of worst-case delay, power consumption and power-delay product for all ranges of supply voltages (0.6v to 3.3v). The delay is calculated from 50% of voltage level of input to 50% of voltage level of resulting output for both rise and fall output transitions. Worst-case delay is chosen to be the larger delay among the two. The results are shown in Figure 9, Figure 10.

Figure 9 show that the proposed XOR-XNOR circuit is faster the existing one under any supply voltage. However, the propose circuit consumes more power but the power delay product is still better than the compared one as shown in Figure 10. Also, a 5-2 compressor circuit from [6], is built with the two XOR-XNOR circuits. This is done to compare the circuits comprehensively in a real application. The multiplexer used for the 5-2 compressor is shown in Figure 11. This multiplexer is widely used for carry output generation in fast full adders and multi-input compressors. Worst-case delay and power consumption is calculated at 1.8v V_{dd}. The results are shown in Table 2.

Table 2. Simulation results for 5 to 2 compressor.

	Existing Ckt	Proposed Ckt
Power Consumption (μW)	57.42	83.7
Worst-Case Delay (ns)	0.081	0.045
Power-Delay Product	4.65102	3.7665

It is clear that the architecture with the proposed circuit is approximately twice (1.8) but it consumes 45% more power. Also, the power delay product for the architecture with the proposed circuit is better than the compared one. In addition to these results, that architecture is much noise-immune as stated in section 4.

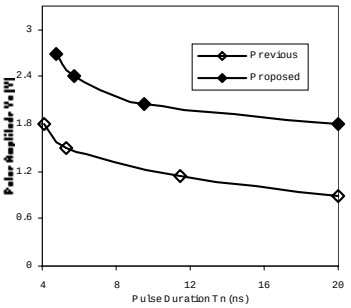


Figure 8. Noise immunity curves for the proposed XOR-XNOR and the compared one

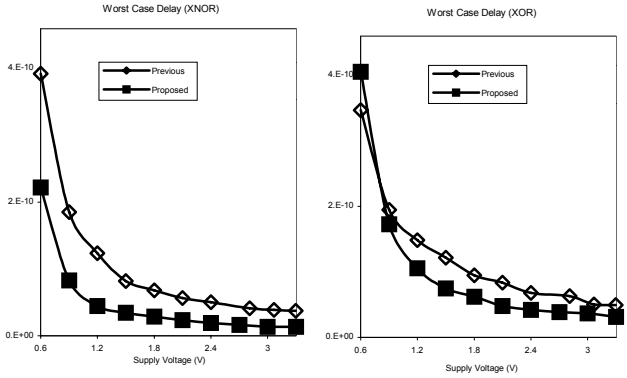


Figure 9. Worst case delay (XNOR), (XOR)

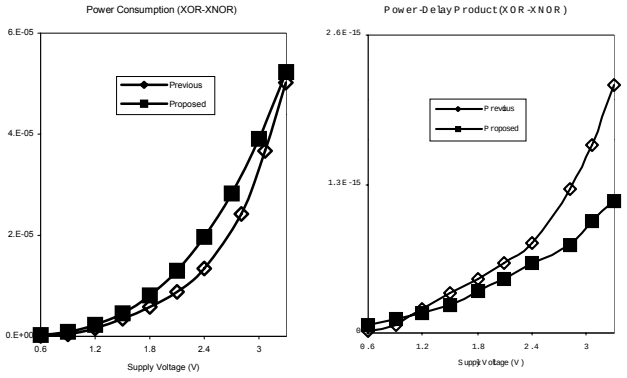


Figure 10. Power consumption and power-delay product (XOR-XNOR)

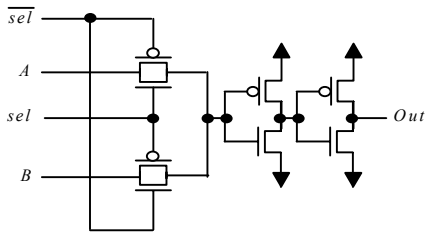


Figure 11. 2 to 1 Multiplexer cell

5. CONCLUSIONS

We have proposed and tested a noise-immune low voltage XOR-XNOR circuit. The circuit performance has been shown to outperform the compared one, which can operate at low-voltage, and has good output levels. The proposed circuit has been tested to be much noise-immune and faster than the compared one. The ANTE for the proposed circuit is 3.07 times better than the existing circuit under comparison. Also, the circuit has been tested inside a real environment. We picked the 5-2 compressor architecture to test the circuit inside it, as it is a critical component in any fast multiplier architecture. The power delay product for the architecture with the proposed circuit has been shown to outperform the one for the same architecture with the already existing XOR-XNOR.

6. ACKNOWLEDGMENTS

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7. REFERENCES

[1] D. Radhakrishnan. Low-voltage Low-power CMOS Full Adder. IEE Proc.-Circuits Devices Syst., Vol 148. No. 1, Fabryary 2001.

[2] G. Balamurugan and N.R. Shanbhag. The twin-transistor noise-tolerant dynamic circuit technique. IEEE Journal of Solid-State Circuits, vol. 36, no. 2.

[3] G.A. Katopis. Delta-I noise specification for a high-performance computing machine. Proceedings of the IEEE, vol. 73, pp. 1405-1415, Sept. 1985.

[4] Hung Tien Bui, A.K. Al-Sheraidah, Yuke Wang. New 4-transistor XOR and XNOR designs. Proceedings of the Second IEEE Asia Pacific Conference on ASICs, 2000,pp.25-28.

[5] Jyh-Ming Wang, Sung-Chuan Fang, Wu-Shiung Feng. New Efficient Designs for XOR and XNOR Functions on the Transistor Level. IEEE J. of Solid-State Circuits, Vol. 29, No. 7, pp.780-786, July 1994.

[6] K. Prasad, and K.K. Parhi. Low-power 4-2 and 5-2 compressors. Proceeding of the 35th Asilomar Conf on Signals, Systems and Computers, vol.1, pp. 129-133, 2001.

[7] L. Wang and N. R. Shanbhag. Noise-tolerant dynamic circuit design. Proc. of IEEE Intl. Symp. on Circuits and Systems, pp. 549-552, Orlando, FL May/June 1999.

[8] Mohamed A. Elgamel and Magdy A. Bayoumi. Noise tolerant low power dynamic TSPCL D flip-flops. 2002 IEEE Computer Society Annual Symposium on VLSI (ISVLSI'2002), April 25-26, 2002, Pittsburgh, Pennsylvania.

[9] Reto Zimmermann and Wolfgang Fichtner, "Low-Power Logic Styles: CMOS Versus Pass-Transistor Logic," IEEE Journal of Solid-State Circuits, Vol 32. No. 7, pages 1079 - 1090, July 1997.

[10] S. Goel, T. Darwish, M. Bayoumi. A Novel technique for noise-tolerance in dynamic circuits. IEEE Computer Society Annual Symposium on VLSI (ISVLSI'2003), February 20-21, 2003, Tampa, Florida, USA.