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*Lucian Stoica*

NON-COHERENT ENERGY  
DETECTION TRANSCEIVERS  
FOR ULTRA WIDEBAND  
IMPULSE RADIO SYSTEMS

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DEPARTMENT OF ELECTRICAL AND INFORMATION ENGINEERING,  
CENTRE FOR WIRELESS COMMUNICATIONS,  
INFOTEC OULU,  
UNIVERSITY OF OULU





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C Technica 292

*LUCIAN STOICA*

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## **Stoica, Lucian, Non-coherent energy detection transceivers for Ultra Wideband Impulse radio systems**

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### ***Abstract***

The focus of this thesis is Ultra Wideband (UWB) Impulse Radio (UWB-IR) transmitters and non-coherent receivers. The aim of the thesis is to investigate, analyze and design UWB-IR transmitter and receiver structures both from a theoretical and circuit design viewpoint.

An UWB-IR transmitter structure is proposed and is the subject of a detailed investigation. The transmitter generates a Gaussian monocycle and can be modified to generate a family of Gaussian waveforms. The Gaussian monocycle is easy to generate while providing good bit-error-rate (BER) performance. The Gaussian monocycle has a wide -10 dB bandwidth and a zero-DC component which does not decrease antenna efficiency. The transmitter design includes a delay locked loop (DLL) based frequency synthesis approach. The advantage of using a frequency synthesis approach based on a DLL is based on the fact that a DLL generates less noise than a phase locked loop (PLL) and is inherently stable. The generated pulse has a width of less than 350 ps and a -10 dB bandwidth of 4.7 GHz. The power consumption of the designed UWBIR transmitter is 20 mW at a voltage supply of 3.3 V. Compared with other integrated UWB-IR transmitters, the transmitter presented in this thesis has the lowest pulse width for comparable integrated processes, one of the lower power consumptions and a low die area.

The BER performance of several UWB-IR non-coherent receiver structures is presented. The energy detection (ED) receiver offers the same BER performance as the transmitted reference scheme with binary pulse amplitude modulation (BPAM) but has a lower implementation complexity since it does not require an analogue delay line in its structure.

Circuit performance of several blocks of the ED receiver is presented. The radio frequency (RF) front-end and analogue baseband sections of the receiver have been designed as an integrated circuit (IC) in a 0.35  $\mu\text{m}$  bipolar complementary metal oxide semiconductor (BiCMOS) process. The RF front-end section includes a low noise amplifier (LNA), a variable gain amplifier (VGA) and a Gilbert cell. The LNA has a noise figure (NF) of less than 3 dB, a gain of 18 dB in the interest bandwidth and less than 20 mW of power consumption. The NF of the LNA can be reduced even further at the expense of a higher power consumption or by using input pads with lower capacitance values. The noise figure can be also lowered by using a process which provides transistors with higher transit frequency ( $f_T$ ). Trading-off power consumption for noise is still a key design issue in the design of integrated UWB-IR receivers.

The analogue baseband section includes a bank of integrators and a 4-bit analogue to digital converter (ADC). The ADC is running at a sampling rate equal to the symbol rate and takes only 2 mW of power at 3.3 V supply. The power consumption of the designed integrated front-end and analogue baseband receiver sections is 117 mW at a power supply of 3.3 V.

The digital baseband of the receiver have been implemented on a field programmable gate array (FPGA) technology. The power consumption of the baseband is 450 mW with a power supply of 1.2 V and a maximum supply of 3.3 V for input-output pins.

The total power consumption of the designed transceiver is 587 mW. When compared with other UWB receiver architectures, the energy detection receiver has the lowest power consumption due to the low power consumption of the LNA, simple synchronization architecture and low sampling rate of the ADC.

*Keywords:* energy detection, Gaussian monocycle, impulse radio, low noise amplifier, ultra wideband



*To my family*





## Preface

Research for this thesis has been carried out at the Centre for Wireless Communications (CWC), University of Oulu, Finland. I joined the CWC in March 2003 where I started my postgraduate studies. Having Dr. Ian Oppermann as a supervisor of my research work was truly a privilege and I would like to thank him for that. His high research standards and technical precision will always remain my professional goals. I thank Professor Matti Latva-aho for all support, advice and encouragements I received from him during my study years.

Most of the work presented in this thesis was conducted in the Ultra Wideband RF-AASIC (URFA), UWB Wireless Embedded Networks (UWEN) and Pervasive Ultra wideband Low Spectral Energy Radio Systems (PULSERS) projects.

I would also like to thank other colleagues, most of which are from the UWB group, Alberto Rabbachin, Sakari Tiuraniemi, now with CERN, and Heikki Repo, now with Embio. Special thanks to Professor Timo Rahkonen, from the Electronics Laboratory, for his review of the first version of the UWB-IR IC transceiver I have worked. The discussions with him have been inspiring and informative.

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During my postgraduate studies I had the privilege of being a student in the Infotech Oulu Graduate School as well as in three research projects. The financial support of Nokia, TEKES, the National Technology Agency of Finland, on these projects is gratefully acknowledged. I am also thankful to Elisa Communications foundation and Nokia Foundation for their financial support.

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My warmest gratitude belongs to my lovely wife Iulia for all the sincere love, support and understanding she had for me throughout all these years. Our children Victor-Markku and Diana-Aleksandra disconnected me from any thesis related troubles the moment I come home. Their support has been my solid ground to stand on.

## List of symbols and abbreviations

$a_i$	incident normalized power wave
$A_n$	amplitude
$b_i$	reflected normalized power wave
$B_{-10}$	-10dB bandwidth
$B_f$	fractional bandwidth
$B_w$	bandwidth
$B_R$	resolution bandwidth
$C$	channel capacity
$C_{loop}$	loop filter capacitor
$c_j$	momentary code phase
$d$	distance
$d_k$	$k$ -th data bit
$E_b$	energy of bit
$E_b/N_0$	bit energy per noise power ratio
$E_p$	energy of a single pulse
$f_c$	center frequency
$f_h$	higher frequency limit
$f_l$	lower frequency limit
$f_m$	offset frequency
$f_{max}$	maximum oscillation frequency
$f_o$	output frequency of the cock multiplier block
$f_T$	transit frequency
$g_{ds}$	output conductance
$G_{RX}$	receiver antenna gain
$G_{TX}$	transmitter antenna gain
$I_{pump}$	charge pump current
$IIP_3$	input third order harmonic intercept point
$IPI$	inter-pulse interference
$ISI$	inter-symbol interference
$j$	index, transmitted bit
$k$	index

$K_D$	phase detector gain
$K_F$	charge pump-loop filter gain
$K_V$	voltage controlled delay line gain
$L$	number of resolvable multipath
$L_{ch}$	electrical channel length of a CMOS device
$L_1$	path loss at 1m
$L_2$	path loss at 3m
$n$	path gain
$N_{collide}$	collide frame
$N_{0bit}$	average noise power per bit
$N_{bit}$	preamble length
$N_{int}$	number of integrators
$N_p$	number of pulses
$N_u$	number of users
NF	noise figure
$NF_{min}$	minimum noise figure
$N_0$	one sided power spectral density white Gaussian noise
<i>OFF</i>	closed switch
<i>ON</i>	open switch
$P_b$	bit error probability
$P_N$	average noise power
$P_{RX}$	received power
$P_{TX}$	transmitted power
PG	processing gain
$r_b$	base resistance
R	data rate
$R_A$	antenna resistance
$R_g$	generator resistance
$R_L$	antenna loss resistance
$R_T$	load resistance
s(t)	transmitted signal
$s_r(t)$	received signal
$S_\Phi$	phase noise
$S_{11}$	input reflection coefficient
$S_{21}$	forward voltage gain

$S_{12}$	reverse voltage gain
$S_{11}$	output reflection coefficient
$Q$	quality factor
$QoS$	quality of service
$t$	time
$t_{ox}$	gate-oxide thickness of a CMOS device
$T_c$	chip length
$T_d$	symbol length
$T_{PRF}$	frame length
$T_p$	pulse width
$T_{ref}$	reference clock period
$T_{OUT}$	output clock period
$T_s$	symbol length
TW	time-bandwidth product
$X_A$	antenna reactance
$X_g$	generator reactance
$Y_1$	observation variable
$Y_2$	observation variable
$Z_A$	antenna impedance
$X_T$	load reactance
$Z_0$	$50\Omega$ impedance
$Z_{in}$	input impedance
$w_{TR}$	transmitted pulse
$\alpha$	multipath gain coefficient, effective channel
$\beta$	modulated symbols
$\delta$	Dirac's delta function
$\lambda$	wavelength, arrival rate of paths
$\Lambda$	cluster arrival rate
$\sigma_l$	standard deviation parameter
$\sigma_{th}$	threshold matching parameter
$\tau_n$	delay
$\omega_{if}$	intermediate angular frequency
$\omega_{LO}$	local oscillator angular frequency
$\omega_{rf}$	angular frequency
AC	auto-correlation

ADC	analogue to to digital converter
AFOM	analogue figure of merit
ALT	alternate
AMPS	advanced mobile phone system
AMS	AustriaMicrosystems
ARAKE	all rake receiver
AWGN	additive white Gaussian noise
BER	bit error rate
BiCMOS	bipolar complementary metal oxide semiconductor
BPAM	binary pulse amplitude modulation
BPF	bandpass filter
BPM	bit position modulation
BPAM	binary pulse amplitude modulation
BPSK	binary phase shift keying
CEPT	European Conference of Postal and Telecommunications Administra- tion
CM	channel model
CMFB	common mode feedback
CMOS	complementary metal oxide semiconductor
CMRR	common mode rejection ratio
DAA	detection and avoidance
DARPA	Defense Advanced Research Projects Agency (USA)
DB	doublet based
DC	direct current
DD	delay detector
DECT	digital enhanced cordless telecommunications
DH	delay hoped
DLL	delay locked loop
DS	direct sequence
DS - SS	direct sequence spread spectrum
DVI	digital visual interface
EC	European Commission
ECC	Electronic Communications Committee
ED	energy detection
EGC	equal gain combining

EIRP	equivalent isotropic radiated power
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
FIR	finite impulse response
FM	frequency modulation
FPGA	field programmable gate array
GPS	global positioning system
GSM	global system for mobile communications
HBT	heterojunction bipolar transistor
IC	integrated circuit
IR	impulse radio
IEEE	Institute of Electrical and Electronics Engineers
ITU	International Telecommunication Union
LNA	low noise amplifier
LO	local oscillator
LOS	line of sight
LPD	low probability of detection
LPI	low probability of interception
OFCOM	Office of Communications (UK)
OFDM	orthogonal frequency division multiplexing
OOK	on-off keying
OTA	operational transconductance amplifier
MAI	multiple access interference
MAC	medium access control
MBOA	multiband-orthogonal frequency division multiplexing alliance
MB-OFDM	multiband orthogonal frequency division multiplexing
MCS	modulation and coding scheme
MIC	Ministry of Internal Affairs and Communications (Japan)
MII	Ministry of Information Industry (China)
MPC	multipath components
MRC	maximum ratio combining
NBI	narrow band interference
NESP	normalized effective signal power
NICT	National Institute of Information and Communication Technology (Japan)
NLOS	non-line-of-sight

PAM	pulse amplitude modulation
PAN	personal area network
PCSNIM	power constrained noise optimization technique
PDP	power delay profile
PHY	physical layer
PLL	phase locked loop
PPM	pulse position modulation
PRAKE	partial rake receiver
PRF	pulse repetition frequency
PSD	power spectral density
PSM	pulse shape modulation
PVT	process-voltage-temperature variations
RF	radio frequency
RMS	root mean square
RO	The First Report and Order (FCC, USA)
RX	receiver
SiGe	silicon-germanium
SNR	signal-to-noise ratio
SOC	system-on-a-chip
SOP	system-on-package
SR	single reference
SRAKE	selective rake receiver
SRD	step recovery diode
SRMC	state radio monitoring center (China)
SS	spread spectrum
SV	Saleh-Valenzuela channel model
TG	task group
TH	time hopping
TOA	time-of-arrival
TR	transmitted-reference
TSMC	Taiwan Semiconductor Company
TX	transmitter
UMTS	universal mobile telecommunications system
USAF	United States Air Force
USB	Universal Serial Bus



UWB	ultra wideband
VCDL	voltage controlled delay line
VCO	voltage controlled oscillator
VGA	variable gain amplifier
VHDL	very high speed integrated circuits hardware description language
WCDMA	wideband code division multiple access
WG	work group
WPAN	wireless personal area network



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# 1 Introduction

*"The best way to predict the future is to invent it." –Alan Kay*

Wireless communications have become a very important part of people's everyday life. The development of wireless technologies is already evident in the success of cellular telephony and wireless local area network (WLAN) applications. The integration of short range devices and networks, based on wireless standards within the IEEE802 suite, into the wireless wide-area infrastructure is far from trivial. Furthermore, new and increasingly challenging requirements constantly emerge from the user side: availability of high-rate data access, long battery life, location and tracking capabilities, and applications offering undisrupted service across different networks. As more and more devices go wireless, future wireless technologies will face spectral crowding and coexistence of wireless devices will be a major issue. Therefore, considering the limited bandwidth available, accommodating the demand for higher capacity and data rates is a challenging task, requiring innovative technologies that can coexist with devices operating at various frequency bands.

## 1.1 Background for UWB Communication

Ultra-Wideband (UWB) communication systems have the potential to provide solutions for many of today's challenges in the area of wireless communications and spectrum management. The approach employed by UWB communication systems is based on sharing spectrum already occupied by other wireless services, by using the overlay principle, rather than identifying still available new bands.

The main advantage of UWB technology can be perceived from Shannon's link capacity formula (97):

$$C = B \log_2(1 + SNR). \quad (1)$$

The link capacity is linearly proportional to the bandwidth and has a logarithmic relationship with the signal to noise ratio (SNR). Therefore, when the bandwidth is extremely large, only a very small signal power is needed to achieve high data rates. With its wide bandwidth, UWB has the potential to offer capacity much higher than the current narrowband systems for short-range applications.

Sensor networks are characterized by low complexity devices that have limitations

on memory and processing power, and restrictions on power consumption. Traffic in sensor networks is bursty with long periods of no activity. For the devices deployed, this has significant implications to the design of efficient medium access protocols, radio frequency technology and the reliability of information transfer (7).

In particular impulse-radio-based (IR) UWB communication systems have noise like-signals, are potentially low complexity and are resistant to severe multipath and jamming. UWB-IR signals have fine time domain resolution allowing for location and tracking applications (75). The low cost and low complexity of UWB-IR systems emerge from the baseband nature of the signal transmission. Unlike classical radio systems, the UWB-IR transmitter produces a very short time domain pulse without the need for an up-conversion mixing stage. The very wideband nature of the UWB signal means that it spans frequencies commonly used as carrier frequencies by existing wireless services. Also, the UWB-IR receiver does not require a down-conversion stage. This means that a local oscillator in the receiver can be omitted, which leads to removal of associated complex phase locked loop (7). As a result UWB-IR transceivers can be implemented in low cost complementary metal oxid-semiconductor (CMOS) or bipolar CMOS (BiCMOS) integrated circuit technologies (21), (73), (44).

The power consumption of UWB-IR devices can be reduced by integration, device scaling and low complexity transmitter and receiver architectures. The tradeoff between tighter variation of devices parameters and better yield, is one of the most important debates today between circuit designers and process engineers (90). From the signal processing viewpoint, the robustness of non-coherent receivers in multipath environments has been proven in open literature (85), (82), (98).

Low data rate UWB-IR is a good candidate for ad-hoc sensor network applications that utilize multi-hop data routing. Using multi-hop routing, UWB-IR transmitters could reduce their power emissions and thus also their coverage area allowing a large number of transmitters to operate simultaneously in the same given area, yielding increased spectral reuse and resulting in higher capacity per area. Thus, UWB based short range wireless communications provide high-spatial-capacity networks. Besides the ability to operate across bands occupied by existing narrowband systems, UWB radio systems offer flexibility in that they can maintain spatial capacity by adapting to either a large number of low-rate devices or a small number of high-rate devices, depending on the requirements of the application. It is not only the data throughput that benefits from the wide bandwidth, but also the ranging resolution of a communication system. The standard deviation of the timing resolution  $\sigma_t$ , which is inversely propor-

tional to that of bandwidth  $B$ , can be expressed as (112):

$$\sigma_r = \frac{1}{2B\sqrt{SNR}}. \quad (2)$$

The increase of bandwidth decreases the  $SNR$  necessary to achieve a certain resolution.

Due to the wide bandwidth of the transmitted signal, very high multipath resolution can be achieved. Impulse radio based UWB systems offer good LPI/LPD (low probability of interception/detection) properties which make it suitable for secure and military applications. UWB-IR is a natural choice for wireless sensor networks (WSN) with location and tracking due to the intrinsic properties of the signal, specifically short pulses supporting a high resolution of signal ranging estimation. Together with good through obstacle imaging, UWB signals offer opportunities for short range radar applications such as vehicular radar, collision avoidance, medical imaging, surveillance, mining, rescue and anti-crime operations. UWB-IR offers frequency diversity and suffers from severe multipath fading channel effects (7), (98).

Unintended detection of UWB signals is difficult due to the low energy density of the transmitted signal. There is evidence in the open literature that UWB-IR signal transmissions do not cause significant interference to existing radio systems if the distance between the victim receivers and UWB-IR transmitter is larger than few tens of centimetres (38), (40), (41). The results of the interference studies between UWB-IR transmitters and existing radio systems is the subject of heated debate between advocates and opponents of UWB.

## 1.2 Historical Review of UWB Technology Development

UWB is seen as having potential for realizing exciting new applications that have not been fulfilled by other wireless short range technologies e.g., 802.11 local area networks (LANs) and Bluetooth personal area networks (PANs). Correspondingly, there has been a recent upsurge of interest in academic research into UWB as evidenced by (1), (2), (3) and an annual conference solely dedicated to UWB systems and technology (4). UWB-IR wireless communication systems utilize very short time domain pulses for transmission that result in a very wide spectrum signal. The use of UWB signals date back to the beginning of the last century with the spark-gap transmission experiments of Hertz (62). The era of spark-signals ended when the superiority of the continuous wave over spark signals was evident. The invention of Armstrong's regenerative receiver and sequently super-heterodyne receiver in 1917 effectively put a halt to spark gap

communications (62).

The use of modern UWB technology started in the 1960's with a focus on development of impulse radars that used wideband signals primarily for extremely accurate localization and imaging in the context of secure communications. By the early 1970's, the basic components of UWB systems were already known, e.g., pulse generators and modulators, switching pulse train generators, detection receivers and ultra wideband antennas. The first systems which make use of the UWB technology were radars. In April 1973, Ross was granted the US Patent 3,728,632 which has been seen as the start for UWB communication systems (92). After the 1970's, the main innovations in the UWB field come from improvements of specific implementations of subsystems, but not in the system concept itself nor in the subsystems concepts (15). A summary of pulse generation methods in 1978 is presented in (17). After the 1970's, the emphasis was put on implementation of the known technology, and understanding the implications of transmitting short duration pulses on existing RF communication systems.

During the years from 1977 to 1989, the United States Air Forces (USAF) conducted a research program in UWB systems whose results were then used by the Defense Advanced Research Projects Agency (DARPA). The term UWB was applied in 1990 by the US Department of Defence. Some early work on UWB were conducted by Scholtz and his group in the early 1990s, focusing mainly on low-rate applications (95), (96), (129), (130). Recent developments in semiconductor manufacturing processes and narrow-band pulse generation has prompted new studies into UWB signal generation for different purposes: low speed, low cost, short range communications in support of a variety of multimedia transport applications in home and office environments.

Non-coherent UWB-IR receiver structures have lately been the focus of intense study. Auto-correlation (AC) receivers have been considered in (42), (25), (83), (117), (131). Transmitted-reference (TR) receivers have been considered in (42), (36). Energy detection receivers have been addressed in (85), (82), (106), (120), (94), (104).

US companies like Time Domain (74), Multispectral Solutions (32) and Alereon have presented various transmitter and receiver architectures enabling data communication and radar applications. Lately, companies from Europe and Japan, like Philips, STM and Sony have presented designs of IC UWB-IR transceivers (44), (101).

IEEE established two task groups to work on UWB physical layer (PHY) standardization: one responsible for the high data rate applications (IEEE802.15.3a) and one responsible for low data rate applications (IEEE802.15.4a). The main focus of the IEEE802.15.4a group is to define the PHY and medium access control (MAC) sub-



layer specifications for low data rate wireless connectivity with fixed, portable, and low mobility devices with low power consumption requirements typically operating in the personal area space of 10 m. The standardization activity of the IEEE802.15.4a group is currently ongoing and summaries and reports are available in (43).

The IEEE established the 802.15.3a High Rate Alternative PHY Task Group (TG3a) for Wireless Personal Area Networks (WPANs) to define a new PHY concept for short range, high data rate applications. Debate inside the IEEE 802.15.3a group raged over two competing PHY proposals: Direct-sequence UWB (DS-UWB) proposal employing short RF pulses for transmission; and Multiband Orthogonal Frequency Division Multiplexing (MB-OFDM) proposal that combines the multi-band approach (splitting the total available bandwidth into sub-bands) together with the OFDM techniques to achieve high-rate transmission.

The MB-OFDM proposal is supported by Intel and Texas Instruments and more than 80 companies (6). Companies which support the MB-OFDM technology have subsequently formed the WiMedia Alliance. The DS-UWB proposal was driven by Freescale and NICT (5). The major supporters of DS-UWB technology formed the UWB Forum. The solutions demonstrated by the Freescale platform ranged from wireless USB 2.0 over UWB, Bluetooth Wireless Technology over UWB, wireless DVI component video, 1394-over coax via UWB and UWB HDTV over electrical wire.

A split formed in early 2004, when WiMedia left the IEEE 802.15 Task Group 3a, after failing to gain the 75% vote needed to become the standard. Neither the DS-UWB or multi-band (MB)-OFDM alternatives received backing from the IEEE 802.15.3a. The IEEE802.15.3a group ceased to exist in January 2006 due to the failure to define an UWB PHY standard (50).

The Center for Wireless Communications (CWC) was strongly involved in the IEEE 802.15.4a standardization activities, and has proposed the energy detection transceiver architecture during this process.

### **1.3 Author's Contribution**

The UWB-IR energy detection transceiver has been design to support research projects at CWC including that related to standardization activities, and to show that the concept of energy collection is feasible in practical environments. The main research area of the thesis covers low complexity, low data rate UWB impulse radio transceiver design from both a communication and circuit design viewpoint. At the time of writing,

there was no other example of a complete implementation of a UWB-IR non-coherent ED transceiver. The study has been carried out by analysis and experimental methods. The analytical part is divided between simulations and theoretical calculations. Comprehensive circuit level simulations have been performed to determine the impact of different circuit sections on the performance of the UWB transceiver. Measurements of several blocks of the energy detection transceiver have been carried out. In addition, the performance from a wireless communication perspective of different UWB-IR transceivers have been simulated. It was determined that the low complexity energy detection receiver offers good performance compared to other coherent and non-coherent structures.

The author has been involved in the design of the transceiver circuit blocks by specifying its structure, designing circuits for the transceiver, defining the simulation and measurements setups and analyzing the results. In addition, the author was the main contributor to the journal and conference publications used as the original papers in this thesis.

Papers (75), (102), (109), (84), (108), (107), (110), investigate the implementation of a time-hopping pulse position modulation design in a FPGA technology, the architecture of an UWB-IR non-coherent energy collection receiver for low data rate, low cost applications, the schematic block diagram of an improved UWB Gaussian pulse generator and the circuit details of the energy collection receiver. In paper (106), the architecture and performance of an UWB system architecture designed for low data rate, low-cost sensor networks applications was presented. In papers (105) and (103), the performance of time-of-arrival (TOA) position estimation techniques as well as the simulated and measured performances of an UWB-IR non-coherent energy collection receiver is shown. An overview of UWB-IR auto-correlation and energy detection receivers has been presented in paper (104).

## **1.4 Outline of the Thesis**

The thesis is organized as follows: Chapter 2 presents a comprehensive literature review of related work on UWB pulse shapes and transmitter structures. Reviews of UWB-IR transmitters structures and circuit implementations are given in more detail. Chapter 2 provides the motivation for implementation of the Gaussian monocycle transmitter. Chapter 3 presents an overview of UWB-IR receivers structures. Reviews of UWB-IR receivers structures and circuit designs are given in more detail. UWB-IR non-coherent

receiver structures, which are considered in more detail throughout the thesis, are also described. Chapter 3, which incorporates Paper (106), presents the performance of different UWB-IR non-coherent receivers from communication systems viewpoint. The theoretical performance versus implementation complexity challenges of UWB-IR receivers is presented. Chapter 3 provides the motivation for the implementation of the ED receiver. Chapter 4, which incorporates Papers (107) and (108), presents the design of an UWB-IR Gaussian pulse transmitter. The circuit implementation details are presented. Chapter 5, which is in part presented in Papers (84), (107) and (109), presents the design of several blocks of an UWB-IR non-coherent energy detection receiver. Chapter 6 concludes the thesis and the main results are summarized and discussed.



## 2 Overview of UWB Signals and Transmitter Structures

This chapter presents a literature review of different UWB-IR waveforms and transmitters architectures. The overview of the transmitters is presented from both a theoretical and implementation viewpoint. Section 2.1 gives the general introduction and a brief system description of a wireless communication system. Section 2.2 presents the UWB standardization efforts in the United States and Europe. Section 2.3 presents the FCC spectral limits for UWB-IR communication systems.

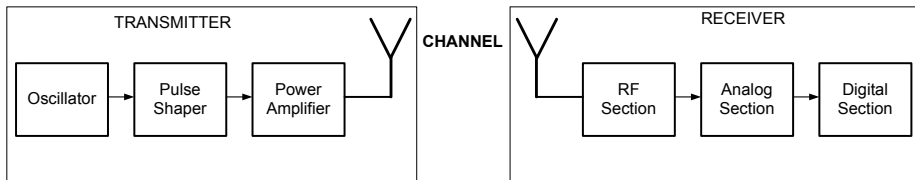
Section 2.4 shows various pulse shapes and their spectral properties. Sections 2.5 gives a performance overview of integrated and discrete UWB-IR transmitters. Section 2.6 presents the conclusions of Chapter 2.

### 2.1 Introduction

The diagram shown in Figure 1 illustrates the signal flow through a typical UWB-IR wireless communication system. This figure can serve as a guide through the chapters of this thesis. The transmitter section includes the oscillator, the pulse shaper, the power amplifier and the antenna. The oscillator represents the signal source for the pulse shaper. The pulse shaper generates the waveform to be used for communication. The pulse shaper may use either the signal at the oscillator's frequency or at a multiple of the oscillator's frequency. In the latter case, a frequency multiplier is used. The frequency multiplier may be integrated into the oscillator. The power amplifier amplifies the pulse shape to the desired transmit power level. The UWB antenna filters the transmitted signal. In some studies, the ideal UWB antenna behaviour is modelled as a differentiator, however other authors are not willing to accept this simplifications (86), (122). In (122), the authors show that the transmitted far field waveform is a scaled version of the voltage across the radiation resistor in the antenna model. The approach from (122), verifies that operating the antenna close to the first resonant frequency is still the optimal approach in terms of power match and nondispersive transmission. The receiver portion consists of an antenna, an RF section, an analogue section and a digital section. The receiver's antenna will again filter the incoming signal. The RF section consists of a bandpass filter (BPF), low noise amplifier (LNA), variable gain amplifier (VGA)

and squaring operation. The analogue section consists of all the analogue processing circuits, after the signal's down-conversion to baseband. The digital section consists of all the digital baseband algorithms, e.g., for data detection and synchronization.

Due to its overlaying nature, UWB systems share the existing spectrum with already defined radio systems. The main scope of regulatory masks is to define the dedicated bands where the UWB signals can coexist with the licensed wireless services in use. Therefore, the existing UWB spectral masks have a direct impact over the transmitted signals in UWB communication systems. Several pulse shapes which satisfy the FCC spectral masks, have been proposed in the literature (64), (99), (23). Among the waveforms presented, the Gaussian pulse and its derivatives, satisfies the FCC spectral mask while presenting a low implementation complexity. Since the central frequency of the Gaussian waveforms increases with the derivative order of the pulses, the allocated spectrum is used more efficiently.



**Fig 1. Schematic Diagram of the UWB Communication System.**

## 2.2 UWB Standardization and Spectrum Regulation

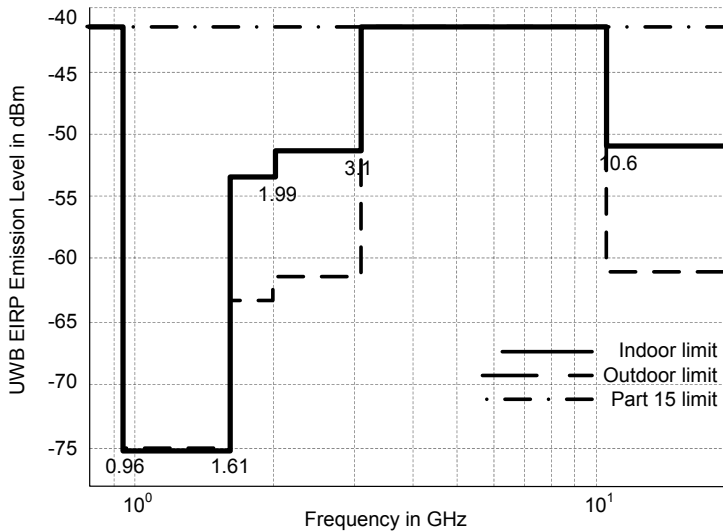
UWB has the potential to offer new solutions to the problem of spectrum management, based on sharing the existing radio spectrum resources rather than looking for new bands. This idea was recently supported by the Federal Communications Commission (FCC) in the United States. The USA started the standardization of UWB in 1998 when the FCC released the "Notice of Inquiry" addressing possible use of UWB technology (28). The FCC radiation mask was released in February 2002 as "The First Report and Order" (RO). The RO allowed commercialization of UWB technology if the UWB radiation adheres to the spectrum mask.

According to (29), a signal was defined as being an UWB signal if its fractional

bandwidth,  $B_f$ , was greater than 0.25, where the definition of  $B_f$  is provided by (111):

$$B_f = 2 \frac{f_h - f_l}{f_h + f_l}, \quad (3)$$

where  $f_h$  and  $f_l$  are the higher and lower  $-10$  dB frequencies, respectively. A signal is also defined as being UWB if the  $-10$  dB signal bandwidth is 500 MHz or larger (39). The frequency bands allowed for UWB operation are below 960 MHz, the 3.1 - 10.6 GHz band, and the 22 - 29 GHz band depending on the type of application. The existing FCC radiation limits for different indoor and outdoor UWB applications are presented in Figure 2. In Figure 2, the Part 15 limit was included as a reference, where Part 15 limit permits the operation of authorized low power radio frequency (RF) devices without a license from the Commission or the need for frequency coordination under general emissions limits (30).



**Fig 2. FCC Indoor Mask and Part 15 limit.**

The FCC indoor mask sets higher emission limits in the band 2 - 3.1 GHz and above 10.6 GHz. For outdoor emission, the maximum EIRP level in the 3.1 - 10.6 GHz band is set to  $-41.3$  dBm/MHz and to  $-61.3$  dBm/MHz above 10.6 GHz. For indoor emission, the maximum EIRP level in the 3.1 - 10.6 GHz band is set to  $-41.3$  dBm/MHz and to  $-51.3$  dBm/MHz above 10.6 GHz. All UWB devices must meet this spectral mask for

legal operation. References (29) and (30) describe the use of UWB technology in toys, aircraft and satellites or in fixed outdoor links.

In Europe, the European Commission Committee (ECC) has twice mandated the European Conference of Postal and Telecommunication Administration (CEPT) to harmonize all the UWB standardization activities within the EU area. The results of the first public inquiry were released in October 2004 (27). The UWB radiation limits are much more complex and sets much lower permitted power levels than the FCC's mask and so is far more difficult to meet for UWB-IR devices. In 2005, the ECC proposed in (27) a detection and avoidance mechanism (DAA) which should allow UWB devices to reduce their own transmit signal power if another signal is detected in the same frequency band. Radiation is allowed in the band 3.1 - 4.95 GHz if the activity factor is 5% or less over one second, or 0.5% over one hour. The use of the 4.1 - 4.8 GHz band is allowed until June 2010 since the upcoming fourth generation (4G) mobile cellular systems are expected to create additional demand on these frequency bands. The ECC is still waiting for comments from academia and industry to the draft report proposed in (27).

At the time of the writing (August 2007) UK, China and U.S are the only countries in the world which allow commercialization of license free UWB systems.

## 2.3 Transmitted Signal Requirements in UWB Communication Systems

The existing FCC mask regulation in the USA allows transmission of UWB signals below 960 MHz and within the 3.1 - 10.6 GHz band. The FCC indoor spectral mask sets the maximum EIRP level to  $-41.3$  dBm/MHz in the 3.1 - 10.6 GHz band. EIRP is defined by the product of the available power of the transmitter  $P_{TX}$ , that is the maximum power that the transmitter can transfer to the transmitter antenna, and the gain off the transmitter's antenna  $G_{AT}$ .  $P_{TX}$  is an average power computed by averaging over the bit interval  $T_b$ , as shown in (16):

$$P_{av} = \frac{N_s E_p}{T_b} = \frac{E_p}{T_s}, \quad (4)$$

where  $E_p$  is the energy of a single pulse,  $N_s E_p$  is the total energy of  $N_s$  the pulses representing one bit. Equation 4 shows that different pulse waveforms may have the same average power with big difference in pulse energy, depending on the number of pulses per bit. For equal waveform duration, the maximum instantaneous power may be signif-



icantly different among waveforms with similar average power. Utilization of the entire spectrum assigned by the FCC requires transmitter and receiver circuits with very fast frequency response, increasing the implementation complexity and decreasing the communication range due to the increasingly lossy nature of high frequency bands. When only a fraction of the bandwidth is used, the narrow band interference (NBI) suppression is improved. Pulse shaping is crucial since it affects the PSD of the transmitted signal. The transmitted spectrum can be shaped by changing the pulse waveform. The spectrum may be shaped by pulse width variation, pulse derivation, and combination of base functions. Among the most common waveforms are the pulses based on the baseband Gaussian pulses since their spectral properties satisfy the indoor FCC mask.

The spectral utilization efficiency of Gaussian pulses can be measured in terms of the normalized effective signal power (NESP) (7), (64), which is the ratio of the power transmitted in the designated passband of the spectral mask over the total power that is permissible under the given mask. The higher the derivative order of the Gaussian pulses, the higher the number of zero crossing in the same pulse width, acting as if a higher "carrier" frequency sinusoid is modulated by an equivalent Gaussian envelope. Therefore, as the order of the derivative increases, the allocated spectrum is used more efficiently. In section 2.4, we present different pulse shapes which adhere to the indoor FCC mask.

## 2.4 UWB Pulses

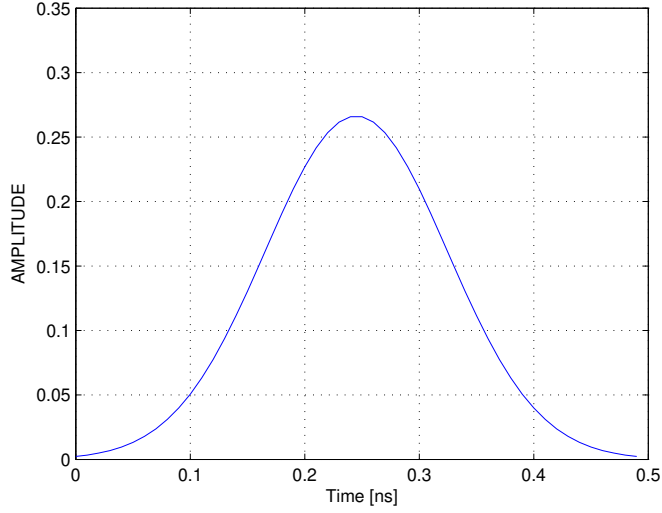
A suitable pulse waveform can be any function which satisfies the spectral mask limitations. Among the most common pulse shapes are the Gaussian, Rayleigh and mono-cycle waveforms. The Gaussian waveform is given by equation (5) (74). The nominal centre frequency and the bandwidth of the Gaussian pulse depends on the pulse's width in time.

$$p_{G_0}(t) = \frac{1}{\sigma\sqrt{2\pi}} \exp\left(\frac{-t^2}{2\sigma^2}\right). \quad (5)$$

By differentiating  $p_{G_0}(t)$  against  $t$ , the Gaussian pulse derivatives can be obtained. The  $n^{th}$  derivative is given by:

$$p_{G_n}(t) = \frac{d^n}{dt^n} p_{G_0}(t). \quad (6)$$

The Gaussian pulse with a pulse duration of 0.5 ns is presented in Figure 3.



**Fig 3. Gaussian Pulse with a 0.5 ns Pulse Duration.**

The theoretical formulation of the first derivative of the Gaussian pulse, namely the Gaussian monocycle, is presented as:

$$p_{G_1}(t) = -\frac{te^{-\frac{t^2}{2\sigma^2}}}{\sqrt{2\pi}\sigma^3}. \quad (7)$$

The nominal centre frequency and the bandwidth of the first derivative of the Gaussian pulse, known also as the Gaussian monocycle, depends on the monocycle width in time. The  $-3$  dB bandwidth is approximately 116% of the monocycle's centre frequency  $f_c$  (113). The ideal Gaussian monocycle has a single zero crossing in the time domain. The spectrum decays with increasing frequency, but does not ever reach DC implying an infinite spectrum signal and therefore an finite time domain signal. From an implementation viewpoint, infinite duration pulses cannot be used. The pulse width or duration of the pulse can be defined as:

$$T_p = \sqrt{2\pi}\sigma, \quad (8)$$

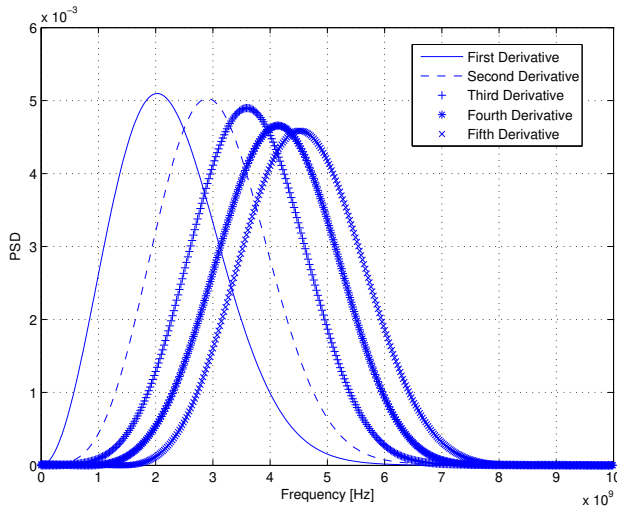
where  $\sigma$  is the variance of the Gaussian distribution. Outside the interval  $(-T_p/2, T_p/2)$ , the pulse must be nulled for practical implementation purposes.

The Fourier transform is calculated in order to obtain the spectrum of the impulses used in UWB transmissions. In Table 1, the first and second UWB Gaussian derivatives and their frequency spectrum are presented.

**Table 1. UWB Gaussian Derivatives.**

Theoretical formula	Frequency spectrum	Central frequency
$p_{G_1}(t) = \frac{t e^{-\frac{t^2}{2\sigma^2}}}{\sqrt{2\pi\sigma^3}}$	$P_{G_1}(f) = 2j\pi f e^{-2(\pi\sigma f)^2}$	$f_0 = \frac{1}{T_p}$
$p_{G_2}(t) = \frac{1 - \frac{t^2}{\sigma^2}}{\sqrt{2\pi\sigma^3}} e^{-\frac{t^2}{2\sigma^2}}$	$P_{G_2}(f) = -4(j\pi f)^2 e^{-2(\pi\sigma f)^2}$	$f_0 = \frac{\sqrt{2}}{T_p}$
$p_{G_3}(t) = \frac{3 - \frac{t^3}{\sigma^3}}{\sqrt{2\pi\sigma^5}} e^{-\frac{t^2}{2\sigma^2}}$	$P_{G_3}(f) = -8j(\pi f)^3 e^{-2(\pi\sigma f)^2}$	$f_0 = \frac{\sqrt{3}}{T_p}$
$p_{G_4}(t) = \frac{3 - 3\frac{t^2}{\sigma^2} + \frac{t^4}{\sigma^4}}{\sqrt{2\pi\sigma^5}} e^{-\frac{t^2}{2\sigma^2}}$	$P_{G_4}(f) = 16(\pi f)^4 e^{-2(\pi\sigma f)^2}$	$f_0 = \frac{2}{T_p}$
$p_{G_5}(t) = \frac{15 - 10\frac{t^3}{\sigma^3} + \frac{t^5}{\sigma^5}}{\sqrt{2\pi\sigma^7}} e^{-\frac{t^2}{2\sigma^2}}$	$P_{G_5}(f) = 32j(\pi f)^5 e^{-2(\pi\sigma f)^2}$	$f_0 = \frac{\sqrt{5}}{T_p}$

The higher order derivatives of the Gaussian pulse are presented in Figure 4.



**Fig 4. PSD of the First, Second, Third, Fourth and Fifth Derivatives of the Gaussian Pulse with a Time Duration of 0.5 ns.**

Scholtz's monocycle was proposed by Scholtz and his group in the early 1990s (95), (96), (130). The Scholtz's monocycle is given by (95):

$$p_{Scholtz}(t) = \left[ 1 - 4\pi \left( \frac{t}{\tau} \right)^2 \right] e^{-2\pi \left( \frac{t}{\tau} \right)^2}, \quad (9)$$

where  $\tau$  will adjust the pulse width. Comparing with the second derivative of the Gaussian pulse, Scholtz monocycle has the advantage that  $\tau$  parameter can adjust the pulse width.

Time Domain Corporation was one of the first commercial enterprises to employ Gaussian pulses and their derivatives in practical systems. The UWB pulse waveform proposed by Time Domain Corporation is given by (74):

$$p_{TD}(t) = 6A \sqrt{\frac{e\pi}{3}} \frac{t}{T_p} \exp\left(-6\pi \frac{t}{\tau_p}\right)^2, \quad (10)$$

where  $A$  is the pulse amplitude,  $e$  is Neper's constant and  $\tau_p$  is the pulse duration. The choice of this pulse waveform is given by the fact that antenna behaves approximately as a differentiator. The electromagnetic radiation of the antenna can occur if the transmitted pulse has a zero DC component. If  $\sigma$  is chosen to be small enough, the second derivative of the pulse which is presented as in equation (11) does not present sidelobes of the power density spectrum:

$$p_{TD_2}(t) = \frac{1 - \frac{t^2}{\sigma^2}}{\sigma^2 \sqrt{2\pi}} \exp\left(\frac{t^2}{2\sigma^2}\right). \quad (11)$$

Power spectral measurements based on the Time Domain pulse generator have been presented in (14). Based on a measurement setup according to ITU-R Task Group 1/8, Geneva 2005, the measured PSD level was  $-50.1$  dBm/MHz which is below the FCC mask value of  $-41.3$  dBm/MHz while the  $-10$  dB bandwidth was 3800 MHz.

A further evolution of Gaussian pulses was developed by Aether Wire of the US. The formula of the pulse used by Aether Wire is given by (74):

$$p_{ae}(t) = \frac{1}{\sigma \sqrt{2\pi}} \exp\left(\frac{-(t - \mu)^2}{2\sigma^2}\right) - \frac{1}{\sigma \sqrt{2\pi}} \exp\left(\frac{-((t - \tau_a) - \mu)^2}{2\sigma^2}\right), \quad (12)$$

where  $\tau_a$  is the time separation between the Gaussian pulses within a doublet. The pulse is a Gaussian doublet composed of two Gaussian pulses with variable time separation between them. One drawback of using a time separation is restricting the use in high-speed data communication systems because of the longer total bi-pulse width. The

time separation can be used to generate nulls in the signal spectrum. Therefore, the transmitted spectrum can be shaped by modifying the time separation.

Orthogonal pulse shapers which meet the FCC spectral mask were recently proposed in (77). The orthogonal pulses presented in (77), are obtained by numerically evaluating the discretization of the convolution function between the filter response and its input signal. Converting the digital designs into analogue form uses digital-to-analogue operations at a rate of 64 GHz which is extremely expensive to implement with existing processes. An optimum pulse design methodology, where it was shown that pulse design problem is equivalent to a finite impulse response (FIR) filter was presented in (64). The pulses designed with the algorithm presented in (64) meet the FCC regulations, optimally exploit the allowable bandwidth and power, and are more resistant to narrowband interference than the Gaussian monocycle. The downside of the method is that the 28 GHz clock rate needed for implementation is too high to be implemented with existing digital processes.

In (39), the authors evaluate the level of interference caused by the following radio systems: GSM900, UMTS/WCDMA and GPS on different UWB signals, as well as the performance degradation of UWB-IR systems in the presence of narrowband interference and pulsed jamming. In (39), the authors stated that by decreasing the pulse width or increasing the order of the derivative of the radiated waveform, the UWB spectrum moves to the higher frequencies and eventually out of the range of the interfering frequency, giving a larger jamming margin against GSM interference in both TH-UWB and the DS-UWB systems. The interference experienced by UWB will depend on the proper selection of the UWB pulse waveform and width.

When measured in the presence of an interfering and jamming radio system, the UWB-IR system performance suffers most if the interference and the nominal center frequency of the pulse are overlapping. If the UWB-IR system is low rate and long pulses can be used, lower order derivatives offer better performance (39).

A new monocycle based on the fifth derivative derivative of the Gaussian pulse and which satisfies the FCC spectral limits, has been proposed in (99). In this paper it is stated that in order to maintain a bandwidth as wide as possible, the fifth-order derivative should be used for indoor systems and the seventh order for outdoor systems. A comparison in terms of spectrum characteristics, bit error rate (BER) performance in an AWGN channel and multiple access BER performance in an AWGN channel, between Gaussian pulse, Scholtz's monocycle and Gaussian monocycle has been presented in (23). In this paper, the authors report that Gaussian pulse and rectangle monocycle

have DC components which reduces the antenna efficiency. Scholtz's monocycle and Gaussian monocycle have wider 3 dB bandwidth than sinus and RZ-Manchester pulses. Single link BER performance in AWGN channel shows that performances of Scholtz's and Gaussian monocycle are better than those of Gaussian and rectangle monocycle. In (137), several conclusions about UWB-IR system dependence on Gaussian monocycles are provided. Firstly, higher order monocycles give lower synchronization error variance, pulses generated from a higher order derivative imply higher SNR gain in single user and asynchronous multiple access channel but inferior interference resistance ability. Secondly, pulses with smaller time length imply higher SNR gain in asynchronous multiple access channel conditions, but inferior interference resistance ability.

If additional derivatives of the Gaussian pulse are taken, the relative bandwidth decreases, and the centre frequency increases for a fixed time delay constant  $T_p$  as shown in Figure 4. The higher the order of Gaussian pulse derivatives used, the higher the implementation complexity of the circuits required to implement the pulse shaper. This is because more analogue or digital circuit stages are required to synthesize the pulse shape.

## 2.5 Review of UWB-IR Transmitters

The pulse generator in Figure 1 has the role of transmitting low power pulses starting from a low frequency reference clock generator. The main difference between UWB-IR transmitters and narrowband transmitters is the lack of the up-conversion stage and the digital-to-analogue converter (DAC) used to centre the transmitted pulse at the desired carrier frequency. This leads to a reduced complexity architecture of the UWB-IR transmitters and to a lower power consumption.

A fifth-order derivative Gaussian pulse generator implemented using the AMISemiconductor  $0.5 \mu\text{m}$  CMOS process, has been proposed in (53). The pulse width is 2.4 ns with corresponding bandwidth of approximately 416 MHz and the average power consumption is 1.159 mW with a pulse repetition frequency of 20 MHz. A design of the Scholtz (130) monocycle pulse shape implemented in Taiwan Semiconductor Manufacturing Company (TSMC)  $0.18 \mu\text{m}$  CMOS technology, has been published in (55). In this paper, the authors proposed a quadrant squarer circuit based on a vertical bipolar transistor available using a standard CMOS process, for implementation of the analogue circuit of the approximated Gaussian pulse. The approximated Scholtz monocycle is obtained by differentiating the output current and voltage by using an inductor

and a capacitor, respectively. A pulse generator implemented in TSMC 0.18  $\mu\text{m}$  CMOS process for a closer approximation to the FCC spectral mask has been proposed in (51). The power consumption of the pulse generator presented in (51) is 0.4 mW for a 100 MHz pulse repetition frequency with a 1.8 V power supply level.

An UWB-IR pulse generator design for a 0.35  $\mu\text{m}$  CMOS process for TH-PPM UWB systems was reported in (118). The length of the monocycle is approximately 520 ps while the bandwidth is approximately 1.9 GHz. In this paper, the pulse repetition interval may be determined by the timing circuit presented in (102).

A programmable pulse modulator working in the 3.1 - 5 GHz band with a  $\pi/2$ -shift BPSK modulation scheme, fabricated in 0.18  $\mu\text{m}$  CMOS process has been presented in (44). In this paper, the authors used a four-bit barrel shifter to control a set of variable gain amplifiers which in turn modulate a 4 GHz clock in a cycle-to-cycle fashion with programmed gain values. Due to the large number of components and high toggling rates of the flip-flops, the designed presented in (44) has a power consumption of 105 mW. The power consumption of the pulse modulator reported in (44) is relatively high so would be unsuitable for low power applications.

A single chip impulse radio transmitter with all-digital-controlled pulse generator designed in 0.18  $\mu\text{m}$ , which supports BPSK modulation, has been presented in (71). The power consumption of the UWB-IR transmitter presented in (71) is 29.7 mW from a 2.2 V power supply. A single chip CMOS pulse generator designed for a 0.13  $\mu\text{m}$  process, which supports PPM and BPSK modulations and the third, fourth and fifth order derivatives of the Gaussian pulse, has been presented in (100). The power consumption of the pulse generator presented in (100) is 5 mA from a voltage supply of 1.2 V.

An UWB transmitter using a system-on-package (SOP) 0.35  $\mu\text{m}$  CMOS impulse generator together with an UWB bandpass filter (BPF) and a compact planar UWB antenna have been presented in (60). The output impulse amplitude is 650 mV, and the pulse duration and bandwidth are approximately 2 ns and 500 MHz respectively. The results presented in (60), emphasize the suitability of SOP technology for the miniaturization of UWB-IR transmitters.

An alternative BiCMOS pulse generator based on the idea described in (51) has been published in (138). An integrated pulse generator for both bi-phase and pulse-position modulations (PPM), designed in 0.18  $\mu\text{m}$  SiGe BiCMOS technology was presented in (8). The power consumption of that chip was estimated at 270 mW with a 2.7 V supply. A low power re-programmable pulse generator together with a power saving scheme, designed in TSMC 0.18  $\mu\text{m}$  CMOS technology, for both IR and MBOA UWB systems

have been presented in (66). The main drawback of the pulse generator presented in (66) is the required off-chip RF choke and the need to design a fast clock generator to set the pulse repetition frequency. Also, the value of the delay elements is fixed at the time of designing and is dependent on the load. We believe that a variable delay value is most suitable for the pulse generator because a pulse with adjustable time duration can be generated. A  $0.18\ \mu\text{m}$  SiGe BiCMOS pulse generator which generates a Gaussian monocycle, which consumes only 30 mW with a 1.8 V supply, was reported in (9). A co-design of the impulse generator presented in (9) together with a pulse-position modulator and a butterfly antenna, has been presented in (10). The current consumption of the full UWB-IR transmitter presented in (10) is 14.4 mA at 1.8 V supply.

A carrier based UWB-IR manufactured in a digital  $0.18\ \mu\text{m}$  CMOS process has been presented in (93). In this paper, the authors used a frequency up-conversion technique where a triangular pulse is multiplied with an RF carrier frequency to suppress the signal power below 3.1 GHz to satisfy FCC requirements.

A Gaussian monocycle pulse generator designed in  $0.18\ \mu\text{m}$  CMOS process has been presented in (119). The pulse generator consumes 2.7 mW and the pulse width is approximately 0.6 ns. A digitally controllable bi-phase CMOS UWB-IR pulse generator has been presented in (54). The pulse generator presented in this paper has been designed in AMISemiconductor  $0.5\ \mu\text{m}$  CMOS technology and the total power consumption is 1.88 mW with a 1.8 V supply voltage. The resulting waveform shows substantial ringing while the transmitted pulse repetition frequency is 77 MHz.

A Gaussian monocycle pulse generator designed using a  $0.18\ \mu\text{m}$  CMOS process has been presented in (139). In this paper, the pulse width is 800 ps, the -10 dB bandwidth is 2 GHz, the maximum transmission rate is 50 Mbps, while the power consumption is 7 mA. An interesting concept, where the frequency response of the antenna is used to shape the UWB waveform, which eliminates the need for pulse generator, is proposed in (115).

In Table 2, a comparison of previous presented integrated UWB-IR transmitters is shown.



**Table 2. Comparison of Integrated UWB-IR Transmitters in CMOS and BiCMOS processes.**

Process	Pulse Shape, Width	Consumption [mW]	Reference
0.5 $\mu\text{m}$ AMI CMOS	$5^{\text{th}}$ -derivative @ 2.4 ns	1.159@3.3 V	(53)
0.18 $\mu\text{m}$ TSMC CMOS	Scholtz @ 3 ns	<sup>a</sup> @ 3.3 V	(55)
0.18 $\mu\text{m}$ TSMC CMOS	<sup>b</sup> @ 500 ps	10.4@1.8 V	(138)
0.18 $\mu\text{m}$ BiCMOS	<sup>c</sup>	270@ 2.7 V	(8)
0.18 $\mu\text{m}$ TSMC CMOS	Monocycle	8.47 $\mu\text{W}^{\text{d}}$ @ 1.8 V	(66)
0.18 $\mu\text{m}$ IBM BiCMOS	Monocycle @ 250 ps	30 @ 1.8 V	(10)
0.5 $\mu\text{m}$ AMI CMOS	3rd-order @ 420 ps	1.88 @ 1.8 V	(54)
0.18 $\mu\text{m}$ CMOS	Doublet @ <sup>e</sup>	2.5 @ 2.5 V	(115)
0.18 $\mu\text{m}$ CSM CMOS	Monocycle @ 800 ps	12.6 @ 1.8 V	(139)
0.35 $\mu\text{m}$ AMS CMOS	Monocycle @ 350 ps	20.48 <sup>f</sup> @ 3.3 V	(106)

<sup>a</sup>unknown

<sup>b</sup>unknown

<sup>c</sup>unknown

<sup>d</sup>with power saving schemes

<sup>e</sup>unknown

<sup>f</sup>with 533MHz frequency synthesis circuits included

The most important part of the UWB-IR transmitter is the pulse generator.

Early techniques for the generation of short-pulse RF waveforms utilized the rapid rise or fall times of a baseband pulse to excite a wide-band antenna. A recent overview of short-pulse communications systems and short-pulse radar systems is presented in (32). In this paper, the authors stated that the physical properties of wide-band antennas determined the frequency and bandwidth characteristics of the resulting UWB pulses.

Some of the most commonly used components in discrete UWB-IR transceiver implementation are transistors operated in avalanche mode, tunnel diodes and step recovery diodes (SRD). Transistors operated in avalanche mode were one of the first techniques used as a source of UWB pulses due to their fast rise time (112), (15). In (32), the authors proposed a combination of conventional heterodyne and gated power-amplifier design. Time-gated oscillators are relatively easy to implement, used mostly for transmitter testing and prototyping for testing basic properties of the transmitted spectrum. The conventional heterodyne transmitters make use of a classic up-converter stage. The

gated power-amplifier uses a digitally controllable power-amplifier for controlling the transmitted power spectrum and for reducing the power consumption. Among all discrete components, the fastest transition time of 25 ps is offered by the tunnel diode. SRDs have been used in high voltage, low repetition rates pulse generators (61). More details on semiconductor properties of tunnel diodes and other microwave discrete components can be found in (63).

Recently, time-gated oscillators and low-level impulse sources with time-gated power amplification for prime power minimization techniques have been used for generation of short-pulse waveforms based on discrete implementations (26).

## **2.6 Conclusions**

This Chapter has presented a review of previous work over UWB-IR transmitters and the global UWB standardization efforts.

The UWB standardization activities in Europe and Japan are currently in progress. UK, China and United States are the only countries in the world which allows commercialization of license free UWB systems.

Some pulse shapes suitable for UWB-IR communication systems have been reviewed. The Gaussian monocycle shows good BER performance in AWGN channels, has no DC component, and has a lower implementation complexity. As the order of derivative of the Gaussian pulse increases, the implementation of complexity also increases, since more analogue and digital circuit stages are needed to synthesize the pulse shape. The performance of previously published integrated UWB-IR transmitter architectures have been presented. A large part of previously published transmitters have been integrated in CMOS processes. Discrete implementations of UWB-IR transmitters allows faster evaluation of the UWB-IR communication concepts.

Some of the most commonly used Gaussian waveforms in UWB-IR data communications were presented. The nominal central frequency and the bandwidth of the Gaussian pulses depends on the pulse width. UWB-IR systems have the advantage of being simple and thus, potentially low cost.

### 3 Overview of UWB Receiver Structures

UWB technology has applications in wireless personal area networks (WPAN) providing short-range ad-hoc connectivity among portable consumer communications devices. Since UWB-IR uses extremely short duration transmitted pulses, sub-meter ranging is possible. Therefore, there has been rising interest in vehicular radar systems where UWB-based sensing has the potential to improve the resolution of conventional proximity and motion sensors (7), (98), (133). In UWB-IR, no up/down-conversion is required at the transmitter or receiver side, with the benefit of reducing the cost and size of the devices. Other benefits of UWB include low power transmission and robustness against interference.

This Chapter presents the analysis of one non-coherent UWB-IR receiver and a comparison from both a communication and implementation viewpoint among several non-coherent receiver structures. Coherent receiver structures such as Rake receivers provide very good BER performance at the expense of high computational and hardware complexity (7), (128). For optimal coherent reception, several parameters need to be estimated including multipath delays, channel coefficients for each delayed multipath components and the distortion of the pulse shape. In UWB systems, the number of multipath components is very large, depending on the environment, while the power in each of the multipath components is very low (7), (69). Therefore, the estimation of delays and coefficients of the received multipath components is not a trivial task. Non-coherent receivers do not require channel estimation or received pulse estimation, and exploit the rich multipath channel characteristics of the UWB channel.

Section 3.1 shows the structure of Rake, FM-UWB and auto-correlation receivers and a comparison of coherent and non-coherent receivers from a theoretical viewpoint. Section 3.2 presents the UWB system description. Section 3.3 presents the signal format of the non-coherent energy detection receiver. Section 3.4 presents an overview of UWB-IR receivers ICs. Section 3.5 presents a comparison of TR and EC receivers from an implementation viewpoint. Section 3.6 shows the conclusions of Chapter 3.

## 3.1 Comparison of UWB-IR Receiver Structures

This section provides the insights into the UWB-IR receivers from a communications systems viewpoint. The principles of UWB-IR communication systems have recently been studied in (95), (130), (133), (128). This section reviews the Rake receivers, FM-UWB receivers auto-correlation receivers.

### 3.1.1 Rake Receiver Structures

Rake structures consist of a matched filter that is matched to the transmit waveform that represents one symbol, and a tapped delay line that matches the impulse response of the channel. This structure can be implemented as a number of correlators that are sampled at the delays related to specific MPCs; each of those correlators is called a "Rake finger" (69). Rake receivers are used due to their ability to improve the received signal energy in a multipath fading channel (80). The operation of Rake receivers can be characterized as a type of time diversity. Rake receivers will increase the SNR due to the combination of different signal components. There are generally three types of Rake receivers considered in UWB systems: all-Rake (ARAKE), selective-Rake (SRAKE) and partial-Rake (PRAKE) receivers. Ideally, the ARAKE receiver captures all of the received signal power since the number of fingers equal the numbers of multipath components (129), (126), (125).

The implementation of the ARAKE receiver is not feasible since it requires an infinite, or at least a very large, number of Rake fingers which requires an infinite number of correlators to be implemented. In a modified Saleh-Valenzuela channel model 3, for a BER =  $10^{-3}$ , the non-coherent receivers presents a 6 dB penalty in SNR when compared with SRake receivers with 12 fingers. The performances of the SRAKE receiver in a multipath fading environments has been presented in (129), (127). In (22), the authors present the performances of low-complexity ARAKE, PRAKE and SRAKE receivers to UWB channels. In (22), the authors showed when the number of Rake fingers is 4, the PRAKE and SRAKE have approximately the same diversity order, and differ by only 2dB in a multipath fading environment. This is due to the exponential decay of the average PDP and to the Nakagami distribution with Rayleigh fading for the first arriving signal components. The exponential decay suppresses the multipath components at large delays, while the Nakagami fading leads to smaller variations of the instantaneous amplitudes than the Rayleigh fading. This implies that the strongest

signal components arrive first. Therefore, there is little benefit in increasing the receiver complexity by adding the selection mechanism, because the PRAKE and SRAKE reception are comparable already for a rather small number of fingers (22). Maximum ratio combining (MRC) is a technique which coherently combines all of the signal components to obtain optimal performance (80). MRC requires phase recovery of the received signal and estimating the received power level for each multipath. The distinguishable propagation paths can be separated by the receiver based on the channel estimate. All of the paths that arrive within the receiver's time resolution will be regarded as a single channel path, while the energy of the single path is a combination of the energy of all the undistinguishable paths.

One low complexity UWB-IR solution is FM-UWB (33), (35), (34). FM-UWB approach uses analogue wideband FM to produce an FCC-compliant RF spectrum. The main advantages of FM-UWB are that no local oscillator is required at the receiver while being robust to interference and multipath.

The performance degradation compared with narrow band FM systems is between 10 and 15dB in terms of probability of error performance and depends on the subcarrier modulation index. Due to the squaring action of the demodulator, the dynamic range of the demodulated signals is expanded. Therefore, FM-UWB receivers requires steep sub-carrier filtering. Also, the number of users is limited by multiple-access interference (MAI).

### **3.1.2 Autocorrelation Receivers**

AC receivers utilize the received waveform to perform the correlation, avoiding the need to produce an approximate channel estimate and a replica of the received signal at the receiver (42), (25). AC receivers are advantageous when transmitting through an unknown channel that distorts the transmitted waveforms. The use of noisy templates at the receiver have been studied and some performance losses have been reported (83), (117), (131).

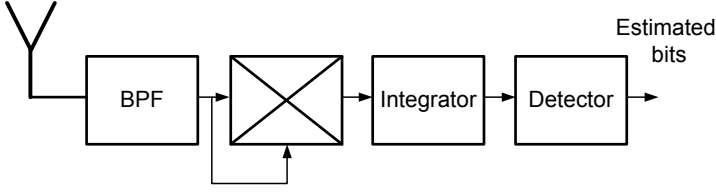
In a TR scheme, two transmitted pulses are used in each frame. The first pulse is not modulated and is called the reference pulse. The second pulse, which is modulated, is separated by a known time delay from the first pulse, and is called the data pulse. The receiver uses pulse-pair correlators to recover the data, thus performing channel estimation and despreading the received signal in one step (42), (36) as shown in Figure 8. Thus, from an implementation viewpoint, the AC receiver does not require a local

oscillator and fast sampling circuits for generating the channel estimator. However, the disadvantage is noise enhancement since the reference pulse, which is correlated with the information pulse, contains noise.

Another receiver type that can be considered as an AC receiver is the energy detector (ED) which have been studied in (85), (82), (120), (94). The ED can be seen as a TR system with zero delay between the reference and the information signal. It can be proven that TR with pulse amplitude modulation (PAM) and ED receivers have equal performance (83). The TR has less noise contribution but only half of the useful received power can be recovered after correlation, while the ED has higher noise contribution but all the useful received energy is recovered (83).

AC and ED receivers are examples of low complexity UWB receiver architectures which do not require a channel estimation section. The delay between reference and data pulses is chosen to be less than the coherence time of the channel so that both pulses are affected similarly by the channel. The reference pulse is used as a template for correlation with the data pulses and for demodulation of the received signal. The main benefit is that there is no need for a local template signal oscillator as in coherent receivers since the TR receiver uses the reference pulses as the template for correlating the data pulses and for demodulation. Therefore, the TR receiver is able to capture the energy from all the multipath components of the received signal with a lower complexity receiver structure when compared with coherent structures. Among the advantages of TR receivers are the relaxed timing requirements and the lack of a classical channel estimation section. In TR receivers, noise has three components: the noise in the template, the noise in the signal and the cross-product noise component. The collected energy will depend on the length of the integration window. With an ideal received pulse template, the integrator will collect the energy from all the multipath components. In practice, for a given channel environment, there is an optimum integration interval which will maximize the collected energy (85).

Another non-coherent receiver structure is the ED scheme. A diagram of an ED receiver is presented in Figure 5.



**Fig 5. Block Diagram for the Energy Collection Receiver.**

Non-coherent modulation schemes such as OOK and PPM are typically employed with ED receiver structures. OOK requires a threshold to be set for taking a decision between a bit '0' or '1'. Finding the optimal threshold is the main drawback of OOK. Since the channel conditions and noise statistics can vary significantly in different environments, an optimum implementation of OOK for non-coherent receivers therefore requires the use of an adaptive threshold. PPM requires the separation between transmitted bits to be higher than the maximum excess delay of the channel, leading to a reduced maximum data rate.

At the output of the integrator shown in Figure 5, the signal is given by (7):

$$y = \int_0^T [\beta s_r(t) + n(t)]^2 dt = \beta \int_0^T s_r^2(t) dt + 2\beta \int_0^T s_r(t)n(t) dt + \beta \int_0^T n(t)^2 dt, \quad (13)$$

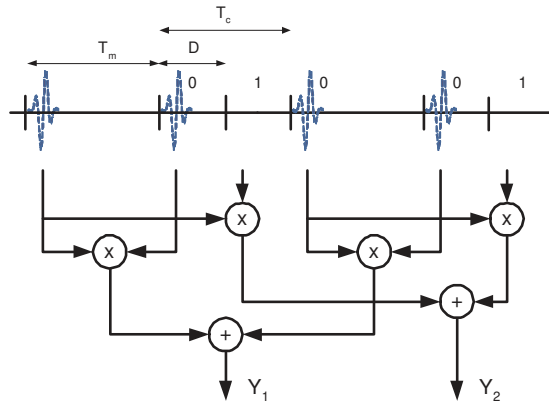
where  $s_r(t)$  is the received signal and  $n(t)$  is the received noise variance. The noise term has two components: the first component is a zero mean Gaussian distributed random variable, while the second component has a chi-square distribution with a variance  $2TB_w \frac{N_0^2}{2}$  (7).

A performance comparison between AC and TR systems for both binary pulse position modulation (BPPM) and binary pulse amplitude modulation (BPAM) has been presented in (83), where it is shown that doublet based structures are not the best solution particularly when the number of pulses per symbol increases. The best structure is the so called "alternate AC" scheme, based on pair-wise combination of pulses for which succeeding pulses form the reference for subsequent pulses (83). This scheme demonstrates robustness to the noise accumulation effects and is able to recover from the signal energy loss typical of doublet based transmitted reference structures(83). The AC receiver slightly outperforms TR based structures, primarily because of the low values of time-bandwidth product, and high values of  $E_b/N_0$ , due to a reduced number of

signal-noise cross terms that defines the decision variable (83). In (135), an energy efficient modulation scheme is proposed where the reference pulse also carries information. In (136), a generalized TR front-end giving better performance than standard TR-UWB scheme was proposed. The receiver front-end proposed in (136) makes use of a joint decision over the received signal to decode each symbol.

Studies presented in (135) and (136), consider the usual transmitted reference structure based on doublets. In (36), the authors present the performance of TR systems in terms of bit error probability (BEP), in both AWGN and multipath environments. In (36), the authors reported a significant impact of non-Gaussian nature of the noise on the BEP, when the effects of inter-frame interference (IFI) and the interference between the reference pulse and the data pulse, have been taken into account.

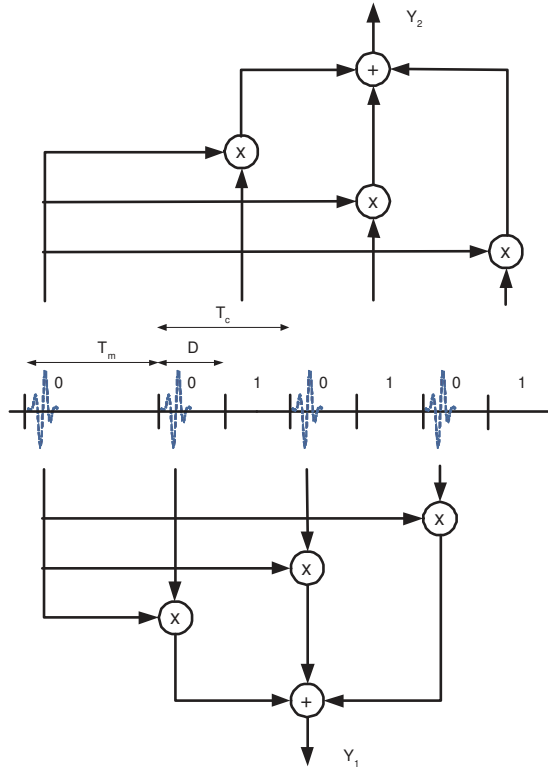
For TR receivers the same reference pulse is used to generate the observation variables  $Y_1, Y_2$  for demodulation, while for AC receivers two different pulses are used. In single reference (SR) schemes, one reference pulse is used together with  $N_p$  data pulses to generate  $(N_p-1)$  correlation values. In doublet based (DB) schemes  $N_p/2$  reference pulses are used with  $N_p/2$  data pulses to generate  $(N_p/2)$  correlation values. The DB-TR structure is presented in Figure 6.



**Fig 6. Block Diagram of the Doublet Based Transmitted Reference Structure.**



The diagram of the SR-TR structure is presented in Figure 7.

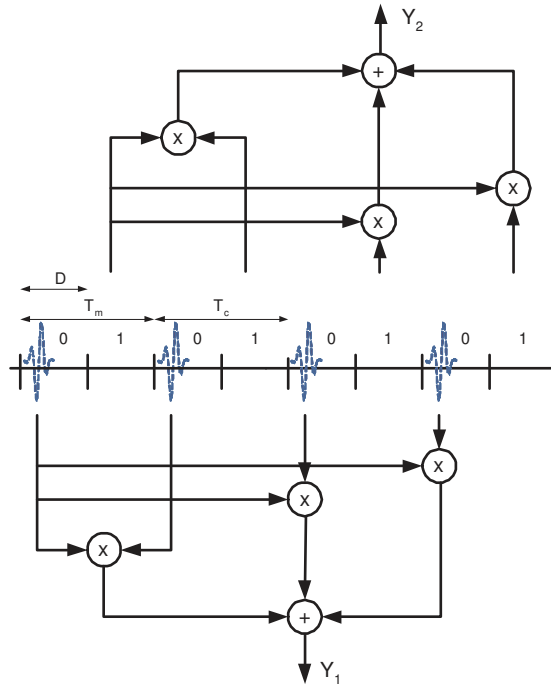


**Fig 7. Block Diagram of the Single Reference Transmitted Reference Structure.**

For AC/TR receivers for both BPPM and BPAM modulations, the transmitted signal is given by (104):

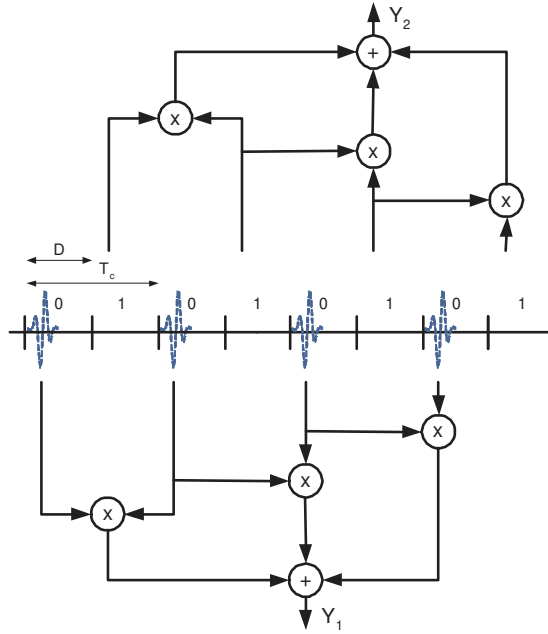
$$s_k^{TR}(t) = \sum_{i=0}^{\frac{N}{2}-1} \left( \sqrt{\frac{E_b}{N_p}} w(t - iT_c - g_{TR}d_kD) + \sqrt{\frac{E_b}{N_p}} a_k w(t - iT_c - T_m - d_kD) \right), \quad (14)$$

where  $w(t)$  is the pulse waveform,  $\int_0^{T_p} w^2(t) = 1$ ,  $N_p$  represents the total number of transmitted pulses,  $d_k \in \{0, 1\}$  and  $a_k \in \{-1, 1\}$  are the symbol alphabets respectively for BPPM and BPAM modulations.  $D \geq T_p + T_g$  is the modulation delay used to distinguish between bit '0' and bit '1', where  $T_p$  denotes the pulse duration. The diagram of the SR-AC structure is presented in Figure 8.



**Fig 8. Block Diagram of the Single Reference Auto-Correlation Structure.**

The diagram of the ALT-AC structure is presented in Figure 9.



**Fig 9. Block Diagram of the Alternate Auto-Correlation Structure.**

For alternate TR/AC (ALT-TR, ALT-AC) receivers and for both BPPM and BPAM modulations, the transmitted signal can be presented as (104):

$$s_k^{ALT}(t) = \sum_{i=0}^{N_p-1} \sqrt{\frac{E_b}{N_p}} a_{k,i} w(t - iT_c - g_{TR} d_k D), \quad (15)$$

where  $a_{k,0} \in \{-1, 1\}$  and  $a_{k,i} = a_{k,i-1}^{i+1}$  for  $i \neq 0$ . For BPPM modulation the values  $a_k = 1$  and  $a_{k,0} = 1$  are used, while for BPAM,  $d_k = 0$  was used.  $T_c$  and  $D$  are set to avoid inter-pulse interference (IPI) and inter-symbol interference (ISI). The symbol energy is equally spread over  $N_p$  pulses composing a symbol. The variable  $g_{TR}$  is used to distinguish between AC receivers, when  $g_{TR} = 0$  and TR receivers when  $g_{TR} = 1$ .

Due the large bandwidth and to the long delay spread of the channel, the output of the correlator can be considered as Gaussian. The bit error probability (BER) can be then expressed using the  $Q(\cdot)$  function using then the SNR values derived in (83). For

the AC/TR receiver with BPPM modulation the BER is given by (104):

$$BER_{DB-BPPM} = Q \left( \sqrt{\frac{\frac{2E_b}{N_0}}{\left(4 + 2g_{TR} + 2N_p 2TW \frac{N_0}{E_b}\right)}} \right). \quad (16)$$

For the AC/TR receiver with BPAM modulation the BER is given by (104):

$$BER_{DB-BPAM} = Q \left( \sqrt{\frac{\frac{2E_b}{N_0}}{\left(4 + N_p 2TW \frac{N_0}{E_b}\right)}} \right). \quad (17)$$

Comparing equations (16) and (17), the conclusion is that the performance of the AC/TR receiver with BPPM is lower than BPAM due to the double number of pulses used to transmit the information signal. For the ALT-TR receiver with BPAM modulation, the BER is given by (104):

$$BER_{ALT-BPAM} = Q \left( \sqrt{\frac{\frac{N_p-1}{N_p} \frac{2E_b}{N_0}}{4 \frac{N_p}{N_p-1} - \frac{6}{N_p-1} + N_p 2TW \frac{N_0}{E_b}}} \right). \quad (18)$$

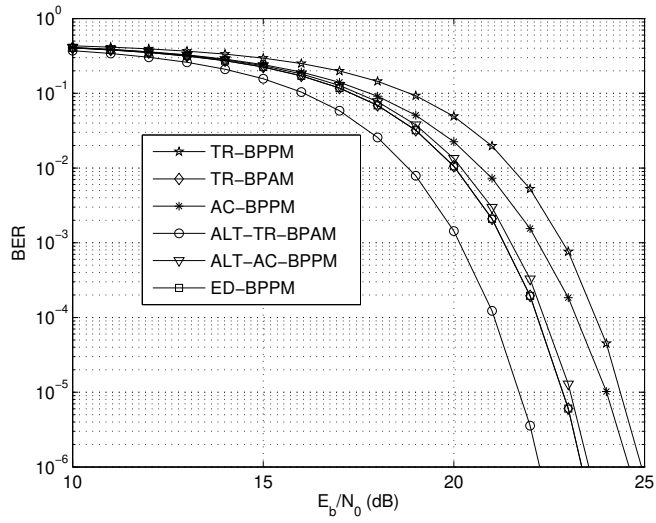
For the ALT-AC receiver with BPPM modulation, the SNR can be presented as (104):

$$BER_{ALT-BPPM} = Q \left( \sqrt{\frac{\frac{N_p-1}{N_p} \frac{2E_b}{N_0}}{4 \frac{N_p}{N_p-1} - \frac{6}{N_p-1} + N_p 2TW \frac{N_0}{E_b}}} \right). \quad (19)$$

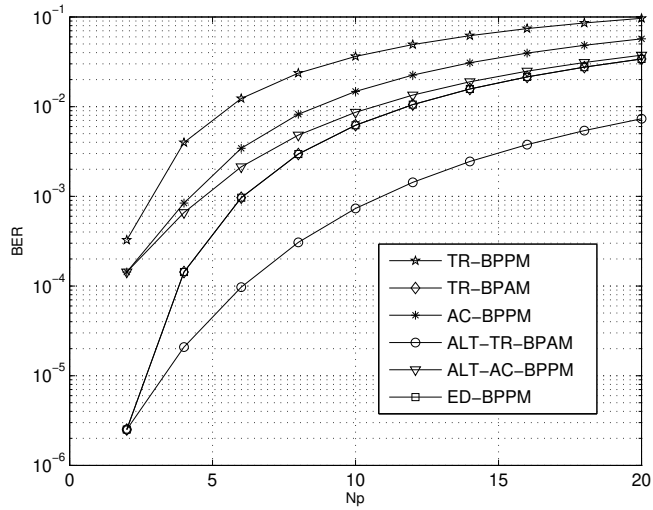
Comparing equations (18) and (19), the conclusion is that the performance of the ALT-TR receiver with BPAM is worse than BPPM due to the double value of the time bandwidth product at the denominator of equation (19).

In order to understand the behaviour of the different receiver structures, the BER plotted versus  $E_b/N_0$  is presented in Figure 10. The performance of TR-BPAM system is similar to that of ED with binary pulse position modulation (ED-BPPM) system. This is because while the ED has higher noise contribution due to squaring operation, all the useful received energy is recovered, the TR has less noise contribution but only half of the useful received power can be recovered after correlation. Therefore, the performance curves of TR-BPAM and ED-BPPM in Figure 10 overlap. In Figure 11, the dependence of BER and number of pulses  $N_p$  is presented. The ALT-AC structure can be seen to provide the best performance because it is able to compensate the signal energy degradation and to reduce the noise accumulation that is typical in single reference

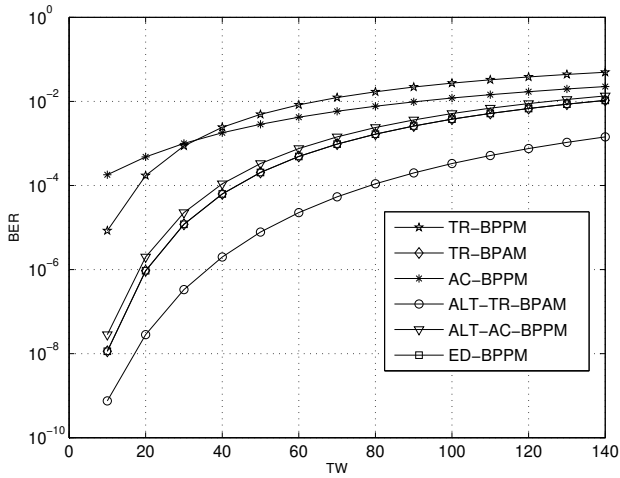
structures. The performance of the other systems decreases when the number of pulses increases. Increasing the number of pulses in single reference schemes will increase the variance of the signal-noise cross terms produced by the noise present in the single reference. The ED-BPPM structure is heavily influenced by the pulse repetition structure due to the squaring operation. The TR-BPAM structures performance is heavily influenced by the pulse repetition structure because one single reference pulse is used for all the data pulses. ED-BPPM and TR-BPAM structures presents same BER versus number of pulses performance. This is because the ED-BPPM saves 3dB of energy power comparing with the TR-BPAM structure since a reference pulse is not transmitted while noise variance increases when compared with the TR-BPAM scheme due to the squaring of the noise. In Figure 12, BER performance is presented versus time bandwidth product  $TW$ . For low value of time bandwidth product and low values of  $E_b/N_0$ , the performance of doublet structures is close to that of single reference structures since the integration time of the noise is lower. When the delay spread of the channel increases requiring a longer integration time, the performance of the doublet structures degrades due to the higher integration time of the noise. The AC receiver slightly outperforms TR based structures, mostly because of the low values of time bandwidth product, and high values of  $E_b/N_0$ , due to a reduced number of signal-noise cross terms that defines the decision variable. For low values of  $N_p$  and  $TW$  and high values of  $E_b/N_0$ , the AC systems slightly outperform the TR systems due to the reduced number of signal-noise cross terms that defines the decision variable. ED-BPPM and TR-BPAM structures shows identical performance, therefore their performance curves overlap.



**Fig 10. Simulated bit error rates as a function of bit energy per noise power ratio for different non-coherent receivers in AWGN channel with the number of pulses  $N_p = 12$  and the time-bandwidth product  $TW = 140$ .**



**Fig 11. Simulated bit error rates as a function of number of pulses for different non-coherent receivers in AWGN channel when the time-bandwidth product  $TW = 140$  and bit energy per noise power ratio  $E_b/N_0 = 20\text{dB}$ .**



**Fig 12. Simulated bit error rates performance as a function of time-bandwidth product for different non-coherent receivers in AWGN channel when the number of pulses  $N_p = 12$  and bit energy per noise power ratio  $E_b/N_0 = 20\text{dB}$ .**

In Table 3, the theoretical performance versus implementation challenges of several UWB-IR receiver structures are presented.

**Table 3. Theoretical performance vs. Implementation Challenges for UWB-IR Receiver Structures.**

Receiver	Implementation challenge	Author
All-Rake	Infinite number of fingers	(129)
Partial-Rake	Channel estimation	(129), (22)
Selective-Rake	Channel estimation	(129), (22)
Autocorrelation	Finite number of fingers, channel estimation	(42), (135)
Non-coherent	Finite number of fingers, no channel estimation	(85), (106)
FM-UWB	Steep sub-carrier filtering	(33), (35), (34)

## 3.2 UWB System Description

With improvements in power consumption, device size, communication and medium access control (MAC) algorithms, sensor networks are becoming more popular for an ever increasing range of applications. Due to the bursty nature of the traffic in sensor networks, the device may remain idle for long periods of time, then sending significant amounts of information when an event occurs. Low duty cycle operation of sensor network devices requires design of efficient medium access protocols, low power consumption RF and baseband circuits, and inexpensive receiver architectures in terms of computing power. UWB-IR systems have a number of inherent properties that are well suited to sensor networks scenarios. Impulse based UWB systems have low cost and low complexity devices, have noise like signals, and have good time domain resolution, enabling for location and tracking applications.

To realize the benefits of using UWB-IR technology in sensor networks, this thesis has explored inexpensive devices and low complexity receiver architectures. The UWB system is based on low-power, low-complexity UWB transceivers. The UWB transceiver circuit is designed for low-data-rate, low-cost applications with built-in location and tracking capabilities.

In order to minimize the complexity of the UWB devices, the location information can be obtained by fixed nodes (FN) which will send the information to a central system. The FN can detect and exchange information to determine the position of the UWB devices based on the time of arrival of the UWB signals coming from the UWB devices. The UWB-IR based sensor network operates in a Master-Slave configuration where the UWB devices receive a limited set of commands from the FN and send back the requested information. The UWB devices are identified based on their unique identifiers. The fixed nodes communicate with each other to exchange information about the perceived position of each sensor in the network (75). The computational task needed for positioning are left to the central system. The MAC solution must be low complexity and interference free when performing positioning measurements, which leads to the choice of TDMA. Making use of a TDMA architecture for timing maximizes the sleep time of nodes and minimizes the amount of control traffic needed (75).

The system also uses Time Division Duplexing (TDD) which separates the "talk" time frame, where the UWB devices can send information to the FN, and the "listen" time frame where the UWB devices receive commands and information from the BS. The principle diagram of the MAC frame is presented in Figure 13.



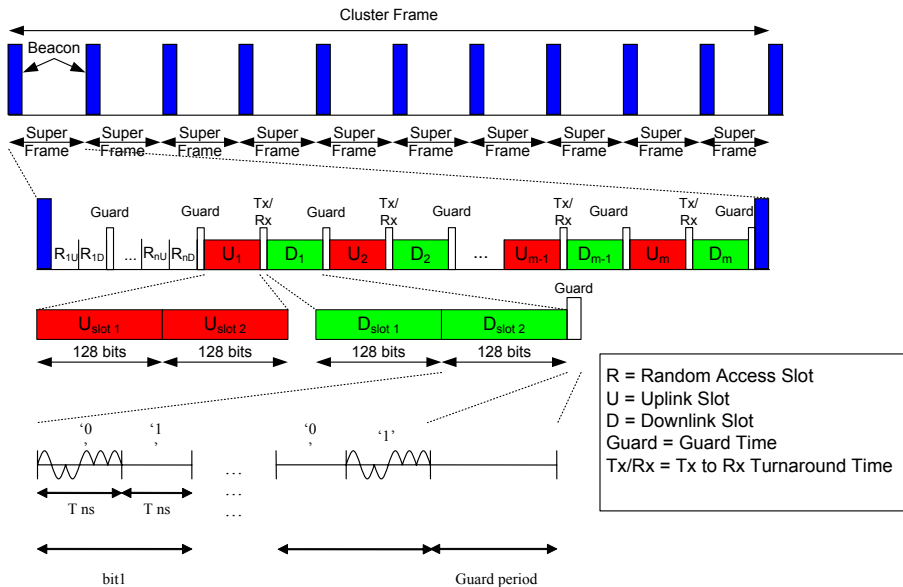


Fig 13. Diagram of the MAC Frame.

Each of the "listen" and "talk" time frames are introduced by a beacon that carries information both on the presence and structure of the network. The frame duration is divided in time slot units, and each UWB device has a number of consecutive slots assigned to compose a message. The TDMA network has an aggregate data rate of 5 Mbps which may be divided amongst hundreds or thousands of devices if a per device data rate of several kbit/s is considered.

### 3.3 UWB Signal Format

The UWB signal used for the system considered in this thesis is based on a train of short pulses multiplied by a spreading sequence using the direct sequence (DS) approach. The bit interval is divided into  $M = 2$  time slots (binary modulation). Each time slot defines a possible transmitted symbol. We are using 64 pulses for bit '0'. As the detection procedure is based on energy collection, the separation of different users can only be done in the time domain.

The transmitted signal for the user of interest is given by:

$$s(t) = \sum_{k=-\infty}^{\infty} \sum_{j=1}^N (c_p)_j w_{TR}(t - kT_d - jT_c - \delta d_k), \quad (20)$$

where  $w_{TR}$  is the transmitted pulse with pulse width  $T_p$ ,  $T_d$  is the symbol interval,  $\delta = 120\text{ns}$  is the delay used to distinguish different transmit symbols  $d_k \in [0, 1]$ ,  $T_c = NT_p$  with  $N \in I$  is the chip interval, and  $(c_p)_j$  is the  $j$ -th chip of the pseudo-random (PR) code.

The received signal after the receiver antenna is given by:

$$s_r(t) = \sum_{l=0}^L A_l \sum_{k=-\infty}^{\infty} \sum_{j=1}^N (c_p)_j w_{RX}(t - kT_d - jT_c - \delta d_k - \tau_l) + n(t),$$

where  $w_{RX}$  is the first derivative of the transmitted waveform  $w_{TR}(t)$ ,  $L$  is the number of resolvable paths,  $A_l$  defines the gain for path  $l$  and  $n(t)$  is zero mean additive Gaussian noise. The pseudo random (PR) code is bipolar with values  $\{-1, +1\}$ . The data rate  $R$  is defined by:

$$R = \frac{1}{T_d} = \frac{1}{2\delta}. \quad (21)$$

The non-coherent energy collection receiver detects the signal energy over a time window that is determined by the delay spread of the channel. During the energy collection process, noise is also integrated changing the receiver SNR. Thus, a large delay spread of the channel which imposes a larger integration window decreases the performance of non-coherent receivers. The capacity of the energy collection receiver to collect almost all the signal energy compensates for the drawback due to noise enhancement characteristics (85), (106). There is no correlation in the receiver and so, the modulation must be orthogonal in the time domain. The UWB transceiver architecture for the UWB tags is based on a non-coherent structure utilizing binary position modulation (BPM) and simply collects the signal energy in different time windows and determines the transmitted bit based on the detected maximum energy.

### 3.4 Overview of Integrated Circuits UWB-IR Receivers

This section presents the performance of full UWB-IR receivers and LNAs, implemented in different IC technologies. We have chosen to present the performance of the LNA because it is the first amplifier of the receiver front-end, after the antenna, and has a strong impact over the performance factors of the receiver.

The architecture of an integrated Rake UWB-IR receiver intended for low-rate, indoor wireless systems, operating below 960 MHz, was presented in (72). In this paper, implementation issues of the system, including clock generation, conversion bit-width, gain, noise, and the choice of pulse rate versus pulse amplitude were discussed in relation to their impact on both performance and circuit design constraints. However, in (72) the authors do not present the power consumption of the integrated UWB-IR receiver. In (73), a low power, DC - 1 GHz UWB-IR front-end was presented. The power consumption of this transceiver is approximately 1 mW at 1.1 V supply voltage while using signal sampling at a rate of 1.92 Gsamples/s. In (116), a CMOS UWB-IR transceiver for 1 Mbps was presented. The power consumption of this transceiver is 1 mW while using a 1.8 V supply voltage, because the duty cycle of this transceiver is only 0.007%.

A wireless link was demonstrated at a data rate of 193 Kbps based on a 0.18  $\mu\text{m}$  CMOS digital baseband processor using up to 300 MHz pulsed UWB signals (20). The total power consumption of the baseband processor reported in (20) was 275 mW. In (116), the authors report a 0.18  $\mu\text{m}$  CMOS UWB-IR transceiver for 1 Mbps data communications. The range for data communication used was 1 m with a BER of  $10^{-3}$ . In (44), the authors have presented an 0.18  $\mu\text{m}$  CMOS, direct-sequence, spread spectrum (DSSS) UWB integrated transceiver, working in 3.1 - 5 GHz band. The modulation employed is  $\pi/2$  shift BPSK. The receiver's LNA has a gain of 16 dB in the 3.5 - 4.5 GHz band, has a noise figure of 4 dB, an IIP3 = -4.5 dBm while the current consumption is 4 mA. The receiver makes use of a 8 GHz VCO which is divided by 2 for the  $I$  and  $Q$  receiver branches while the ADC speed is 1 Gsamples/s, which significantly increases implementation complexity when compared with non-coherent receiver structures. The power consumption of the receiver reported in (44) is 280 mW using a 1.8 V supply.

In (140), a BPSK IR receiver is presented. The hardware design uses a 0.18  $\mu\text{m}$  process and data rates up to 200 Mbps are reported over the inter-chip channel length of 20 cm. The power consumption of the receiver reported in (140) is 99 mW using a 1.8 V supply.

In (76), the analysis of an UWB SiGe LNA is performed examining noise, linearity and minimum group delay variation. The implemented LNA achieves a gain of 13 dB, a minimum noise figure of 3.3 dB and an IP3 = -7.5 dBm between 2 - 10 GHz while consuming 9.6 mW with a 2.4 V supply.

A 3 - 10 GHz LNA with wideband LC-ladder matching network was presented in (45). In this paper, the reported power consumption of the LNA is 30 mW and the

reported noise figure is 2.5 dB. An UWB CMOS LNA for 3.1 - 10.6 GHz wireless receivers was reported in (18). The power consumption of the LNA reported in this paper is 9 mW and the reported minimum noise figure is 4 dB.

A 0.13  $\mu\text{m}$  CMOS LNA including a 3<sup>rd</sup> order Chebyshev bandpass matching network based on the power constrained noise optimization technique (PCSNIM) (62) concept was presented in (123). The LNA presented in this paper has a  $-3$  dB bandwidth of 7.7 GHz with an input return loss better than  $-10$  dB and output return loss better than  $-15$  dB over the entire bandwidth. Another systematic approach of a 3 - 5 GHz UWB CMOS LNA together with two output impedance matching methods was presented in (58). In this paper, both  $S_{11}$  and  $S_{22}$  parameters are below  $-10$  dB, the overall gain was 13.5 dB and the noise figure was below 2 dB. Another UWB digital receiver, based on the frequency-domain approach, was presented in (59). This architecture requires a large number of LNAs and filter-banks which translates into increased power consumption. However, in both (8) and (9), only the pulse generators have been integrated. It is reasonable to assume that when all the other modules required for a full transceiver are included, the power consumption of both architectures will increase significantly. The receiver is correlation-based, and the integrated solution for the correlator, LNA, and filter required is given in 0.18  $\mu\text{m}$  CMOS technology. A 900 MHz UWB baseband front-end designed in 0.18  $\mu\text{m}$  CMOS was presented in (57). The total power consumption of the front-end reported in (57) was 71 mW. The total power consumption of the UWB transceiver reported in (20) and (57) was 346 mW. With the exception of (20), the synchronization and detection modules are not reported in these papers. In (121), the authors report an interesting investigation regarding power consumption of both analogue and digital UWB-IR receivers in the 3.1 - 5 GHz band, targeting data rates up to 10 Mbps. Contrary to previous opinions regarding the use of fully digital UWB-IR receivers, the authors in (121) demonstrate that, in terms of power consumption per bit, the partially analogue UWB-IR receiver outperforms the fully digital UWB-IR receiver by a factor of 7.

### **3.5 Comparison of Autocorrelation Receivers From An Implementation Complexity Viewpoint**

The main difference between ED and TR receivers is that while the ED receiver uses only one reference signal for correlation and a bank of integrators for energy collection,

the TR requires several analogue delay lines between the reference and information bearing signal as shown in Figure 7. The ED receiver does not require a delayed version of the transmit signal to perform the correlation. Using only one transmitted signal instead of a doublet obviously makes the pulse generation process less complex to implement, since generation of different waveforms requires additional circuitry.

For an ED receiver, from the implementation viewpoint, the analogue delay line is substituted with a mixer implementing the square function. The square function can be implemented with already available analogue circuit topologies, while the analogue delay line with a long delay line, requires a lot more components which increases the occupied die area of the circuit. The delay between the reference and information bearing signal will typically be implemented using an analogue delay line.

From an implementation point of view, the design of an analogue delay line with a delay of the order of a few tens of nanoseconds, with a very wide bandwidth is very challenging (11). This is due to the fact that the delay value of one simple filter stage is of the order of tens to hundreds of picoseconds, while the insertion loss is a few dB. An analogue delay line with few delay stages will heavily attenuate the received signal. This requires a high gain, a low noise amplifier to compensate for the insertion loss of the analogue delay line.

Therefore, TR receivers collect more noise than an ideal matched filter. The integration process can be optimized if the position of the multipath components are known. In this case, the integrators will collect the received components only from the known multipath positions.

The analogue delay line can be implemented by using the group delay  $t_g$  properties of the bandpass filters. The bandpass filter filters the signal within the bandwidth of interest and will delay the input signal with a value equal with its own group delay  $t_g$ . Since the received signal must be delayed with same value, the filter has to be designed with linear phase. Due to the wideband nature of the signals used, the bandpass filter must have a wide bandwidth in the order of few gigahertz. The design of an analogue delay line must balance the complexity of implementation and high bandwidth since  $t_g$  increases with the order of the filter (therefore a higher implementation complexity). In order to achieve large values of delay with minimum implementation complexity, the analogue delay line must use low order and low bandwidth bandpass filters instead of higher order and higher bandwidth filters. In order to avoid IPI and ISI, the delay of the delay line has to be long (of the order of tens of ns), which increases the number of stages and therefore increases the implementation complexity.

The ED receiver does not require an analogue delay line for doublet generation further reducing the implementation complexity compared with TR receivers. As seen in Figure 10, the performance loss of the ED structure is less than 3 dB when compared with the TR-BPPM structure and shows the same performance as the TR-BPAM receivers.

Based on the BER comparison between different receiver structures as presented in Figure 10, and on the implementation complexity comparison, the conclusion is that UWB-IR ED receiver offers reasonable performance in multipath channels for reduced implementation complexity and lower power consumption.

### 3.6 Conclusions

This Chapter has presented a comparison between UWB-IR coherent and non-coherent receiver architectures from both a theoretical and implementation viewpoint. UWB-IR Rake receivers show excellent BER performance while their implementation complexity is extremely high, mainly due to their requirement for channel estimation section. In a modified Saleh-Valenzuela channel model 3, for a BER =  $10^{-3}$ , the non-coherent receivers presents a 6 dB penalty in SNR when compared with SRake receivers with 12 fingers. However, non-coherent receivers offer a much lower implementation complexity than 12 fingers SRake receivers. We have presented the BER performance versus  $E_b/N_0$  for TR and AC receivers in AWGN channel, showing that the energy detection receivers offer the same performance as the TR-BPAM receivers and less than 3dB degradation when compared with the TR-BPPM receivers. The performance of TR-BPAM system is the same as that of the ED-BPPM system because the TR has less noise contribution but only half of the useful received signal energy can be recovered after correlation. On the other hand, the ED has higher noise contribution but all the useful received energy is recovered.

The alternate receiver structure gives the best performance among all systems compared since it reduces the noise accumulation specific to the single reference structures and is able to recover from the undesirable signal energy loss typical with TR receivers. The BER performance versus number of pulses of different non-coherent receiver structures has also been presented. The ALT-AC structure provides the best performance since, due to its signaling, is able to compensate the signal energy degradation and to reduce the noise accumulation. The performance of the other non-coherent receiver structures decreases when the number of pulses increases because more noise will be in-

tegrated by the receiver. The ED-BPPM and TR-BPAM structures demonstrate similar BER performance as the number of pulses varies.

BER performance versus time bandwidth product  $TW$  has also been presented. Again, the TR-BPAM and ED-BPPM structures show identical performance because the ED-BPPM scheme integrates more of the signal energy, the noise being higher than the TR-BPAM noise due to squaring operation. On the other hand, the TR-BPAM scheme integrates half of the signal energy due to the reference pulse. The bit error rate simulations of the UWB-IR non-coherent receiver architectures presented in Figures 10, 11 and 12 were validated by a Matlab<sup>TM</sup> simulator.

It was shown that the implementation complexity of the UWB-IR non-coherent receivers is greatly reduced compared with Rake receivers. This is because non-coherent receivers do not use the channel estimation section required by the Rake receivers. The drawback of the non-coherent approach is noise enhancement due to the squaring and the degradation in time resolution, which is proportional with the length of the integration time window. Currently, the robustness of non-coherent UWB-IR receivers against narrow-band and wide-band interferers is still a subject of active research. Among the analyzed non-coherent receiver structures, the non-coherent energy detection receiver has the lowest implementation complexity. This is because energy detection receivers do not use analogue delay lines which greatly decreases the implementation complexity of the front-end section of the receiver.





## 4 Proposed UWB-IR Transmitter Architecture

This Chapter presents the design of an UWB-IR Gaussian monocycle transmitter. As explained in Chapter 2, as the order of derivatives of the Gaussian pulse increases, the spectral utilization efficiency increases, too. The UWB-IR transmitter presented in this Chapter can be modified to produce any derivative of the Gaussian monocycle due to its capability of generating the positive and negative Gaussian pulses, as shown in Figure 20. Therefore, a UWB-IR transmitter which is able to transmit multiple pulse shapes, can be designed with only minor modifications of the presented architecture.

The UWB-IR transmitter implemented has a low die area of only  $400\mu\text{m}$  by  $400\mu\text{m}$ , contains no inductors and has the advantage that it can be integrated in digital CMOS processes which are relatively more advanced than analogue CMOS processes. The Gaussian monocycle shape has been chosen primarily because it is easy to implement with readily designed circuit topologies in inexpensive CMOS processes, has a zero-DC component and has a high central frequency and a wide -10 dB bandwidth.

The structure of this Chapter is as follows: in Section 4.1, we present the motivation and the general overview of the proposed UWB-IR transmitter architecture. In Section 4.2, the approximation of the Gaussian monocycle and the implementation details of the pulse shaper are presented. In Section 4.3, the implementation details of the RF clock generation process are shown. In Section 4.4, we present the measured and simulated results of the UWB-IR transmitter. In Section 4.5, we present the conclusions of this Chapter.

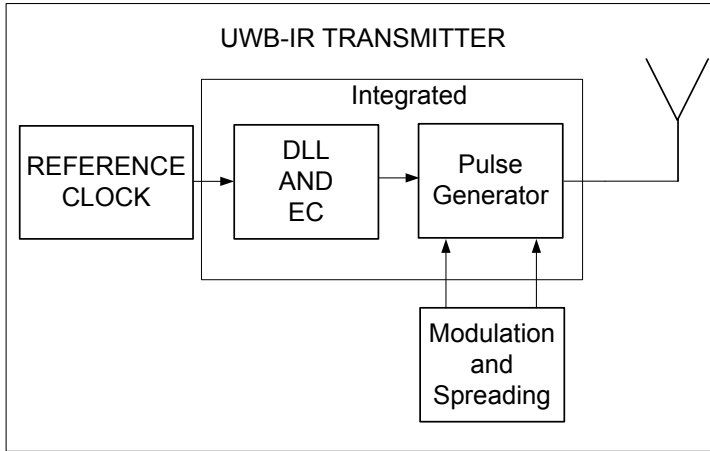
### 4.1 Introduction

The choice of the pulse shape in UWB-IR systems depends on the design objectives including good approximation of the generated pulse with theoretical pulse shape, efficient spectral utilization, low implementation complexity, zero-DC component, high central frequency and large -10 dB bandwidth. In (23), the authors show that the single link and multi-access BER performance of the Gaussian and Scholtz monocycle is better than that obtained using the Gaussian pulse. Therefore we have selected the Gaussian monocycle for implementation. We have chosen to design and implement a Gaussian monocycle generator since its easy to implement in inexpensive CMOS pro-

cesses, has a zero-DC component which does not decrease the antenna efficiency, is suitable for low data rate sensor networks, and has a  $-10$  dB bandwidth in the order of 3 - 4 GHz.

The UWB-IR transmitter presented in this chapter, generates a pulse shape which is a good approximation of the Gaussian monocycle waveform. The approximation is based on the transient response of a first order network to a step-like input function. The system design takes into consideration the implementation complexity and adheres to the FCC spectral mask limits. The UWB-IR transmitter utilizes readily available circuit topologies such as DLL, digital edge combiner, NAND gates and differential pairs. A zero-DC waveform will not decrease antenna efficiency, improving the receiver's SNR.

The block diagram of the UWB-IR transmitter we propose is presented in Figure 14 (107). The UWB-IR transmitter is based on three main sections: a reference clock signal; a clock multiplier (DLL and EC) which sets the pulse repetition frequency; and the pulse generator which fixes the pulse shape, the pulse spectrum and the pulse width. The reference clock signal is a low frequency signal produced by a quartz oscillator. The clock multiplication section fixes the pulse repetition frequency and was implemented in order to increase the transmitted signal amplitude up to the maximum emission level allowed by the FCC spectral masks. The clock multiplication section can be implemented based on a frequency synthesis approach or a DLL and edge combiner (65). Traditionally, the frequency synthesizers are implemented with PLLs and frequency dividers (88). PLL systems are inherently unstable, they need high die area to accommodate large inductors and are noisier due to the voltage controlled oscillators (VCO) (88). Therefore, we have designed a DLL based on a clock multiplication process since the DLL has the advantage of being simple to implement, has a better noise figure, needs less die area since inductors are not integrated on-chip, and is inherently stable. More details about the clock multiplication section are presented in section 4.3.



**Fig 14. UWB IR Transmitter.**

The die photo of the UWB-IR transmitter is shown in Figure 66. Only the CMOS modules of the process have been used for the transmitter. The pulse generator section has the task of generating the pulse waveform which feeds the antenna. UWB scrambling codes whiten the spectrum as much as possible to minimize the power spectral density and hence the potential interference to other systems. Gaussian monocycles have a wide  $-10$  dB bandwidth which is highly desirable. The bandwidth requirement of the transmitted waveform is mainly determined by the need to fill as much as possible of the spectrum available within the FCC mask. This enables the transmission of the maximum allowable transmitted power. The pulse amplitude has to be adjustable due to the need to modify the transmitted power. The pulse width will affect the transmitted bandwidth and central frequency.

The pulse generator contains two sections: a delay stage and a pulse shaping stage. The delay stage has the role of fixing a delay for the pulse shaper. The delay can be fixed by using a DLL or a string of inverters. We choose to use a string of inverters due to its simplicity, lower power consumption and lower die area. The pulse shaper produces a Gaussian monocycle whose pulse width can be controlled through the bias current of the pulse shaper.

### **4.1.1 UWB-IR IC Transmitter Test Board**

The integrated UWB-IR transmitter has been manufactured without packaging and therefore has to be manually glued and bonded to a test board. The testbed presented in Figure 65 shows the UWB-IR IC mounted on a printed circuit boards (PCB) together with the current sources, SMA connectors and the RF balun at the transmitter output and receiver inputs. Due to bonding to the test board, the parasitic of the traces between the transmitter's output pins and SMA connector will increase the pulse width to approximately 700 ps. For spectrum measurements, the Agilent-PSA-E4446A<sup>TM</sup> spectrum analyzer have been used. The Agilent-PSA-E4446A<sup>TM</sup> has a frequency range up to 50 GHz.

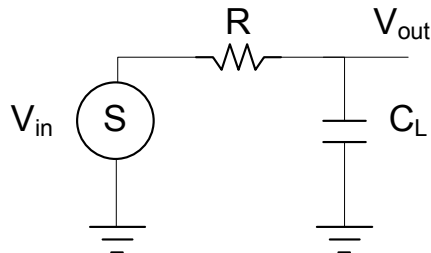
## **4.2 Pulse Generator**

The Gaussian monocycle is relatively easy to generate with readily designed circuit topologies, is inexpensive to implement using CMOS processes, has a zero-DC component which does not decrease the antenna efficiency and has a  $-10$  dB bandwidth of 3 - 4 GHz. Since the pulse amplitude at the output of the pulse shaper section is quite low (tens of millivolts), a multi-pulse approach has been taken to design the UWB-IR pulse generator. The power supplies of future CMOS processes will go lower than a few hundred millivolts and hence a high amplitude pulse will not be possible. The multi-pulse transmitter is a practical way of increasing the total transmitted energy. The UWB-IR pulse generator is built based on two main sections: the delay stages section and the differential output section. Both delay stages and differential output sections are implemented in a  $0.35 \mu\text{m}$  CMOS process.

### **4.2.1 Approximation of the Gaussian Monocycle**

In this section we present one method of approximation of the Gaussian monocycle by using readily available circuit topologies. The Gaussian monocycle approximation is composed of two Gaussian pulses which are subtracted from each other by a cross-coupled differential pair. The generation of the Gaussian pulse is based on NAND gates triggered by precisely delayed digital signals. The digital signals are generated by a DLL based frequency synthesizer and delayed by a string of inverters. Then the delayed digital signals triggers two NAND gates. The propagation of the digital input

signals through the NAND gate is similar with analysis of a first-order linear RC network excited by a step function, with  $V_{in}$  going from 0 to  $V$ . In Figure 15 we present the first order network excited by a step like function.



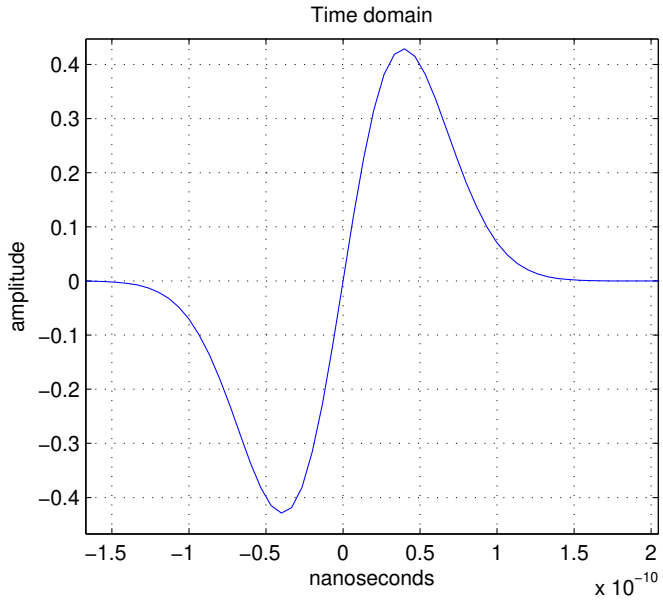
**Fig 15. First Order Network.**

The transient response of this circuit is known to be an exponential function, and is given by (81):

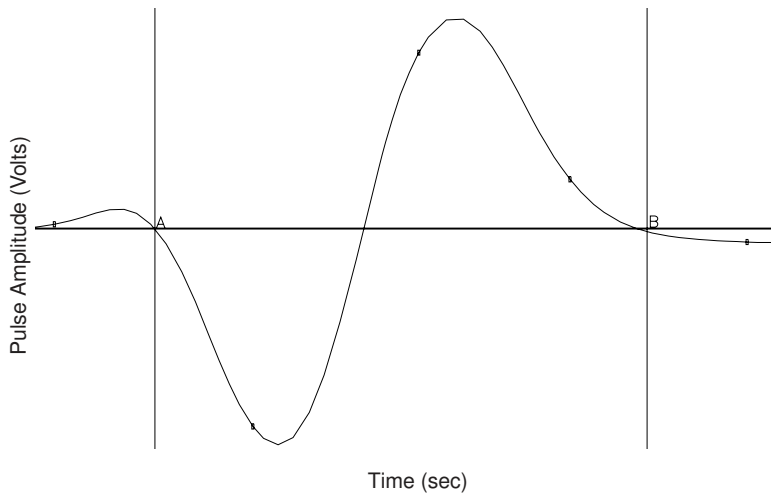
$$V_{out}(t) = (1 - e^{-\frac{t}{\tau}})V_{in}, \quad (22)$$

where  $\tau = RC_L$  is the time constant of the network. In order to obtain the same values for the monocycle's positive and negative transitions, it is desirable to have identical propagation delays for both NAND gates for both rising and falling input signal. This condition can be achieved by making the "ON" resistance of the NMOS and PMOS approximately equal by designing the PMOS transistor with double the width of the NMOS transistor. The Gaussian monocycle width can be made smaller by following design rules of digital design. The capacitance of critical nodes must be minimized, and the currents available for charging or discharging the nodes during the transients voltage changes should be maximized. The inverters which fix the delay of the Gaussian monocycle have been designed to minimum size and so to limit the parasitic capacitances.

In Figure 16 and 17, we present a comparison between the theoretical Gaussian monocycle and the measured pulse at the output of the transmitter. The measured Gaussian monocycle exhibits ringing effects due to the noise from the supply and ground lines (67).



**Fig 16. Theoretical Plot of Gaussian Monocycle with a time duration of 3ns.**



A: (7.421 ns -86.51u) delta: (339.21 ps -5.31u)    B: (7.760 ns -91.82u) slope: -15.66K

**Fig 17. Measured Monocycle from Implemented UWB-IR Transmitter with a time duration of 339 ps.**

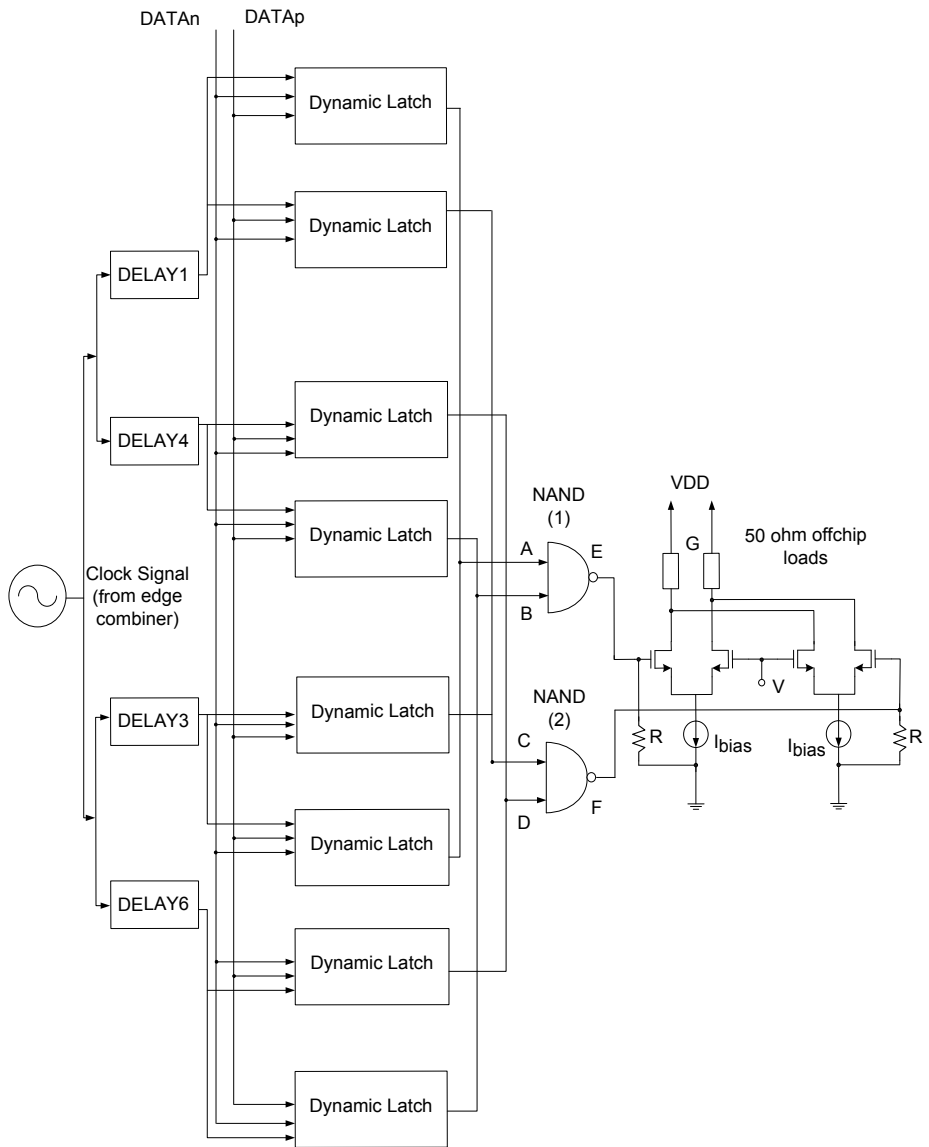
### **4.2.2 Delay Stage Block**

As shown in Figure 18, the 533 MHz signal coming from the digital edge combiner is fed into the delay stages of pulse shaper section of the transmitter. The delay stages will generate delay signals needed by the NAND1, NAND2 gates and the cross-coupled differential pairs at the output of the pulse generator.

The delay stage section contains 4 delay stages and 8 dynamic latches for signal phase inversion. The phase of the transmit pulses are switched by the digital multiplexor according to a selected direct sequence (DS) spreading code at DATAn, DATAp inputs.

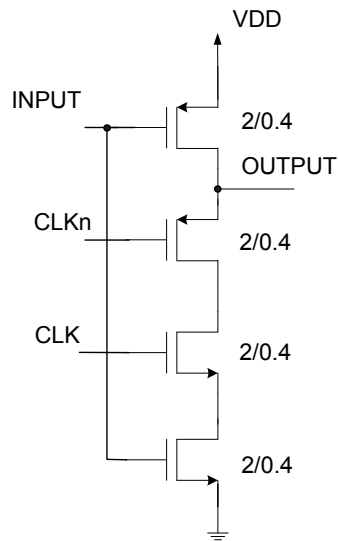
The dynamic latch used in the phase inversion stages is presented in Figure 19. One NAND gate between the digital edge combiner and the pulse generator controls the clock signal going to the pulse generator thus enabling data modulation.

As presented in Figure 18, the clock signal at the output of the digital edge combiner drives four digital delay stages, one with a single inverter delay (DELAY1), one with four inverter delays (DELAY4), one with three inverter delays (DELAY3) and one with six inverter delays (DELAY6). The delay of a single inverter is approximately 50 ps with a threshold voltage of 0.56 V.



**Fig 18. Schematic Diagram of the UWB Pulse Generator.**

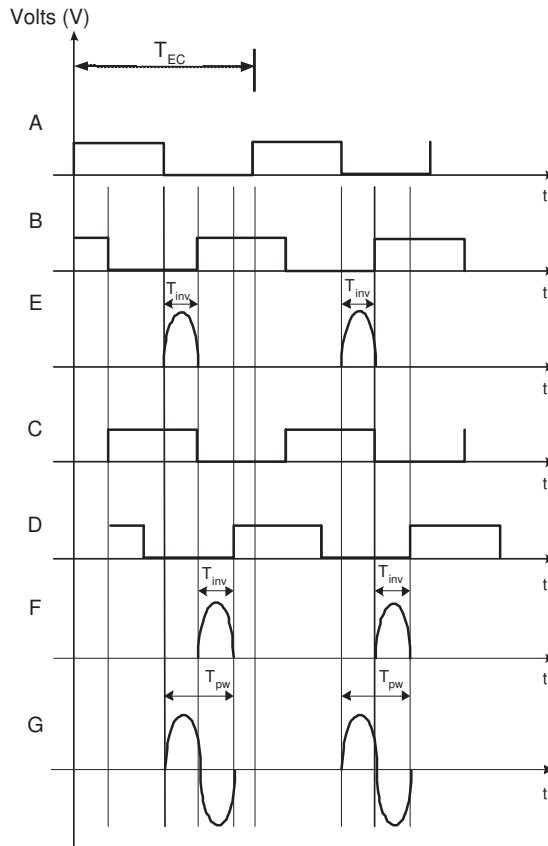




**Fig 19. Dynamic latch used in the phase inversion stages.**

The timing diagram of the signals inside the pulse generator section is presented in Figure 20. One pulse is transmitted each 1.87 ns.

The pulses formed at point E in Figure 20, are formed by the NAND1 gate since signals A and B are delayed differently by the delay stages DELAY1 and DELAY3. The pulses formed at point F in Figure 20, are formed by the NAND2 gate since signals C and D are delayed differently by the delay stages DELAY2 and DELAY4.



**Fig 20. Waveforms in Different Phases of Monocycle Generation Process Inside Pulse Generator Block.**

### **4.2.3 Pulse Shaper Block**

The pulse shaper section shown in Figure 18 takes the signals coming from the delay stages and combines them through the NAND1 and NAND2 gates. The cross-coupled differential pair will subtract the signals coming from the NAND gates, and produce an approximation of the Gaussian monocycle. One of the differential pairs will generate the difference between the signal at point E and the voltage V which is  $E - V$ , while the other pair will provide the signal  $F - V$ . The output of the cross-coupled differential pairs will be the difference between the signals at point E and F, respectively, which is

$$E - V - (F - V) = E - F.$$

When DATAn is negative (so DATAp is positive), the output of the NAND1 gate is first fed into the differential pair and then a  $0^0$  phase pulse is transmitted. When DATAn is positive (so DATAp is negative) then the output of the NAND2 gate is first fed into the differential pair and then a  $180^0$  phase pulse is transmitted. The resistors R at the input of the differential pairs reduces the swing of the signal at the inputs of the differential pairs. The pulse generator delay structure is very robust against the duty cycle variation of the synthesized 533 MHz clock signal, being able to produce pulses in a range of clock signal duty cycle of 5% to 95%. The minimum width of the pulses at points E and F, is given by the delay through the NAND1 and NAND2 gates. Therefore, the shorter the propagation time of the NAND gates, the shorter the pulse width will be. Thus the pulse width is scalable with the latest digital IC processes. Lower delay values for the inverters of newer digital CMOS processes will decrease even more the width of the generated Gaussian monocycles. The bias current through the cross coupled differential pairs can also affect the pulse width, since the unity gain bandwidth of the differential pairs depends on the transconductance of the NMOS transistors. Therefore, by increasing the bias current through the differential pairs, the transconductance of the NMOS transistors will increase which increases the unity gain bandwidth of the cross-coupled differential pairs.

### 4.3 Clock Multiplication Block

One of the main advantages of the DLL based frequency synthesizers when compared with PLL based frequency synthesizers is the inherent stability and lower design complexity, since DLLs do not use VCOs in their architecture (89), (134).

The clock multiplication sections contain a DLL and a digital edge combiner. Unlike PLL frequency synthesizers, the DLL contains a voltage controlled delay line (VCDL) instead of a VCO. The jitter in a ring-oscillator based VCO is proportional to the number of ring stages, the jitter contribution per stage, and a PLL accumulation factor, which is inversely proportional to the square-root of the bandwidth of the PLL (52). For a DLL, the result is the same, except the noise enhancement factor is 1 (52). Therefore, a DLL based clock synthesizer is less noisy than one based on a PLL (52). This is also true because, since the noise injected into a DLL disappears at the end of the delay line, whereas it is recirculated in an oscillator.

The DLL's VCDL generates 16 equally delayed replicas of the reference clock. The

digital edge combiner combines the equally spaced input clock signals, and produces a clock signal with a frequency 16 times higher than that of reference signal frequency. As opposed to a VCO which uses inductors, the VCDL uses a simple delay line and thus has a lower die area. The edge combiner was implemented with digital gates instead of an analogue solution since it requires less area, generates less noise, consumes less current and is scalable with digital processes. In subsection 4.3.1, the DLL based clock multiplier is presented. In subsection 4.3.2, the digital edge combiner is presented.

### ***4.3.1 DLL Based Clock Multiplier Block***

A block diagram of the DLL based frequency synthesis section together with the input and output signals are presented in Figure 21. The structure of the DLL is very similar to that of a charge-pump PLL, where instead of the VCO, a VCDL is used (88). The propagation time of the delay line is locked to the reference clock cycle with a DLL. The delay detector architecture is presented in Figure 22.

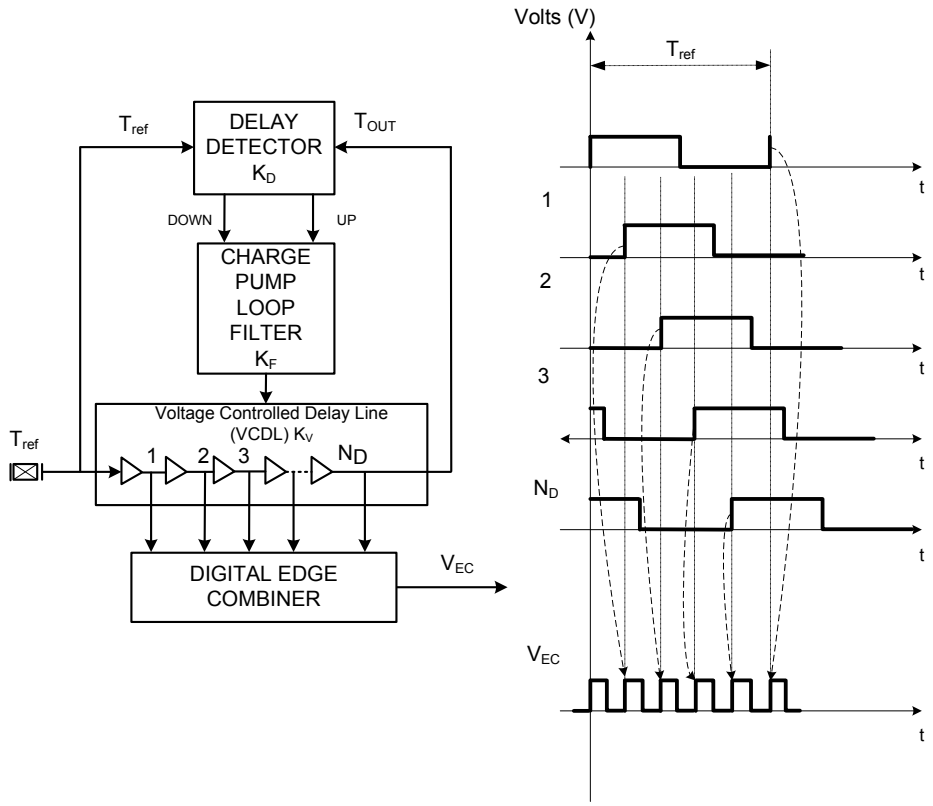


Fig 21. DLL Based Frequency Synthesis Approach.

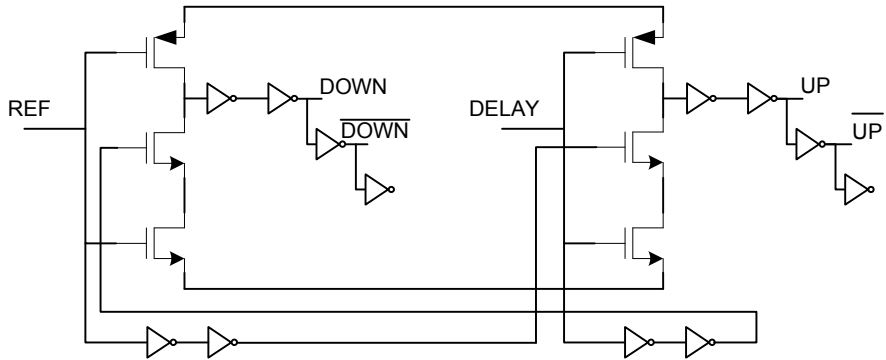


Fig 22. Delay Detector Used in the DLL Architecture.

A delay detector (DD) compares the rising edges of a buffered reference clock ( $V_{REF}$ ) with the buffered output of the last delay cell ( $V_{VCDL}$ ). The phase in radians of the input clock signal is related to the phase of the output clock signal coming from the voltage controlled delay line (VCDL), by (12):

$$T_{out} = T_{ref} + t_0 \cdot \frac{2\pi}{T_{ref}}, \quad (23)$$

where  $T_{ref}$  is the period of the reference clock and  $t_0$  is the delay time of the VCDL. The gain of the VCDL in terms of the delay  $t_0$  is given by (12):

$$t_0 = K_V \cdot V_c, \quad (24)$$

where  $K_V$  has units of seconds/V and  $V_c$  is the control voltage of the VCDL coming from the loop filter charge pump as shown in Figure 23. The total delay of the VCDL of our implementation is between 16 ns and 100 ns which is between  $T_{ref}/2$  and  $3.3T_{ref}$ . The output voltage of the loop filter is given by (12):

$$V_c = T_{out} \cdot K_D \cdot K_F, \quad (25)$$

where  $K_F = \frac{1}{sC_{loop}}$  since the loop filter is a simple capacitor  $C_{loop}$ , which makes the DLL a first-order feedback loop. The transfer function of the DLL is given by (12):

$$H_{DLL}(s) = \frac{T_{out}}{T_{ref}} = \frac{1}{1 - K_D \cdot K_F \cdot K_V \cdot \frac{2\pi}{T_{ref}}}, \quad (26)$$

where  $K_D = -\frac{I_{pump}}{\pi}$  in amps/radian is the gain of the delay detector and  $I_{pump}$  is the charge pump current. The gain has a negative value since provides a negative feedback around the loop.

The transfer function of the DLL which relates the input signal with the time-shifted output can be presented as:

$$H_{DLL}(s) = \frac{T_{out}}{T_{in}} = \frac{s}{s + K_V \frac{2I_{pump}}{C_{loop}T_{ref}}}. \quad (27)$$

The change in the output phase  $T_{out}$  due to a step input change of the input phase  $\Delta T_{ref}$  can be presented as:

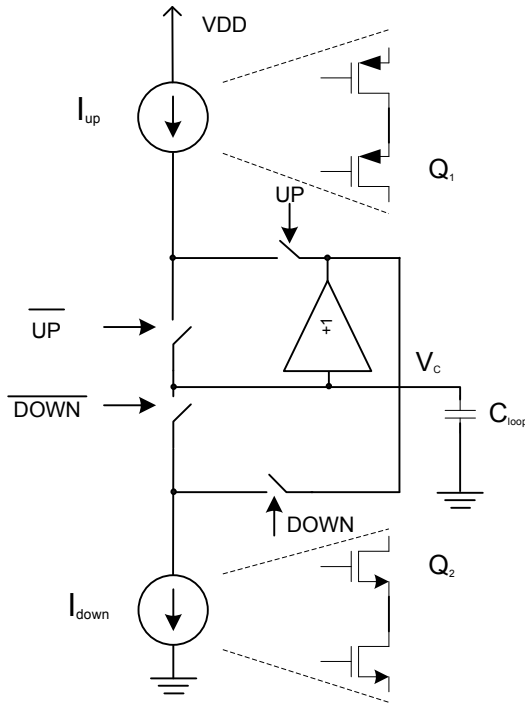
$$\Delta T_{out} = \frac{\Delta T_{ref}}{s + K_V \frac{2I_{pump}}{C_{loop}T_{ref}}}. \quad (28)$$

The time it takes the DLL to respond to an input step in phase is given by:

$$T_{react} = 2.2 \frac{C_{loop} T_{ref}}{K_V 2 I_{pump}}. \quad (29)$$

The reaction time of the DLL can be decreased by using low values for the  $\frac{C_{loop}}{I_{pump}}$ , since it will increase the ripple on the control voltage  $V_c$  of the VCDL. For our DLL, the ratio  $\frac{C_{loop}}{I_{pump}}$  has a value of approximately  $4 \cdot 10^{-7}$ .

The charge pump architecture is presented in Figure 23. We have used a single-ended charge-pump with an active amplifier (90), (91).



**Fig 23. Charge-pump Used in the DLL Architecture.**

Both, upper and lower charge pump current sources  $I_{up}$  and  $I_{down}$  are implemented by wide-swing cascode current mirrors (47) so that the signal swing of the control voltage of the VCDL at the output of the delay detector/charge pump system, is not limited. In addition, the wide-swing cascode current mirrors will provide a good match

between  $I_{up}$  and  $I_{down}$  current sources. Therefore the level of frequency spurs at the output of the clock multiplier section is low, which will minimize the interference with other existing RF systems.

Another important figure of merit for clock multipliers used in RF applications is phase noise. The phase noise is related to the ratio of the offset frequency to the clock's multiplier frequency, as shown by (124):

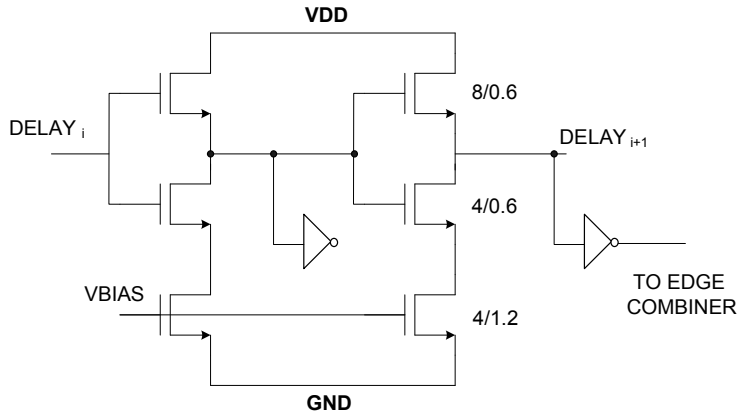
$$S_{\Phi} \approx \frac{f_0}{f_m^2} \left( \frac{\Delta\tau_{rms}}{T_0} \right)^2, \quad (30)$$

where  $f_0$  is the output frequency of the clock multiplier,  $f_m$  is the offset from  $f_0$  and  $\frac{\Delta\tau_{rms}}{T_0}$  is the instantaneous error in the period of oscillation. The phase noise produced by our DLL is small due to the low value of the instantaneous error in the period of oscillation. Therefore the interference with existing RF systems is minimized. A high signal swing is desirable in order to be able to control the control voltage of the VCDL and bring the DLL into the 'lock' state.

The operational amplifier used in unity gain configuration will set the voltage of the drains of  $Q_1$ ,  $Q_2$  in Figure 23 to the voltage of the output node when the switch is OFF, and will reduce the charge sharing effect when the switch is turned ON. When both  $\overline{UP}$  and  $\overline{DOWN}$  switches are off,  $Q_2$  will discharge to ground and  $Q_1$  will charge towards VDD. At the time of the next comparison, when both  $\overline{UP}$  and  $\overline{DOWN}$  switches are ON, the voltage at the drain of  $Q_2$  will rise and the voltage at drain of  $Q_1$  falls until  $V_{DQ1} = V_{DQ2} = V_c$ . When the delay difference between the reference input and the output of the VCDL is zero, then  $I_{D1} = I_{D2}$ . Without the unity gain amplifier,  $V_c$  will not remain constant after both  $\overline{UP}$  and  $\overline{DOWN}$  switches are on.

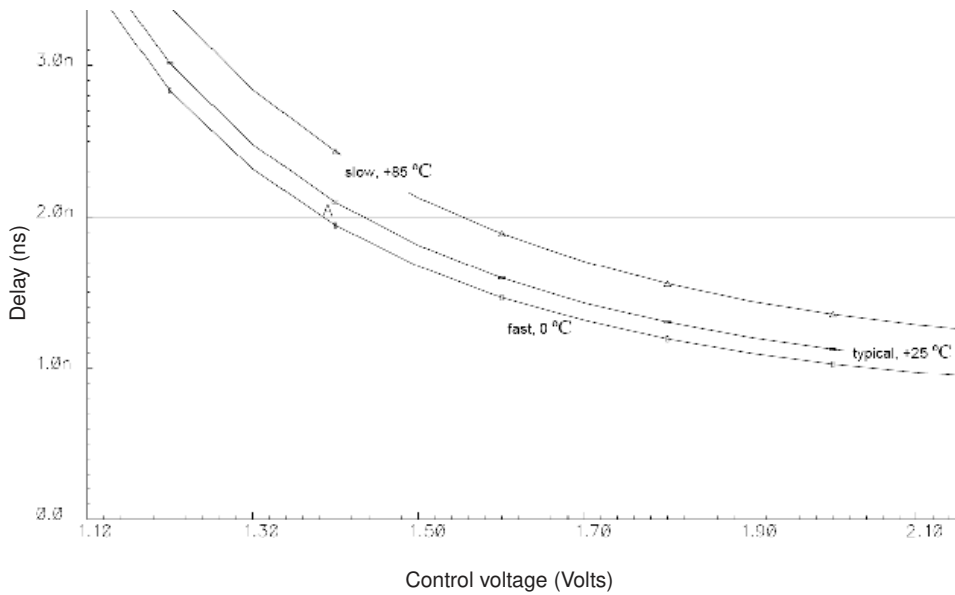
The VCDL consists of  $N_D$  delay stages. The input of the first delay stage is connected to the charge-pump, while the output of the last delay stage is connected to the input of the delay detector as shown in Figure 21. Therefore, the feedback loop of the DLL is established by the VCDL. The output of each delay cell is connected to the input of the next delay cell and buffered to provide the multiple clock phases. An identical buffering tree is connected to all delay cells to have equal loading and thus equal propagation delay in all branches. The PD controls the charge pump so that the voltage of the loop filter capacitor sets the propagation delay of the VCDL equal to a clock cycle. The delay cell consists of two identical current starved inverters (48) and is presented in Figure 24.





**Fig 24. Schematic Diagram of One Delay Element.**

The temperature behaviour of one delay cell is presented in Figure 25. For a nominal delay of 2 ns, the difference in control voltage for the whole temperature range is 200mV, which can be easily compensated by the phase detector and the charge-pump.



**Fig 25. Temperature Behaviour of One Delay Element between 0 - 85 °C.**

The control voltage of the phase detector/charge-pump section reach its stable value in approximately  $2 \mu\text{s}$ . Therefore, the DLL will reach the locked state in  $2 \mu\text{s}$ .

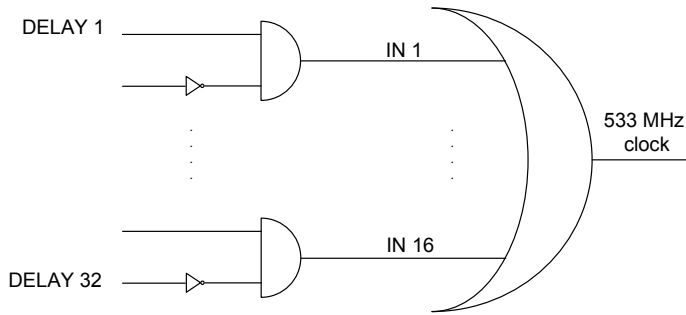
In order to reduce power consumption, a clock reference frequency as low as possible has been chosen, settling on 33.33 MHz. The unit delay and the number of delay cells of the DLL have been designed in order to obtain the desired pulse repetition frequency of 533 MHz. Table 4 shows the dominant component for power consumption of the transmitter is the DLL. The power consumption of the circuits presented in Table 4, have been calculating by determining the average current consumption of the circuits and then multiplying it with the voltage supply value.

**Table 4. Power Consumption of the Implemented UWB-IR Transmitter Components at an Reference Clock Frequency of 33.33 MHz.**

Block	Value
Charge pump	1.93mW
Delay detector	0.43mW
Delay line	3.9mW
Edge combiner	1.2mW
Pulse generator	12.8mW

### **4.3.2 Digital Edge Combiner**

The function of the edge combiner is to take the outputs of the DLL and generate a 533 MHz signal. Each delayed version  $\text{DELAY}_i$ ,  $i = 1, \dots, 32$ , of the reference clock is fed to the AND gate as shown in Figure 26. Then each output of the AND gate,  $\text{IN}_j$ ,  $j = 1, \dots, 16$ , is fed into the OR gate. The RF 533 MHz clock signal is produced at the output of the OR gate. In Figure 26 the digital edge combiner based on AND-OR gates is presented.



**Fig 26. Schematic Diagram of the Digital Edge Combiner.**

The circuit layout must be highly symmetric in order to obtain equal delay times for each delay cell.

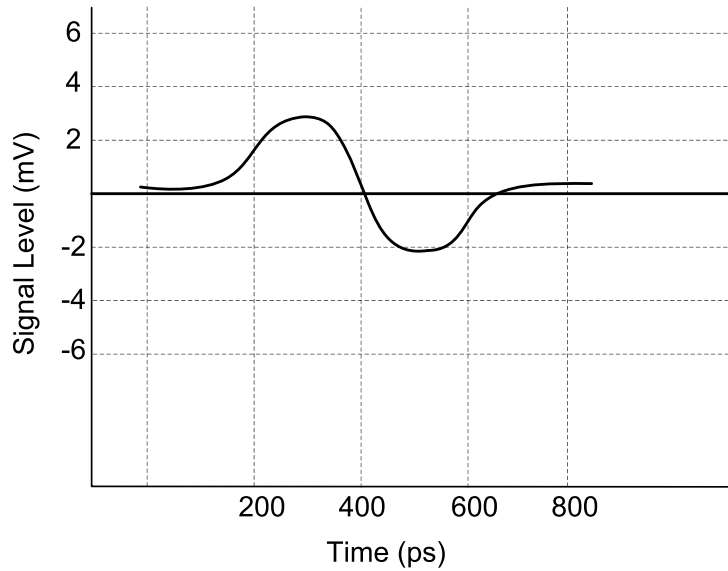
#### **4.4 Measured Results of the UWB-IR Transmitter**

In Table 5, some of the key parameters of the UWB-IR transmitter are presented.

**Table 5. Main Parameters of the 0.35  $\mu\text{m}$  CMOS UWB-IR Gaussian Transmitter.**

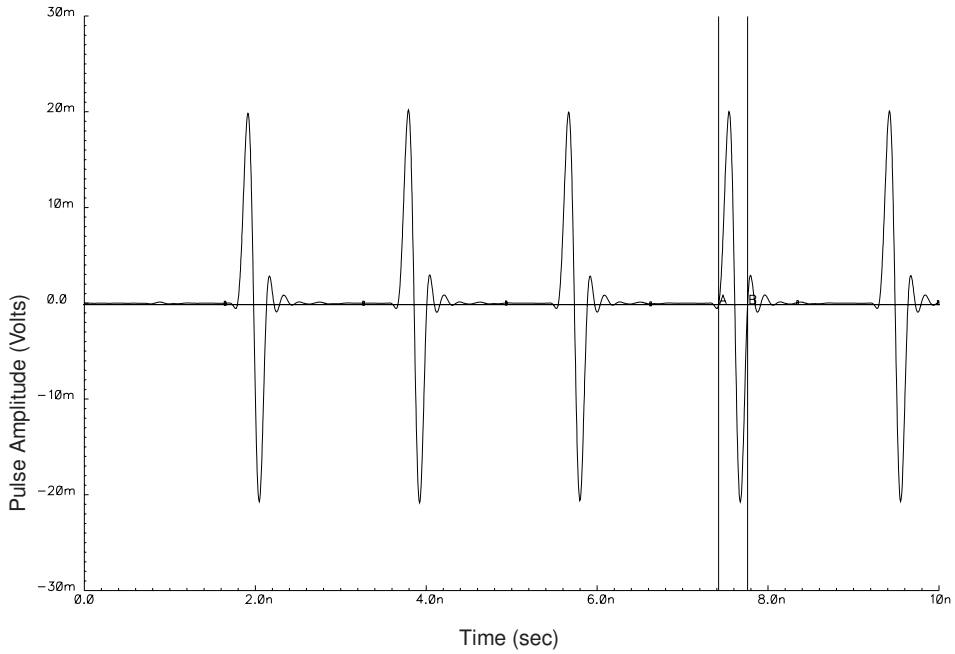
Parameter name	Values
Transmitter Area	400 $\mu\text{m}$ x 400 $\mu\text{m}$
Current consumption (simulated)	6.2mA
Power supply	3.3V
Power consumption (simulated)	20mW
Bandwidth (-10dB)	4.7GHz
Center frequency	3.2GHz

The UWB-IR transmitter has been designed using the 0.35  $\mu\text{m}$  BiCMOS AMS process. The die area of the transmitter is 400 $\mu\text{m}$  by 400 $\mu\text{m}$ . The power consumption is 20 mW. The simulated pulse width is 340 ps while the measured pulse width is approximately 700 ps. The measured pulse waveform at the output of the transmitter is presented in Figure 27.



**Fig 27. Measured Pulse Waveform at the Output of the UWB Transmitter (Amplitude Scale is at 2 mV per division).**

The transmitted waveform has been determined by measuring the signal at the output of the testbed presented in Figure 65 with the HP - INFINIUM<sup>TM</sup> oscilloscope. The external clock signal generator was connected to the testbed by a coaxial cable. The testbed was connected to the oscilloscope by a 50  $\Omega$  coaxial cable. The pulse width increases due to the parasitic on the debugging board and the parasitic between the debugging board and the transceiver IC. Without parasitics, the measured pulse would be approximately the same as the simulated one. Figure 28 shows a pulse train obtained from a post-layout simulation of the transmitter over a period of 10 ns.

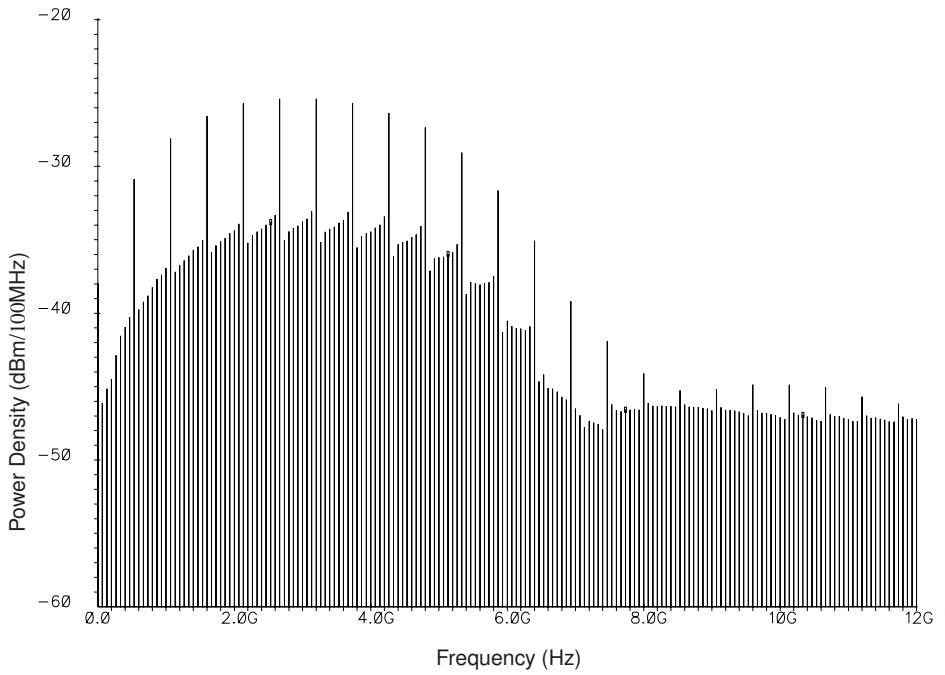


A: (7.42 ns -86.51u) delta: (339.21 ps -5.31u)      B: (7.76 ns -91.82u) slope: -15.66K

**Fig 28. Simulated UWB Pulse Generator Output.**

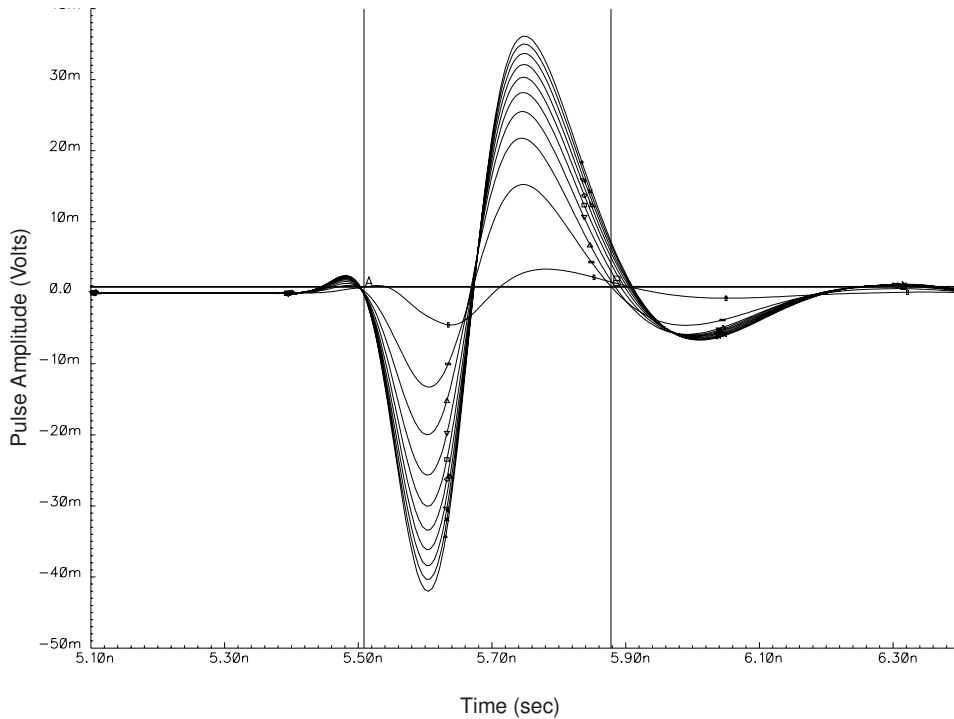
The simulated pulse train shown was produced without any randomization technique, thus strong lines are apparent in the signal spectrum. It is seen that the typical impulse generated by the circuit is a 340 ps-wide monocycle waveform. The simulated parameters of the transmitter were validated by the Cadence SpectreRF<sup>TM</sup> simulator.

The spectrum of the train of pulses is presented in Figure 29. The -10 dB bandwidth of the UWB transmitted signal is 4.7 GHz as shown in Figure 29.



**Fig 29. Simulated UWB Pulse Generator Output Spectrum (No Randomization Applied).**

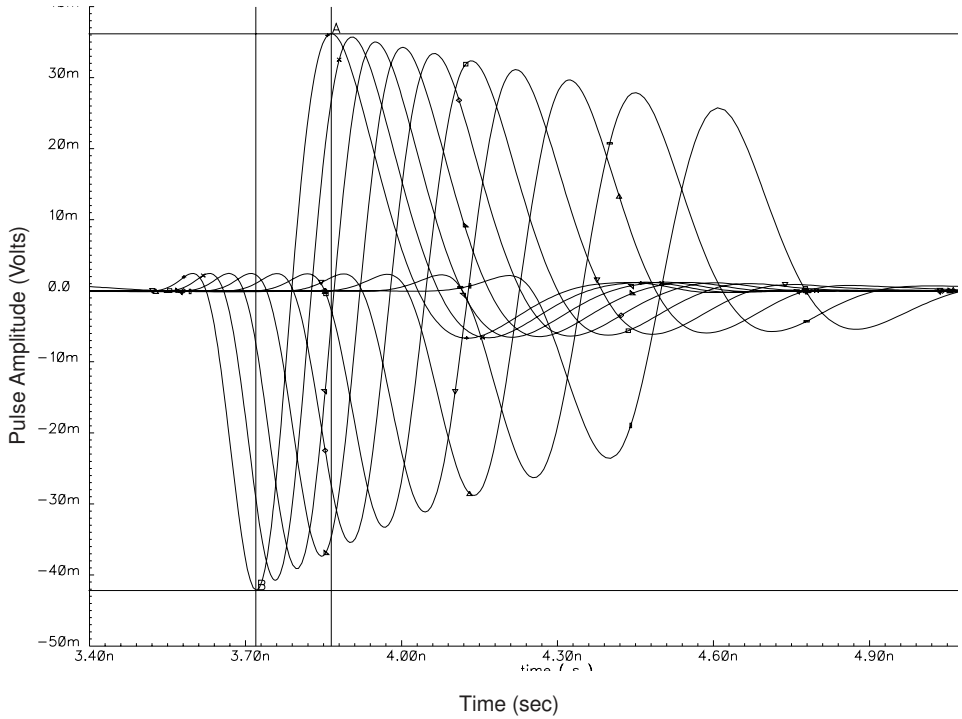
Notice that since the train of pulses simulated has a duration of 10ns, the spectrum resolution is of 100MHz. As such, for comparison with the FCC mask, the values of Figure 29 must decrease by  $10\log(100) = 20$  dB, because the FCC mask is defined using a resolution of 1MHz. The centre frequency of the pulse is 3.2 GHz.



A: (5.50 ns 804-72u) delta: (368.37 ps 59.47u)    B: (5.87 ns 864.20u) slope: 161.45K

**Fig 30. Simulated UWB Pulse with Bias Current Variation From 10  $\mu\text{A}$  to 500  $\mu\text{A}$  (Nominal 350 ps Pulse).**

The variation of pulse parameters with VDD variation is presented in Figure 31.



A: (3.86 ns 36.194m) delta: (-145.06p -78.35m) B: (3.72 ns -42.15m) slope: 540.099M

**Fig 31. Simulated UWB Pulse with Power Supply Variation From 2 V to 3.3 V (Nominal 350 ps Pulse).**

The variation of pulse amplitude and pulse width with VDD is presented in Table 6. The pulse amplitude and pulse width vary proportionally with the power supply voltage.

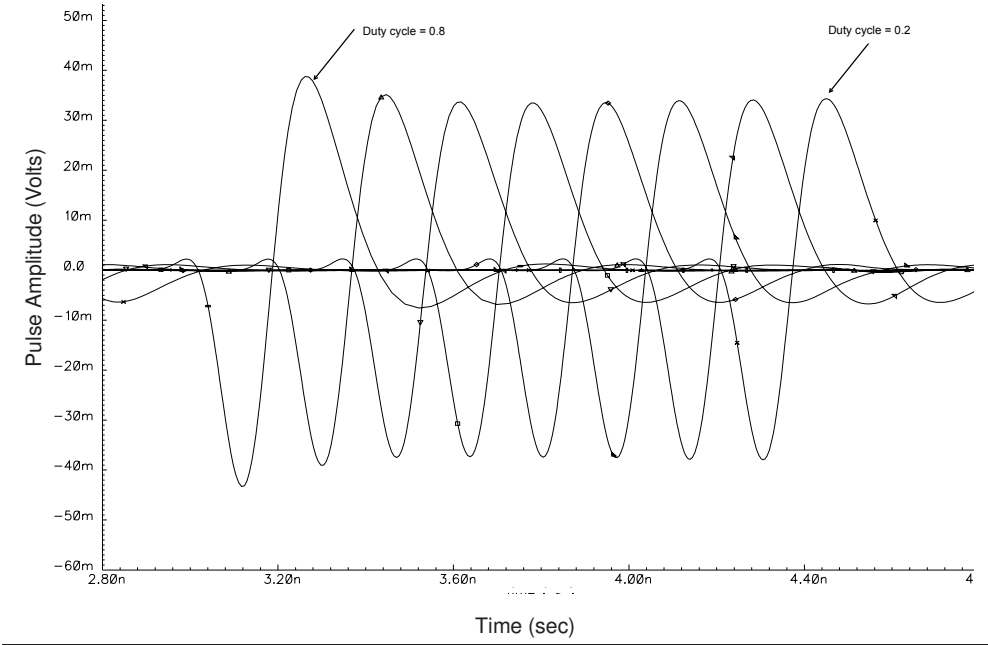
**Table 6. Simulated Pulse Parameters with VDD Variation (Nominal 350 ps Pulse).**

VDD (V)	Pulse Width (ps)	Pulse Amplitude (mV)
3.3	380	78
3.0	418	73
2.7	435	68
2.4	450	62
2.0	525	49



Even higher values can be obtained by increasing the bias current in the output amplifier, by using better processes which allows higher currents densities in the transistors, by using bipolar differential pairs instead of the CMOS ones or by using antennas with higher impedance values. If the desired output voltage of the pulse of 1 V is delivered across a  $50 \Omega$  antenna, the amount of bias current in the output amplifier must be 20 mA. Increasing the bias current in the output amplifier will increase the overall power consumption of the transmitter. Bipolar transistors will offer higher speed when compared with CMOS. However, then a BiCMOS process is required to design the transmitter.

The variation of pulse amplitude and pulse width with duty cycle of the DLL's clock is presented in Figure 32. The output pulse shape is preserved for a duty cycle value between 0.15 to 0.95. Due to the digital triggering of the pulse generator by the signal coming from the digital edge combiner, the monocycle generation process is highly tolerant against duty cycle variation of the clock signal.



**Fig 32. Variation of the UWB Monocycle When DLL's Clock Duty Cycle has Values From 0.2 to 0.8 (Simulated).**

Comparing with the UWB-IR IC transmitter presented in (44), our transmitter has a much lower implementation complexity while consuming 10 times less current. When compared with the UWB-IR IC transmitter presented in (100), our transmitter consumes the same amount of current or less while using an older CMOS process. When compared with the UWB-IR IC transmitter presented in (139) where the pulse width is 800 ps, our transmitter has the same current consumption while producing a Gaussian monocycle with a width of 350 ps.

## 4.5 Conclusions

This Chapter presents the design of a Gaussian monocycle pulse generator. The circuits for generation of an approximation waveform of a Gaussian monocycle have been presented. The approximation is based on the exponential response of the first order linear network to a step like function. An overview of classical narrowband transmitters have been presented in Section 4.1. The main difference between a UWB-IR transmitter and a narrowband system transmitter is the absence of up-conversion stages which greatly simplifies the design, lower the costs due to its lower area and lowers the power consumption and generated noise levels due to the lack of VCO's.

The implemented UWB-IR transmitter contains a DLL based frequency synthesizer and a Gaussian pulse generator. The DLL based frequency synthesizer contains a DLL and a digital edge combiner. The DLL and digital edge combiner simplifies the frequency synthesizer's design due to stability of the DLL, lower generated noise, lower die area and lower power consumption.

The pulse generator contains one block for fixing a delay and the pulse shaper. The pulse shaper contains two cross-coupled differential pairs which produce a Gaussian monocycle at their output. The pulse width and the slope of the pulse are both adaptable by modifying the biasing current and the supply voltage. The pulse amplitude is attenuated and the pulse width increases due to the parasitic on the debugging board and the parasitic between the debugging board and the transceiver IC. In order to reduce the parasitic of the debugging board a package and debugging board with lower parasitic must be used. The pulse amplitude can be increased by increasing the bias current in the output amplifier, a better IC process or by using antennas with higher impedance. The pulse generator is robust against the duty cycle variation of the RF clock coming from the digital edge combiner. Operating continuously at 533 MHz pulse repetition frequency, the pulse transmitter achieves 20.48 mW to 35 mW of total power consump-

tion at  $V_{DD} = 3.3$  V. With the transmitter operating at lower duty cycles, the power consumption will decrease even further. The central frequency of the pulse is 3.2 GHz, while the -10 dB bandwidth is 4.7 GHz.

The UWB-IR transmitter's area is only  $400\mu\text{m}$  by  $400\mu\text{m}$ . The UWB-IR transmitter contains no inductors and has the advantage that it can be integrated in digital CMOS processes which are more advanced than analogue CMOS processes. Compared with other implemented IC transmitters, the transmitter presented in this thesis has the shortest pulse width for a  $0.35\mu\text{m}$  process, one of the lower current consumption values and a low implementation complexity due to the simple Gaussian pulse generation scheme.

The UWB-IR transmitter presented in this Chapter can be modified to produce any derivative of the Gaussian monocycle due to its capability of generating the positive and negative Gaussian pulses, as shown in Figure 20. Therefore, a UWB-IR transmitter which is able to transmit multiple pulse shapes, can be designed only with minor modifications of the presented architecture.



## 5 Proposed UWB-IR Non-coherent Energy Collection Receiver Design

In this Chapter the implementation of the UWB-IR ED receiver architecture is presented. The architecture for the UWB-IR transceiver is based on the non-coherent ED scheme employing BPM which collects the signal energy in different time windows and determines the transmitted bit based on the maximum detected energy. There is no correlation in the receiver and therefore the modulation must be orthogonal in the time domain. Based on the results presented in Chapter 3, it was shown that the UWB-IR ED receivers offers identical performance as the TR-BPAM receivers and does not require analogue delay lines for doublet generation further reducing the implementation complexity compared with TR receivers. At the time of writing, there was no other example of a full implementation of a UWB-IR non-coherent ED receiver. Therefore, the ED receiver has been chosen for implementation since its providing a reasonable performance versus implementation complexity trade-off.

The integration process of the receiver front-end, analogue and ADC sections is implemented in a  $0.35\ \mu\text{m}$  BiCMOS process. The most important advantages of the  $0.35\ \mu\text{m}$  process are the low cost and the widespread availability for manufacture. Compared with the  $0.35\ \mu\text{m}$  CMOS process, the  $0.35\ \mu\text{m}$  BiCMOS process used for the design of the proposed transceiver, offers devices with higher  $f_T$  and lower  $NF_{min}$ , at only a slightly process cost increase. A more detailed price-performance comparison between BiCMOS and CMOS technologies was presented in (49). The digital section of the receiver is implemented on a Field Programmable Gate Array (FPGA). FPGA implementation has the advantage of re-configurability of the internal structure.

This Chapter is set out as follows: in Section 5.1 a link budget analysis of the ED receiver is presented, in Section 5.2, the design constraints of the UWB-IR ED receiver is presented; in Section 5.3, the receiver front-end design details are presented; in Section 5.4, the design of the baseband analogue receiver section is presented; in Section 5.5, the digital baseband section is presented; in Section 5.6 the results of Chapter 5 are shown; in Section 5.7 the conclusions of Chapter 5 are presented.

## 5.1 Link Budget Analysis

The most common formula for link budget analysis is given by the UWB channel model for the frequency range from 2 - 10 GHz (70):

$$P_{RX}(f) = P_{TR}(f) + G_{RX}(f) + G_{TR}(f) - 20 \log_{10} \frac{4\pi}{f} - 20 \log_{10} d \text{ [dB]}, \quad (31)$$

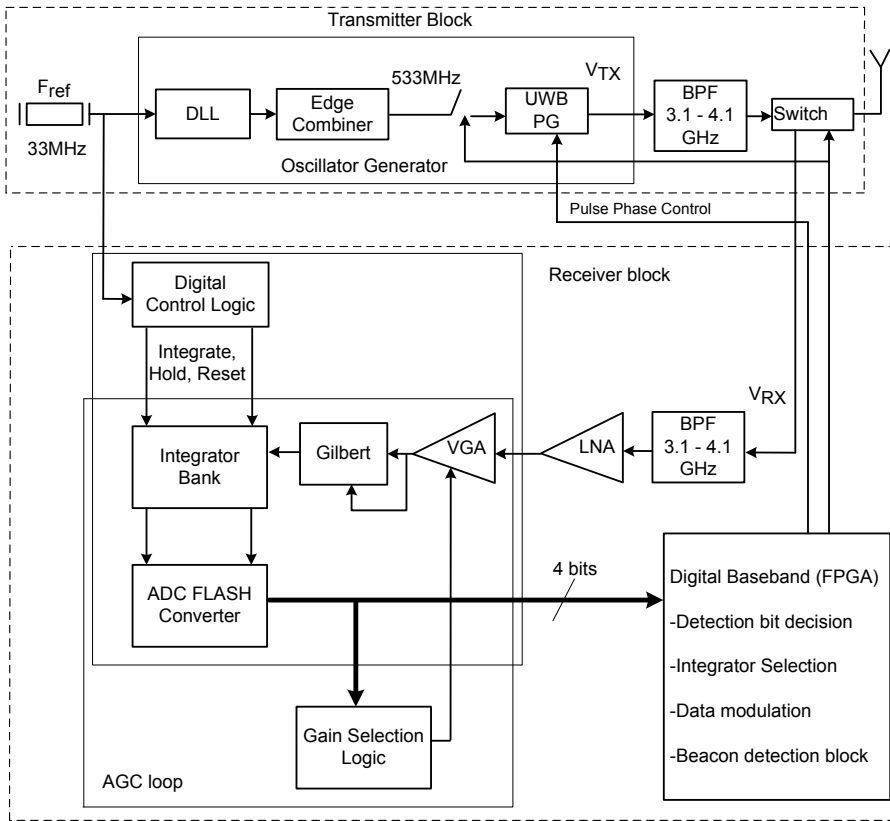
where  $P_{RX}(f)$ ,  $P_{TR}(f)$ ,  $G_{RX}(f)$  and  $G_{TR}(f)$  are frequency-dependent transmitted power, received power, receiver antenna gain and transmitter antenna gain respectively. Frequency  $f$  is expressed in [Hz],  $d$  [m] is the distance between transmitter and receiver antenna and  $c$  is the speed of light in [m/s]. We target an uncoded system data rate of 5 Mbps, an implementation loss of 5 dB and a 3.6 dB of noise figure for the receiver as acceptable design limits. The average transmitted power is  $-8.31$  dBm. The noise figure of the receiver imposes the design parameters of the LNA. The implementation loss takes into account the signal losses due to parasitics and reflections. Both the transmitter and receiver antenna are assumed to have a gain of 0 dBi. The path loss at 1 ( $L_1$ ) and 3 ( $L_3$ ) meters have been calculated with the formulas presented in Table 7. Once the transmitted power and the path loss are known, the received power  $P_{RX}$  can be obtained. Once the data rate and the noise figure of the receiver are known, the average noise power per bit  $N_{0bit}$  and the maximum supported average noise power  $P_N$  can be calculated. For binary PPM modulation, when  $R = 5$  Mbps,  $B_w = 1$  GHz,  $TW = 120$  ns and a target BER of  $BER = 10^{-3}$ , the receiver should provide an  $E_b/N_0$  of 17 dB. The minimum sensitivity level of the receiver provides the minimum signal level that can be detected at the receiver input. This means the LNA should be able to amplify a signal in the range of few  $\mu V$  in a  $50 \Omega$  system. A link budget analysis of the non-coherent EC binary PPM system is presented in Table 7.

**Table 7. Link Budget of the UWB-IR Energy Detection Transceiver.**

Parameter	Value
Data Rate ( $R$ )	5 Mbps
Average TR Power Gain ( $P_{TR}(f)$ )	-8.31 dBm
TR antenna gain ( $G_{TR}(f)$ )	0 dBi
Central Frequency ( $f_c$ )	3.6 GHz
Path Loss @ 1m: $L_1 = 20\log_{10}(4\pi f_c)$	43.56 dB
Path Loss @ 3m $L_2 = 20\log_{10} d$	9.54 dB
RX Antenna Gain ( $G_{RX}(f)$ )	0 dBi
RX Power ( $P_{RX}(f)$ )	-60.66 dBm
Average Noise Power per Bit: $N_{0bit} = -174 + 10\log_{10}(R)$	-106.85 dBm
RX Noise Figure ( $NF$ )	3.59 dB
Average Noise Power ( $P_N = N_{0bit} + NF$ )	-103.26 dBm
Minimum $E_b/N_0(S)$ (for BER = $10^{-3}$ )	17 dB
Implementation Loss	5 dB
Link Margin	21 dB
Minimum RX Sensitivity Level	-62.23 dBm

## 5.2 Design Constraints

The ED receiver architecture makes use of 8 integrators and one digital section for timing signal generation as shown in Figure 33. The grey area of the UWB-IR transceiver architecture presented in Figure 33 shows the integrated components of the transceiver. At the receiver, the signal is amplified by the LNA and VGA, squared by the Gilbert cell multiplier and then integrated by a bank of 8 integrators.



**Fig 33. Block Diagram of the Designed UWB Transceiver.**

The die photo of the implemented UWB-IR transceiver is presented in Figure 67.

In order to obtain a power consumption per bit in the order of  $100 \mu\text{W}$ , for the integrated transmitter and receiver circuits a target consumption of  $200 \text{ mW}$  was selected. The integration of the UWB-IR transceiver should be such as all the components are integrated onto a single die. In order to decrease the implementation complexity, the die area of the integrated transceiver should be as low as possible. The design constraints are presented in Table 8.

One of the most important constraints in the design of the LNA is to achieve sufficiently large gain and low noise figure so as not to introduce additional noise. This can be achieved by designing the LNA input to provide an impedance of  $50 \Omega$  because the



antenna impedance is  $50 \Omega$ . To achieve this input impedance, most LNAs use either a negative parallel resistive feedback, or a resistor in parallel at the input of the LNA (62). Both approaches have the disadvantage they decrease the LNA's noise figure. In order to have a noise figure of the receiver front-end lower than 5 dB, the LNA should have a noise figure less than 3 dB and a gain higher than 15 dB.

The integrator architecture is based on the operational transconductance amplifier (OTA) architecture presented in (132). In this paper, 5 V and 10 V voltage supplies respectively were used to design the OTA. However, due to the 3.3 V voltage supply limitation of the Si-Ge BiCMOS 70 GHz bipolar transistor process a modified architecture using PNP lateral transistors is employed. We do not use a cascade output stage for the OTA to be able to operate at the 3.3 V supply. The integrator filter should have a high DC gain for signal amplification, low power consumption for long battery life and an output signal swing of the order of few hundreds mV in order to use the whole input range of the following ADC. The integrator bandwidth requirements are dominated by the necessity to span the full range of the Gilbert multiplier output.

**Table 8. Design Constraints of the Designed UWB-IR Energy Detection Transceiver.**

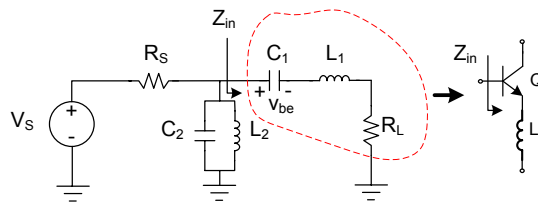
Parameter	Constraint
Die area (complexity)	Low ( $< 10 \text{ mm}^2$ )
Power consumption	Low ( $< 200 \text{ mW}$ )
Integration	High (integrated UWB-IR transceiver)

### 5.3 Receiver Front-end Implementation Design

The front-end section of the receiver contains an LNA, a VGA and a Gilbert mixer (105). The received signal is amplified by the LNA and VGA, and then is squared by the Gilbert cell. All of these three circuits are designed with the Si-Ge BiCMOS process.

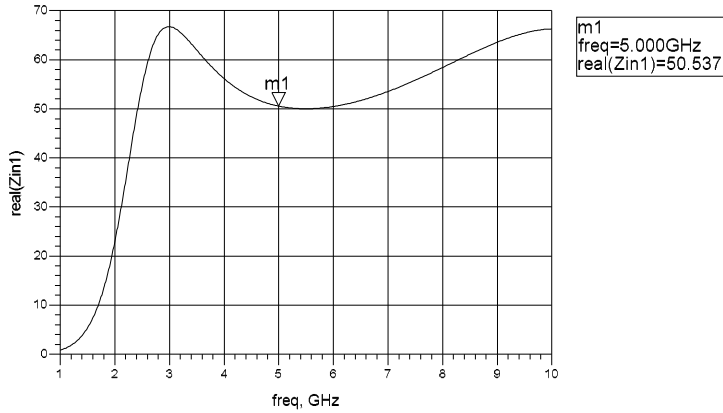
#### 5.3.1 UWB LNA Design

The UWB impedance match to  $50\ \Omega$  is included in the LNA design. The impedance match is implemented by a wideband fourth-order ladder band-pass filter consisting of inductors  $L_b$  and  $L_e$  in conjunction with the capacitors  $C_\pi$  of the input transistors ( $Q_1$ ,  $Q_2$ ) and the parasitic capacitor of the input pad  $C_{PAD}$ . The schematic of the fourth-order ladder filter is presented in Figure 34.



**Fig 34. Schematic Diagram of the Fourth-Order Ladder Filter Used for Impedance Matching in the UWB LNA.**

The input impedance provided by the filter is approximately constant in the pass-band from  $\omega_L$  to  $\omega_U$  as shown in Figure 35.



**Fig 35. Input Impedance of the Fourth-Order Ladder Filter Used for Impedance Matching.**

The values of the circuit elements of the fourth-order ladder filter can be presented as:

$$L_2 \approx \frac{R_L}{\omega_L}, C_1 \approx \frac{1}{\omega_L R_L} \quad (32)$$

$$L_1 \approx \frac{R_L}{\omega_U}, C_2 \approx \frac{1}{\omega_U R_L} \quad (33)$$

With respect with Figure 34, it is important to show that the encircled components of the filter look similar to the equivalent circuit of the  $L_e$  inductively degenerated transistor  $Q$ . Therefore, the fourth-order ladder filter includes the inductively degenerated transistor  $Q$ . We have thus obtain a broadband impedance matching of the inductively degenerated transistor.

Based on equations (32) and (33), the following values can be determined for  $C_i = 1.2$  pF and  $L_b = 2$  nH. The capacitor  $C_{PAD}$  from the LNA schematic presented in Figure 36 is presented as capacitor  $C_2$  from the input impedance fourth-order filter in Figure 34. The capacitance of the input RF pad,  $C_{PAD}$  will shunt the input signal to ground at high frequencies. As the value of  $C_{PAD}$  decreases, the bandwidth of the input signal increases.

For maximum power transfer all the current from generator  $V_S$  must flow into the

load  $R_L$ . Therefore,  $v_{be}$  is given by:

$$v_{be} = \frac{V_S}{2\omega C_1 R_L}. \quad (34)$$

The noise figure of the wideband input impedance amplifier is given by:

$$NF = 1 + \frac{|i_n + \frac{v_n}{Z_0}|}{4kTR_S}, \quad (35)$$

where  $v_n$  is the input-referred voltage source of the amplifier,  $i_n$  is the input-referred current source of the amplifier,  $k$  is Boltzmann's constant,  $T$  is temperature,  $R_S$  is the source resistance and  $Z_0 = 50 \Omega$ . The noise figure as a function of frequency is given by:

$$NF = 1 + \frac{g_m}{2} Z_0 \left( \frac{\omega}{\omega_T} \right)^2, \quad (36)$$

where  $\omega_T$  is the transit frequency of transistor  $Q$ . As the  $\omega_T$  increases, the noise figure of the LNA decreases. The noise figure degrades quadratically with frequency because the gain from the input voltage source  $V_G$  to the drive voltage across the transistor  $Q_1$  decreases with frequency.

Taking into consideration the finite base resistance of the bipolar transistors  $r_b$ , the noise figure of the LNA for a given resonance frequency  $\omega$  is given by:

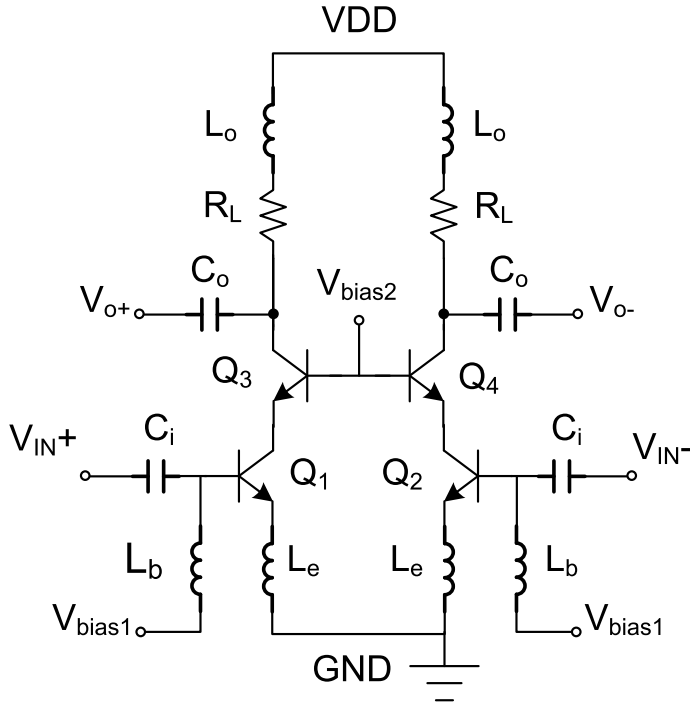
$$NF = 1 + \frac{r_b}{Z_0} + \frac{g_m}{2} Z_0 \left( \frac{\omega}{\omega_T} \right)^2, \quad (37)$$

where  $r_b$  is the base resistance of the input transistor  $Q_1$ ,  $Z_0 = 50 \Omega$ ,  $g_m$  is the transconductance of  $Q_1$ . From equation (33), equation (38) is obtain, which determines the bias current of transistor  $Q_1$ :

$$I_C = \frac{\omega_T V_T}{\omega_L Z_o}, \quad (38)$$

where  $I_C$  is the collector current shown in Figure 36,  $\omega_T$ ,  $\omega_L$ ,  $V_T$  and  $Z_o$  are the transistor's unity gain frequency, lower frequency of interest bandwidth, the transistor thermal voltage and impedance, respectively.

From equation (38), for  $f_L = 3.1$  GHz,  $f_T = 36$  GHz,  $V_T = 26$  mV and input impedance match to  $50 \Omega$ , the bias current will be 6 mA. The high frequency response of the LNA is mainly limited by the  $f_T$  frequency of the transistors, The noise performance of the LNA is mainly limited by the base resistance and minimum noise figure of the bipolar transistors available in the IC process. The schematic of the LNA employed by the ED receiver is depicted in Figure 36.



**Fig 36. Schematic Diagram of the UWB LNA.**

Maintaining low noise figure over the a ultra wide bandwidth is another concern since noise minimization is inversely proportional with bandwidth (90).

The input transistors are dimensioned to be large in order to minimize the base resistance  $r_b$ , which is a considerable source of noise. The noise performance of the amplifier is determined mainly by its minimum noise figure and noise contribution that occurs when input source admittance is different from its optimum admittance. The base resistance  $r_b$  will add noise uniformly at all frequencies and also affects the input resistance as shown by:

$$Z_{in} = \omega_T L_e + r_b. \quad (39)$$

Based on equation (39), the conclusion is that for a higher base resistance  $r_b$ , the smaller degeneration inductor  $L_e$  must be in order to achieve matching. Therefore,  $L_e = 0.4$  nH was chosen, which leads to a value of  $Z_{in}$  close to  $50 \Omega$  at 4 GHz. As the  $\omega_T$  decreases, the values of  $L_e$  and  $r_b$  increases. However, a lower value of  $\omega_T$  will decrease the

noise performance. The emitter inductance  $L_e$  can be implemented as a bonding wire if such low values for  $L_e$  are not found in the IC process used. An off-chip solution for the  $L_e$  has the advantage that chip area is reduced, the disadvantage being that the inductance of the bonding wire is hard to control. By increasing the transconductance of the transistors, a lower noise figure can be obtained at the expense of an increased power consumption. If the value of the coupling capacitor  $C_i$  is too high, then its bottom plate capacitance will add to the value of  $C_{PAD}$ , which will in turn decrease  $\omega_U$ . If the value of  $C_i$  is too low, the fourth-order bandpass filter will not meet the specification for  $\omega_L$ . Therefore, the value of  $C_i$  was chosen so as not to increase the value of  $C_{PAD}$ .

The cascode transistors  $Q_3$  and  $Q_4$  shown in Figure 36 improve the output-input isolation and decrease the Miller effect due to collector-base capacitance of  $Q_1$  (90). Since the current buffer  $Q_3$  has a wide bandwidth, the cascode circuit overall has good high-frequency performance when compared with common-emitter or common-source stage. Another useful property of the cascode stage is the small amount of reverse transmission ( $S_{12}$ ). The current-buffer  $Q_3$  provides good isolation that is required in the design of UWB amplifiers. The LNA's bias is set by voltages  $V_{b1}$  and  $V_{b2}$ . The load contains the resistor  $R_L$  and the  $L_o$  inductor. The inductive load  $L_o$  equalizes the voltage gain to a constant value across the interest bandwidth. Therefore, the LNA design uses  $L_o = 10.02$  nH and  $R_L = 11.28$   $\Omega$ . The resistive load  $R_L$  was chosen to have a low value such that the inductive region of the load impedance spans the bandwidth of interest.

### 5.3.2 Variable Gain Amplifier

The VGA design presented in Figure 37 is based on the Gilbert cell (37).

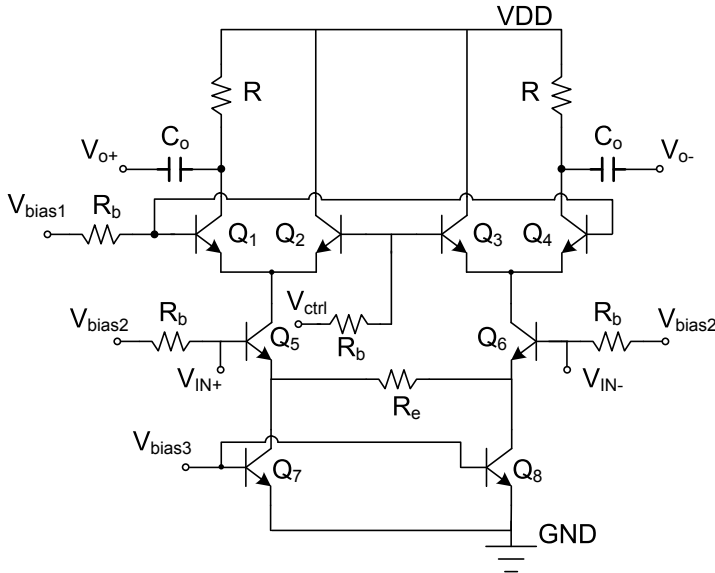


Fig 37. Schematic Diagram of the UWB VGA.

The VGA schematic was presented in (109) and is based on the architecture presented in (37). The VGA gain is adjusted by altering the control voltage  $V_{ctrl}$ . The larger the voltage, the more current is directed through transistors  $Q_2$  and  $Q_3$  and hence the current drawn by the gain transistors  $Q_1$  and  $Q_4$  is decreased, which reduces the gain of the amplifier. The VGA's noise figure has a minimum value when the maximum gain is used. This is due to the fact that the transistors  $Q_2$  and  $Q_3$  are switched off and contribute no noise when all the current is directed through transistors  $Q_1$  and  $Q_4$ . The maximum noise occurs with a 6 dB gain reduction when all the quad transistors draw equal currents (68). The input gain stage of the VGA contains the transistors  $Q_5$  and  $Q_6$ . The bias of the VGA is set by the bias voltages  $V_{b1}$  and  $V_{b2}$  through resistors  $R_b$  which isolates the bases from each other. The degeneration resistor  $R_e$  is used to improve linearity, the drawback being a reduction in the voltage gain of the VGA.  $R_e$  can be eliminated if higher gain is needed from the VGA.  $R_e$  improves the match between

the two current sinks used as the bias current of the VGA.

The VGA control voltage range is between 2.3 V and 2.8 V, and the corresponding gain is from -5 to 15 dB. The gain response of the VGA is presented in Figure 37. The power consumption of the VGA is 10.5 mW using a 3.3 V power supply. The outputs of the VGA are buffered by two output stages to drive the squaring circuit.

### 5.3.3 Gilbert Cell

The squaring circuit of the implemented receiver is a Gilbert cell multiplier presented in Figure 38. The Gilbert cell design is based on a double-balanced active mixer architecture presented in (105), (37). The Gilbert cell has the advantage that when the amplitude of the applied input signals  $V_{IN1}$  and  $V_{IN2}$  is smaller than  $V_T = 26$  mV, the circuit behaves like as a multiplier, developing the product of  $V_{IN1}$  and  $V_{IN2}$ . Because, both  $V_{IN1}$  and  $V_{IN2}$  are connected to the output of the VGA, the circuit will produce the square of the input signal.

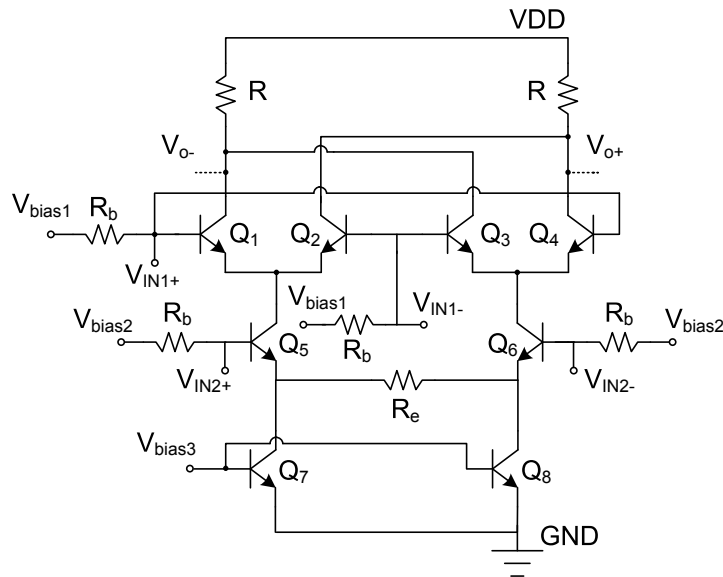


Fig 38. Schematic diagram of the Gilbert square cell.



The mixer comprises two differential cross coupled pairs ( $Q_1, Q_2, Q_3, Q_4$ ), a differential-pair driver stage ( $Q_5$  and  $Q_6$ ), a resistive load ( $R$ ) and bias current sources ( $Q_7$  and  $Q_8$ ). The driver stage amplifies the  $RF$  signal and is degenerated by the  $R_e$  resistors. The power conversion gain is related with voltage or current gain by:

$$G = \left( \frac{V_O^2}{V_{in}^2} \right) \frac{R_S}{R} = \frac{I_O}{I_{in}} \frac{R}{R_S}, \quad (40)$$

where  $R$  is the load resistance and  $R_S$  is the source resistance of the Gilbert cell.

The differential output current of the Gilbert cell is given by:

$$\Delta I_{out} = I_{bias} \left[ \tanh \left( \frac{V_{IN1}}{2V_T} \right) \tanh \left( \frac{V_{IN2}}{2V_T} \right) \right], \quad (41)$$

where  $I_{bias}$  is the bias current and  $V_T = 26$  mV is the thermal voltage. The differential output current can be described as (31):

$$\Delta I_{out} = I_{bias} \left[ \left( \frac{V_{IN1}}{2V_T} \right) \left( \frac{V_{IN2}}{2V_T} \right) \right] \quad (42)$$

The main difference of the Gilbert cell when compared with classical narrowband receivers is that it is used as a multiplier and not as a modulator since the ED receiver does not use a local oscillator (LO). In classical correlation receiver structures, the time-varying elements in the Gilbert cell mixer in the presence of the small-signal RF excitation give rise to mixing frequencies represented as (46):

$$\omega_n = \omega_{if} + n\omega_{LO}, n = 0, \pm 1, \pm 2, \pm 3, \dots \quad (43)$$

where  $\omega_{if} = |\omega_{LO} - \omega_{rf}|$  is the intermediate angular (IF) frequency and  $\omega_{rf}$  and  $\omega_{LO}$  are the RF and LO angular frequencies, respectively. In the ED receiver design, since a LO to switch the Gilbert cell at the receiver is not used, and  $\omega_{rf}$  is used instead of  $\omega_{LO}$ , the following equality can be written:

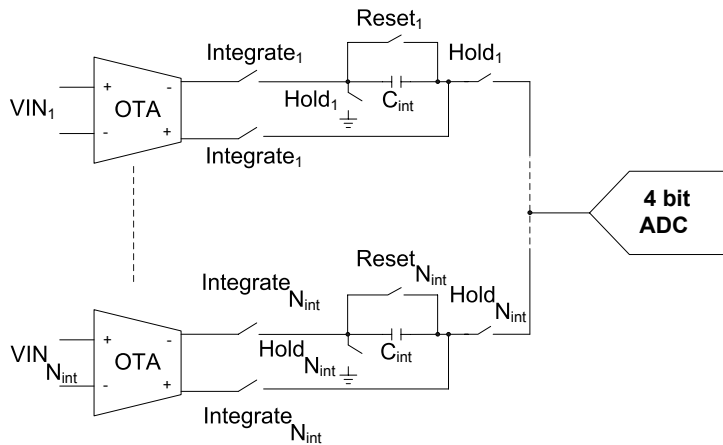
$$\omega_{rf} = \omega_{LO}. \quad (44)$$

The intermediate frequency becomes  $\omega_{if} = |\omega_{LO} - \omega_{rf}| = 0$ . This is why the EC receiver is considered as a direct conversion receiver with baseband detection. Usually, correlation based receivers need special design to improve the isolation between LO and RF ports of the mixer. This is no longer a design issue for EC receivers, since there is no LO-to-RF feedthrough caused by the leaking of the local oscillator signal to the antenna. This will relax the design of the reverse isolation parameter of the LNA. The

common mode (CM) voltage at the output of the Gilbert multiplier is 2.3 V which is sufficient to drive all the following 8 integrators. The power consumption of the Gilbert cell is 3.96 mW with a 3.3 V voltage supply.

## 5.4 Analogue Baseband Receiver Design

The analogue baseband receiver includes the integrator bank and the ADC converter as shown in Figure 33. The structure of the ED receiver stage together with Integrate, Hold and Reset timing signals is shown in Figure 39. The Integrate, Hold and Reset timing signals are generated by the digital control logic circuits as shown in Figure 33. A bank of operational transconductance amplifiers (OTA) amplifiers are coupled to the outputs of the Gilbert cell and will integrate their output currents using integration capacitors  $C_{int}$ . Each integration capacitor has the same value of  $C_{int}$ . After integration, the voltage across  $C_{int}$  will be held for digital conversion, then  $C_{int}$  will be discharged.



**Fig 39. Block Diagram Detail of the Energy Detection Receiver Architecture.**



where  $I_{C5}$  and  $I_{E2}$  are the collector and emitter currents of  $Q_5$  and  $Q_2$ . The total transconductance of the designed OTA, is given by:

$$g_{mOTA} = \frac{i_{out}}{v_{in}} = g_{mIN} \frac{g_{m5}}{g_{m3}}, \quad (48)$$

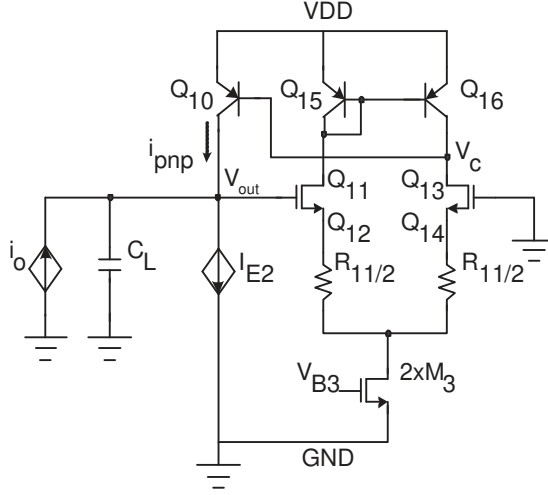
where  $i_{out}$  and  $v_{in}$  are the output current and input voltage of the OTA. Ideally, a transconductor should have infinite input and output impedances. The differential output impedance is the sum of the output conductances of  $Q_5$ ,  $Q_6$ , the load devices  $Q_9$ ,  $Q_{10}$  and the input impedance of the common mode feedback (CMFB) circuit. The differential output conductance for low frequencies is given by:

$$G_o = \frac{1}{2r_{o5}} + \frac{1}{2r_{o9}} + \frac{1}{2r_{CMF}}, \quad (49)$$

where  $r_{o5}$ ,  $r_{o9}$  are output impedances of  $Q_5$  and  $Q_9$ , respectively and  $r_{CMF}$  is the input impedance of the CMFB circuit. In order to assure a high output impedance of the OTA, the input impedance of the CMFB circuit  $r_{CMF}$  should be high enough so that  $r_{CMF} \gg r_{o9}$ . The value of  $r_{CMF}$  is very high due to the CMOS transistors used in the CMFB circuit. The total output impedance is primarily limited by the output impedance of the PNP lateral load  $r_{o9}$ .

#### 5.4.1 Common Mode Feedback Analysis

As shown in Figure 33, the integrator bank will provide the output value after the integration to the ADC converter. The OTA cell is a fully-differential operational amplifier. The applied feedback determines the differential signals, but not the common mode signals. Therefore, the common-mode feedback circuit (CMFB) will determine the output common mode voltage at a value equal with  $V_{CM}$  as shown in Figure 40. For CM signals, the CMFB circuit can be converted to a single differential pair presented in Figure 41. Referring to Figure 41,  $V_{OUT}$  is denoted as the input voltage of the CMFB circuit which is generated by the current  $i_o$  flowing into the impedance at node  $OUT$ . The feedback mechanism of the CMFB circuit works as follows: by increasing  $i_o$  the value of  $V_{OUT}$  increases which makes  $V_C$  rise. When  $V_C$  rises, the forward bias of the  $PNP$  transistor is reduced so that  $i_{pnp}$  is reduced causing  $V_{OUT}$  to reduce.



**Fig 41. Common-Mode Feedback Circuit: Half-Circuit Equivalent for Common Mode Signals.**

The stability of the CM feedback loop can be achieved by the integrator capacitor  $C_{int}$  only when it is connected between the output branches and ground. In Figure 41, load capacitor  $C_L$  includes the integration capacitor  $C_{int}$ , the parasitic capacitance as well as the input capacitance of the ADC comparators. If the integrator capacitor is placed between the output branches, the stability conditions can still be satisfied provided the loop gain of the CMFB circuit is decreased or, alternatively, additional capacitors  $C$  are applied forming a feed forward zero with resistors  $R$ . An example of such a design is shown in (132). The CMFB circuit loop gain can be decreased by decreasing either  $I_{E3}$ ,  $I_{E2}$  or both.

The frequency response of the transconductance is an approximated version of equation (33) from (132):

$$g_m(s) = \frac{g_{mtotal}}{1 + s\tau} = \frac{I_{E2}}{2I_{E1}R_1(1 + \frac{s}{\omega_{p1}})}, \quad (50)$$

where  $\tau$  is the time delay of the OTA. The pole at  $-\omega_{p1}$  represent the phase contributions of all the nodes. The excess phase compensation requires cancellation of the denominator term of equation (50) which can be achieved by introducing the capacitor  $C_1$  in parallel with resistor  $R_1$ . The value of  $C_1$  required to cancel the denominator in equation

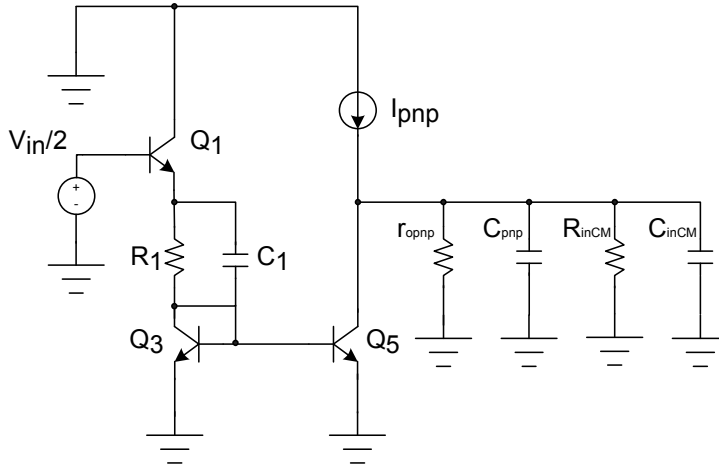
(50) is given by (132):

$$C_1 = \frac{\tau_{OTA}(\omega)}{R_1}, \quad (51)$$

where  $\tau_{OTA}$  is the time delay of the transconductor.

### 5.4.2 OTA's Frequency Response Analysis

As shown in Figure 33, the integrator will integrate the rectified pulses after the Gilbert cell. The frequency bandwidth of the OTA should be high enough so that the energy of the squared pulses is fully recovered. The analysis of its frequency response can be performed using the concept of the half circuit shown in Figure 42. In this figure,  $r_{opnp}$ ,  $c_{pnp}$  are the output resistance and capacitance of the PNP lateral source.  $R_{inCM}$ ,  $C_{inCM}$  are the input resistance and capacitance of the CMFB circuit



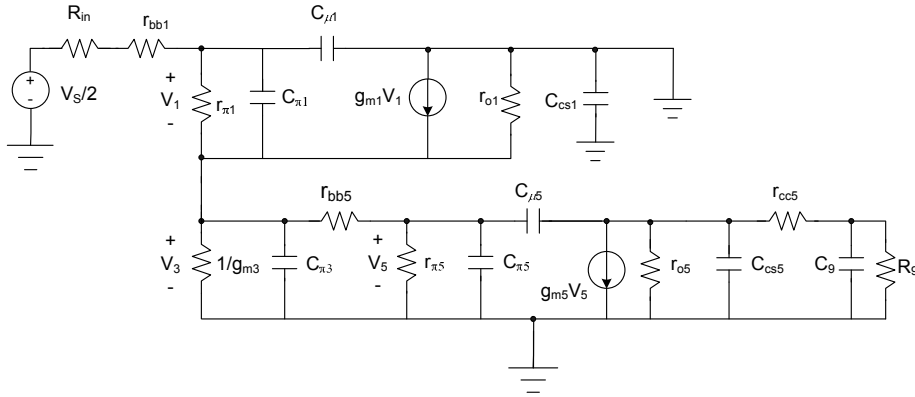
**Fig 42. Half Circuit for Frequency Analysis of the OTA.**

The transconductor works in current mode, i.e., the signal to be processed is current. The signal path of the transconductor includes three different transistor configurations, common-collector, a diode (impedance transformer), and common emitter. The signal current is then directed to the output.

The OTA also works in current mode. The input transistor works as an emitter follower with emitter follower load  $R_1$ , but with no collector load  $R_c$ . Based on the small

signal model of the OTA presented in Figure 43 and assuming that:  $r_{bb5} \ll r_{\pi5}$ ,  $g_{m3} \gg 1/r_{\pi5}$  and  $g_{m3}R_1 \gg 1$ , the impedance seen at the emitter at  $Q_1$  is given by equation (52) (132):

$$Z_{EQ1} = R_1 + \frac{\frac{1}{g_{m3} + sC_{\pi3}} \left( \frac{r_{\pi5}}{1 + sr_{\pi5}C_5} + r_{bb5} \right)}{r_{bb5} + \frac{1}{g_{m3} + sC_{\pi3}} + \frac{r_{\pi5}}{1 + sr_{\pi5}C_5}} \approx R_1. \quad (52)$$



**Fig 43. Small Signal Circuit Model of the OTA.**

A high value of  $R_1$  buffers  $Q_1$  from the effects of  $Q_3$  and  $Q_5$ . Therefore the input signal  $V_{in}$  is not affected by the voltage variations of  $Q_3$  and  $Q_5$ . Neglecting the source resistor  $R_s$ , the base resistance  $r_{bb1}$ , the output resistance  $r_{o1}$  and the collector-base capacitance  $C_{\mu1}$  of  $Q_1$ , the current through  $R_1$  is given by (132):

$$I_1 = \frac{V_{in}}{2R_1}. \quad (53)$$

Leaving the input transistor  $Q_1$ , the signal travels through a diode-connected transistor  $Q_3$  and then into the base of the current-coupled  $Q_5$ . The current through the collector of  $Q_5$  is given by:  $I_5 = -g_{m5}I_1Z_1$ , where the impedance  $Z_1$  is given by (132):

$$Z_1 = \frac{\frac{1}{g_{m3} + sC_{\pi3}} \frac{r_{\pi5}}{1 + sr_{\pi5}C_5}}{r_{bb5} + \frac{1}{g_{m3} + sC_{\pi3}} + \frac{r_{\pi5}}{1 + sr_{\pi5}C_5}} \approx \frac{1}{g_{m3} + s[C_5(1 + g_{m3}r_{bb5}) + C_{\pi3}] + s^2r_{bb5}C_{\pi3}C_5} \quad (54)$$

The transfer function of our OTA output stage can be presented as (132):

$$I_5 = \frac{g_{m5}V_s}{g_{m3} + s[C_{\pi3} + C_5(1 + g_{m3}r_{bb5})] + s^2r_{bb5}C_{\pi3}C_5}. \quad (55)$$

The dominant pole of the transfer function is given by (132):

$$p_1 = \frac{g_{m3}}{C_{\pi3} + C_5(1 + g_{m3}r_{bb5})}. \quad (56)$$

The nondominant pole of the transfer function is given by:

$$p_2 = \frac{C_{\pi3} + C_5(1 + g_{m3}r_{bb5})}{r_{bb5}C_{\pi3}C_5}. \quad (57)$$

Equations (56) and (57) clearly point out that in order to increase the bandwidth of the OTA, the capacitors  $C_{\pi3}$  and  $C_5$  should be minimized. The pole locations can be estimated as (132):

$$|p_1| > \frac{g_{m3}}{C_{\pi3}}, \quad (58)$$

$$\frac{C_{\pi3} + C_5}{C_{\pi3}C_5r_{bb5}} > |p_2| > \frac{1}{r_{bb5}C_5}. \quad (59)$$

The dominant pole of  $Q_5$  is higher than 10GHz due to the small  $C_{\pi3}$ . Therefore, the energy of the high bandwidth pulses can be fully recovered by the integrators. The low-frequency pole related to the output impedance of the OTA is ignored since it affects the output voltage, but not the output current of the transconductor. The output current is given by:

$$i_o = \frac{V_s I_2}{R_1 I_1}. \quad (60)$$

Since, the output signal of the transconductor is current, the working conditions are different from those of a voltage amplifier. The open-circuit voltage gain of the OTA can be presented as:

$$A_v = g_m Z_o, \quad (61)$$

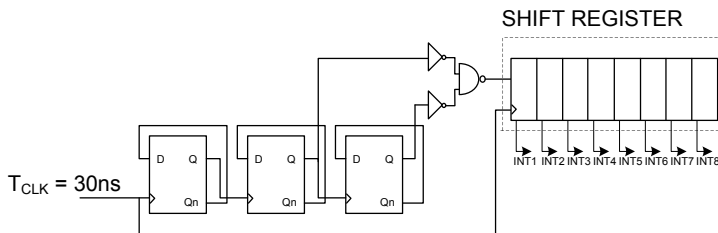
which has a dominant pole at  $\frac{1}{R_o C_o}$ , where  $R_o$ ,  $C_o$ ,  $Z_o$  are the output resistance, capacitance and impedance, respectively. The OTA has a gain of approximately 45 dB up to 10 GHz, depending on the bias current  $I_{E2}$ . The bandwidth of the OTA can be reduced by eliminating the capacitors  $C_1$ . Contrary to the case of using an op-amp in a filter integration application, a transconductor does not normally work as a feedback amplifier which eases the conditions for its stability. Under usual working conditions, the transconductor has a capacitive load given by the input capacitances of the ADC's



comparators, parasitic capacitances of the integrator and the integrating capacitance. With increasing capacitive load, the dominant pole of  $A_v$  shifts toward lower frequencies, which further increases the phase margin. The only source of instability in the transconductor is the feedback loop created by the CMFB, which for purely differential signals should be an open circuit.

### 5.4.3 Timing Circuits

The role of the digital control logic circuits is to produce the Integrate, Reset and Hold timing signals for all of the 8 integrators shown in Figure 33. The timing circuits used for generation of the Integrate signals is presented in Figure 44.



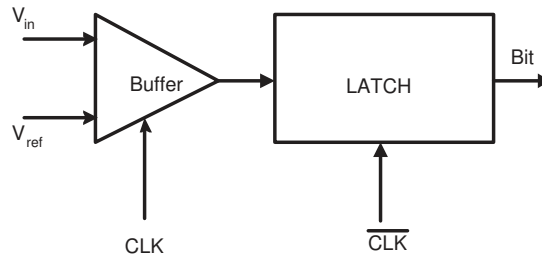
**Fig 44. Timing Signal Generator Block for Integration.**

As shown in Figure 44, the digital control logic circuits make use as a reference signal a clock signal of period  $T_{CLK} = 30$  ns, a divide-by-8 register, and a shift register. At the output of the shift register, all the integration signals  $INT_1, \dots, INT_8$  will be available. The reset timing generator circuits utilizes the integration signals coming from the integrator timing circuits. The reset signal for integrator  $i$  will be produced by an advanced version of the integrate  $INT_{i+1}$  and  $INT_{i+2}$  signals. The hold time signal generator makes use of a shift register and one NOR gate to produce the HOLD signals. All the timing circuits utilize only one external on-chip signal, namely the reference clock signal  $T_{CLK}$ . The active time duration of the Integrate, Hold and Reset active windows are  $\frac{T_b}{2}$  ns,  $\frac{T_b}{8}$  ns and  $\frac{3T_b}{8}$  ns, respectively. During the Integrate timing window, the Integrate switches are closed and the integration capacitor  $C_{int}$  will integrate the output current  $i_o$  of the OTA. During the Hold timing window the integration result is held constant at the input of the ADC. During the Reset timing window the integration capacitor  $C_{int}$  is reset.

#### 5.4.4 ADC Architecture

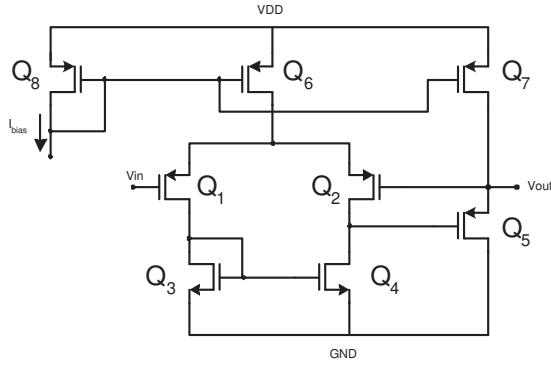
As shown in Figure 33, the ADC converts the analogue values at the output of the integrators into digital format. The ADC runs at symbol rate conversion speed and not at pulse repetition rate, which greatly reduces the power consumption of the receiver. Each integrator analogue output voltage is converted to digital format by a 4-bit parallel (FLASH) ADC architecture (47). The integrator outputs are connected to the ADC input by the Hold timing controlled switches for  $\frac{T_b}{8}$  ns once every  $T_b$  ns. In the current version of the implemented UWB-IR transceiver, only the comparators are integrated. The implemented ADC contains a bank of 15 comparators. The comparator contains one unity gain preamplifier with negative feedback (87) and one dynamic latch (114).

The outputs of the integrated comparators are in thermometer code format. The ADC's latched comparator is presented in Figure 45.



**Fig 45. Schematic Diagram of the Comparator.**

The buffer schematic is presented in Figure 46. The buffer make use of negative feedback and buffers the comparator from the noise on the data line. The negative feedback behaviour used by the buffer preamplifier may be characterized briefly as: while  $V_{in}$  increases, the current through  $Q_1$  will decrease while the current through  $Q_2$  will increase since the current through  $Q_6$  is constant. The higher current through  $Q_2$  will increase the voltage at the gate of  $Q_5$  which will decrease the current flowing through it increasing in this way the current coming from  $Q_7$  and flowing into the output node  $V_{out}$ . Thus, the  $V_{out}$  will increase and the negative feedback effect will gradually adjust  $V_{out}$  to the value of  $V_{in}$ .



**Fig 46. Schematic Diagram of the Buffer Shown in Figure 45.**

The comparator schematic is based on a clocked latch structure as shown in Figure 47. The comparison takes place when CLK is '0', so that  $Q_1$  is ON. The input level  $V_{IN}$  is compared against the reference level  $V_{REF}$ , and the result of the comparison is available at the outputs  $VOUT_p$  and  $VOUT_n$ . When  $V_{IN}$  is higher than  $V_{REF}$ ,  $VOUT_p$  is '1' and  $VOUT_n$  is '0'. When  $V_{IN}$  is lower than  $V_{REF}$ ,  $VOUT_p$  is '0' and  $VOUT_n$  is '1'. The output signals of the latches are sampled by a bank of flip-flops. When CLK = '1', the comparator is set to reset mode.  $Q_8$  and  $Q_9$  will short to ground the outputs of the cross-coupled latch, in this way disabling the whole operation of the comparator. While the buffer preamplifier is only suitable for low to medium frequencies and 4bit resolution, the whole ADC takes only about  $600 \mu A$  of current at 3.3 V for a clock frequency of 33 MHz. As opposed to other proposed UWB-IR receiver structures (21), (72), (20) and (19) the ADC in the UWB-IR ED receiver is not the major power consumption component.

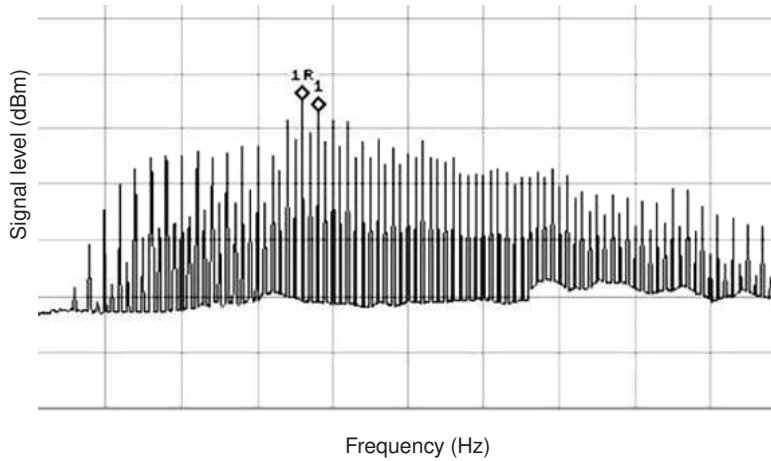
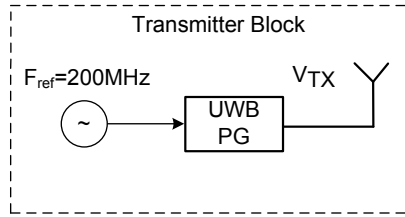


Since the ADC is sampling the analogue signal at the reference clock frequency, low power operation of the UWB-IR transceiver is feasible. All the remaining parts of the beacon detection section presented in (108) remain the same. The output of each integrator is connected to the input of the ADC for a Hold duration once every symbol period  $T_b$  ns. The digital output of the ADC is connected to the MAXSELADC section by a bank of switches synchronized with the Hold signals and the ADC clock signal.

The synchronization algorithms have been implemented in an FPGA using the Very High Speed Integrated Circuits Hardware Description Language (VHDL) language. The FPGA family used for implementation is a Xilinx VIRTEX - 4<sup>TM</sup> device. VIRTEX - 4<sup>TM</sup> has a large number (448) of input/output ports, 24192 logic cells and 21504 slice registers with 4 input lookup tables (LUT).

## 5.6 Simulation and Measured Results

The testboard of the UWB-IR transceiver is presented in Figure 65. In Figure 68, the mapping between the integrated UWB-IR transceiver and the block diagram presented in Figure 33, is given. The RF transceiver is implemented in a 0.35  $\mu\text{m}$  BiCMOS process. The front-end section of the receiver has a maximum overall gain of 46 dB with the overall power consumption of 117 mW with a voltage supply of 3.3 V. The implementation photo of the digital baseband section into the FPGA is presented in Figure 68. The measured spectrum of a train of pulses triggered by an 200 MHz off-chip clock generator without randomising techniques is presented in Figure 49. The external clock signal generator is connected to the testbed by a coaxial cable. The starting point of the spectrum is set at 10 MHz while the ending point is set at 10 GHz.



1R: (-35 dBm) delta: (200 MHz 1)

1: (-34 dBm)

**Fig 49. Measured Spectrum at the Output of the UWB Transmitter (Without Scrambling Sequence Overlay) Shows 200 MHz Separation Between Spectral Lines.**

The maximum peak of the spectral lines is approximately  $-35$  dBm. In Figure 49, the measured spectrum at the output of the transmitter has been determined by the Agilent-PSA-E4446A<sup>TM</sup> spectrum analyzer. The test signal for the receiver section was generated by the pulse generator presented in Figure 49,

Table 9 presents the simulated power consumption of the UWB-IR transceiver circuits.

**Table 9. Simulated Power Consumption of 0.35  $\mu\text{m}$  BiCMOS UWB-IR Energy Detection Receiver Front-End.**

Block	Obtained value [mW]
LNA	20
VGA	10.56
Gilbert	3.96
Integrators block	80
ADC	1.98
Total power consumption	117

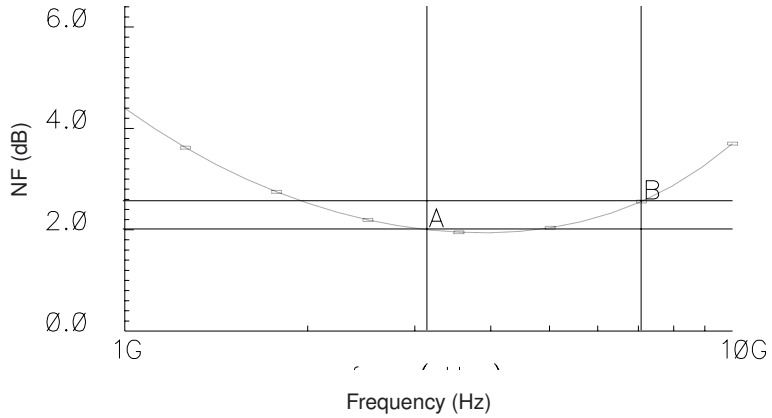
The power consumption of the LNA can be decreased by using a process with lower voltage supply value. The ADC has a power consumption of only 2 mW, because the preamplifier-comparator was especially designed for low power operation.

**Table 10. Simulated Parameters of the 0.35  $\mu\text{m}$  BiCMOS LNA.**

Parameter name	Value
Process	0.35 $\mu\text{m}$ BiCMOS
-3 dB Bandwidth	4 GHz
Current consumption	6 mA
Zin	50 $\Omega$
S11	-25 dB
S21	20 dB
NF	2.5 dB
Supply	3.3 V

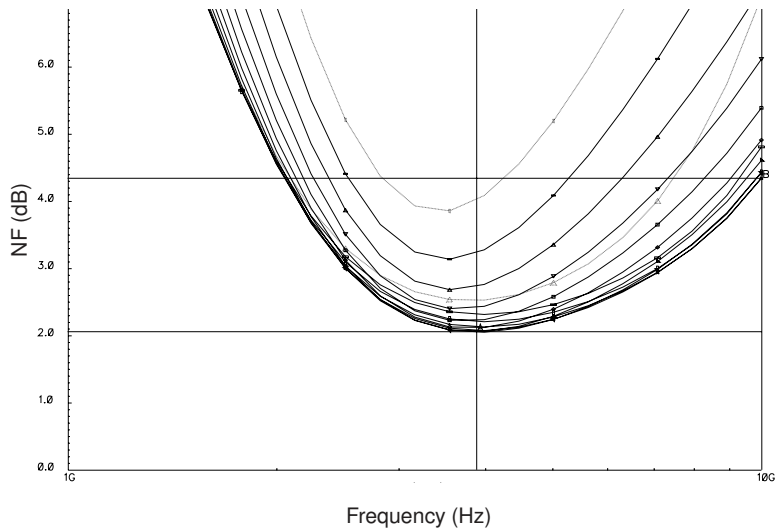
The simulated noise figure of the LNA is presented in Figure 50.

The simulated noise figure of the LNA versus bias current variation is presented in Figure 51. As expected, a higher current consumption will decrease the noise figure of the LNA.



A: (3.10 GHz 2.01) delta: (5.35 MHz 1.054)      B: (8.45 GHz 3.06) slope: 196.835p

**Fig 50. Simulated Noise Figure of the LNA.**

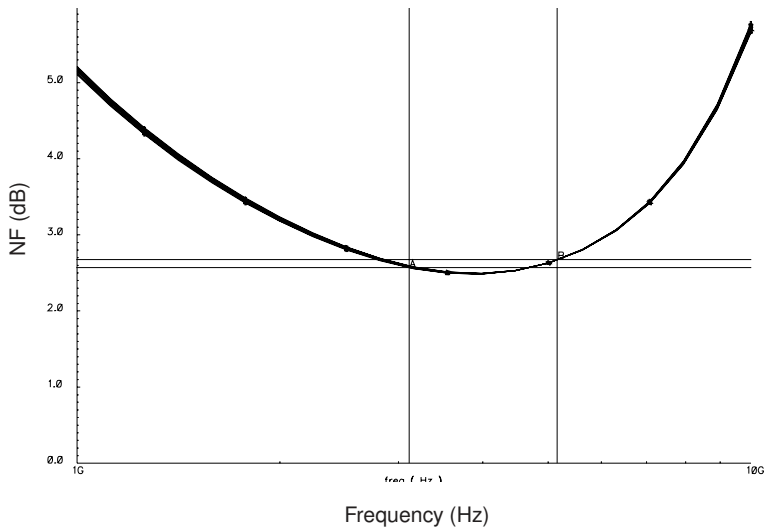


A: (3.88 GHz 2.06) delta: (6.11 GHz 2.28)      B: (10 GHz 4.34) slope: 374.422p

**Fig 51. Simulated Noise Figure of the LNA Versus Bias Current Variation for 400  $\mu$ A to 13 mA.**



The simulated noise figure of the LNA versus input pad capacitance  $C_{PAD}$  is presented in Figure 52. As expected, a lower value for the  $C_{PAD}$  will decrease the noise figure.



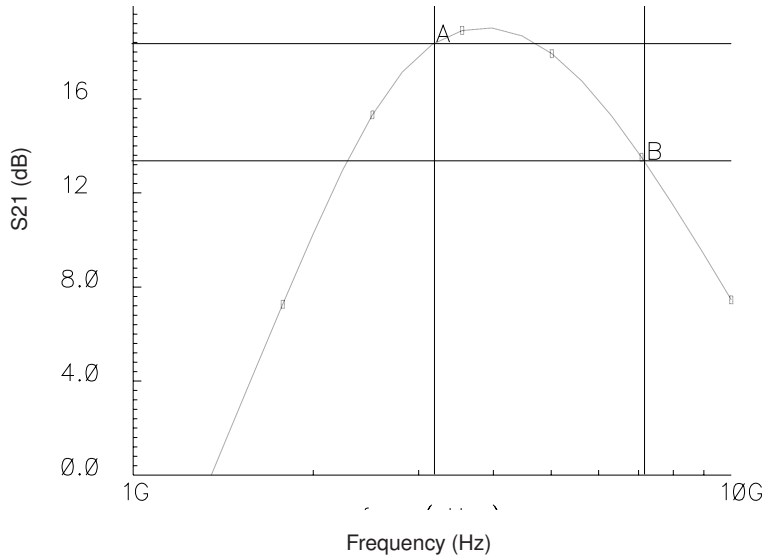
A: (3.10 GHz 2.57) delta: (2.04 GHz 100.165 m) B: (5.15 GHz 2.67) slope: 48.96 p

**Fig 52. Simulated Noise Figure of the LNA Versus Pad Capacitance  $C_{PAD}$ .**

Therefore, a lower noise figure can be obtained either by increasing the current consumption and by decreasing the  $C_{PAD}$ , or both. The lowest value for  $C_{PAD}$  is specified by the IC process. The maximum value of the current consumption is limited by the knee current density value specified in the IC process documentation. If the current density is higher than the knee value, the frequency performance characteristics of the transistors will degrade greatly. The noise figure of the LNA has a maximum of 3 dB and a minimum of 2 dB in the signal bandwidth. The  $S$  parameters of the LNA were validated by the Cadence SpectreRF<sup>TM</sup> noise simulator. The gain of 18 dB is attained with a consumed current level of 6 mA.

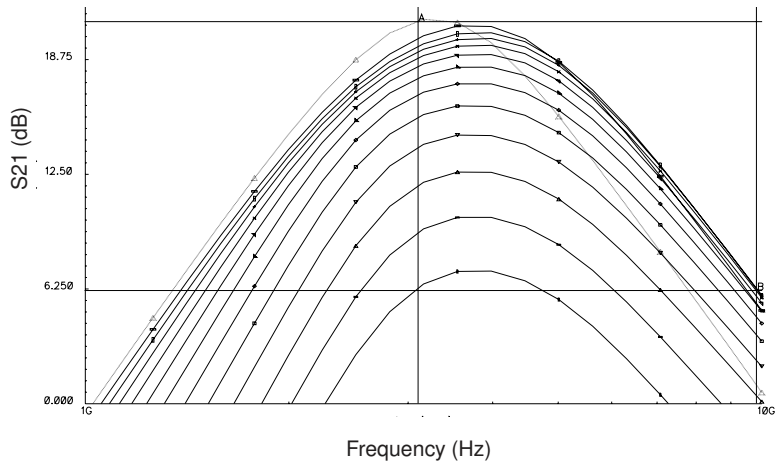
The  $S_{21}$  parameter variation depending on the bias current of the LNA is presented in Figure 54. The  $S_{11}$  parameter of the LNA is presented in Figure 55.

The  $S_{11}$  parameter variation depending on the bias current of the LNA is presented in Figure 56.



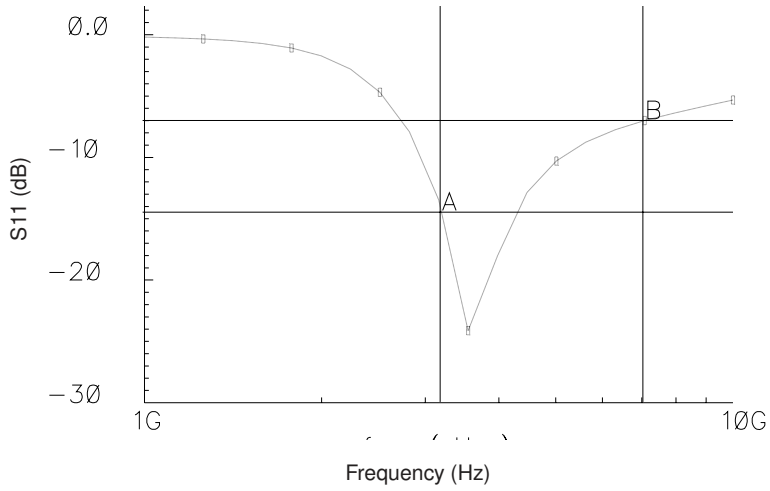
A: (3.19 GHz 18.371) delta: (3.95 GHz -5.02)      B: (7.15 GHz 13.34) slope: -1.26n

**Fig 53. Simulated S21 Parameter of the LNA.**



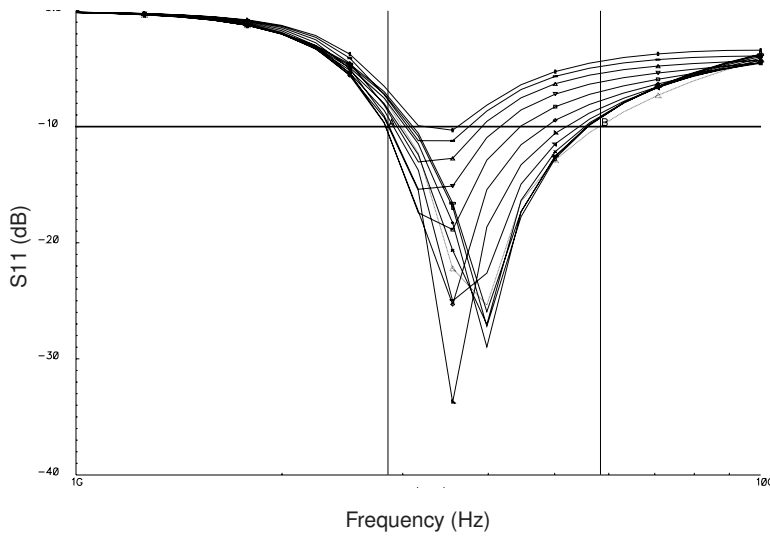
A: (3.10 GHz 20.83) delta: (6.70 GHz -14.671)      B: (9.81 GHz 6.16) slope: -2.188n

**Fig 54. Simulated S21 Variation Depending on the Bias Current Parameter of the LNA.**



A: (3.19 GHz -14.43) delta: (3.85 GHz 7.41)      B: (7.05 GHz -7.02) slope: 1.92n

**Fig 55. Simulated S11 Parameter of the LNA.**



A: (2.85 GHz -9.98) delta: (2.97 GHz 31.637)      B: (5.82 GHz -9.95) slope: 10.652p

**Fig 56. Simulated S11 Parameter Variation Depending on the Bias Current of the LNA.**

The bias current takes value in the 400  $\mu$ A to 13 mA range.

A comparison with the state-of-the-art reported wideband amplifiers is presented in Figure 11. The LNA presented in (58) has the lower power consumption due to its lower supply voltage of only 0.9 V. Therefore, the current consumption of the LNA presented in this work is 10 mA. The supply voltage of the LNA is 3.3 V while the current consumption is 6mA. Therefore, by using a process with a lower supply voltage, the LNA we have presented will provide a lower power consumption. When compared with the LNA presented in (45), the ED receiver’s LNA provides a lower noise figure and a lower power consumption, while forward gain is only 3 dB lower. Among all the LNAs designed in a BiCMOS technology (76), (45) and (56), our LNA has the lowest noise figure.

A WCDMA direct conversion receiver with 5 MHz bandwidth has been presented in (78). The power consumption of the RF front-end section of the WCDMA receiver presented in (78) is 41 mA from a 2.7 V supply. The direct conversion receiver reported in (78), provides a sensitivity of -114 dBm for 128 kbps data at 4.096 Mcps spreading rate. The front-end receiver section published in (78) consumes three times more current and shows a sensitivity which is 60 dBm higher than the UWB-IR receiver front-end section designed in this thesis.

**Table 11. Comparison Between the State-of-the-Art CMOS and BiCMOS Wideband Amplifiers.**

S21 (dB)	Power (mW)	Technology	Reference	NF (dB)
3.3	13	9.6	BiCMOS	(76)
4	9.2	9	CMOS	(18)
2.8	12	24	BiCMOS	(56)
2.5	21	30	BiCMOS	(45)
2	13.5	9	CMOS	(58) <sup>a</sup>
2.5	18	20	BiCMOS	(105) <sup>b</sup>

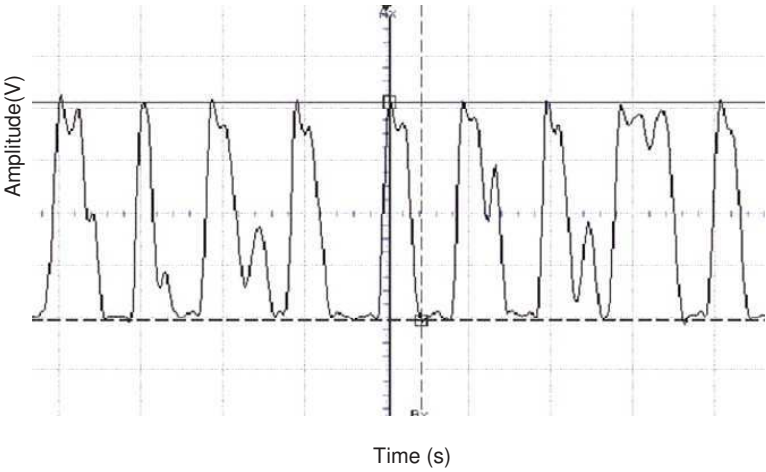
<sup>a</sup>simulated

<sup>b</sup>simulated

The S11 of the designed LNA in the signal band is at least -20 dB which confirms good impedance matching. The 1 dB compression point of the LNA is -3 dBm with the maximum input signal of approximately 250 mV. This is actually sufficient to ensure

the linearity and dynamic range of the amplifier as long as the waveform of the signal does not become distorted. The 1 dB compression point of the VGA is lower than that of the LNA with the maximum input signal of approximately 120 mV. This is however acceptable, since the maximum input signal level of the LNA is very low. With the LNA gain of 18 dB, the maximum input signal level at the input of the VGA will not exceed tens of mV.

The receiver circuits are implemented on the UWB-IR transceiver chip in two different set-ups. The first set-up includes the VGA, the Gilbert square cell and the output buffer. The second receiver chain contains the VGA, the Gilbert square cell, a bank of 8 integrators and the ADC. In Figure 57, the measured amplified and squared pulses at the output of the Gilbert cell output buffer are presented.

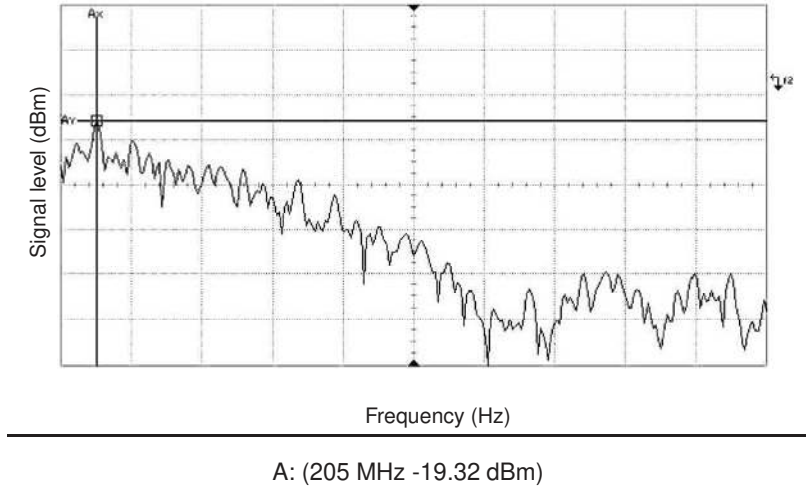


A: (182.1 ps 51.62 mV) delta: (1.93 ns 0)                      B: (2.11 ns -28.94 mV) slope: 0

**Fig 57. Measured Time Domain Waveforms After VGA Amplification and Squaring by the Gilbert Cell.**

In Figure 58, the measured spectrum at the output of the first receiver set-up is presented. The measured spectral power at the output of the receiver test section, has been determined by measuring the signal at the output of the testbed presented in Figure 65 with the HP - INFINIUM<sup>TM</sup> oscilloscope. The testbed was connected to the oscilloscope by a 50 Ω coaxial cable. The test signal at the input of the receiver test section was generated by the pulse generator presented in Figure 49. The HP - INFINIUM<sup>TM</sup>

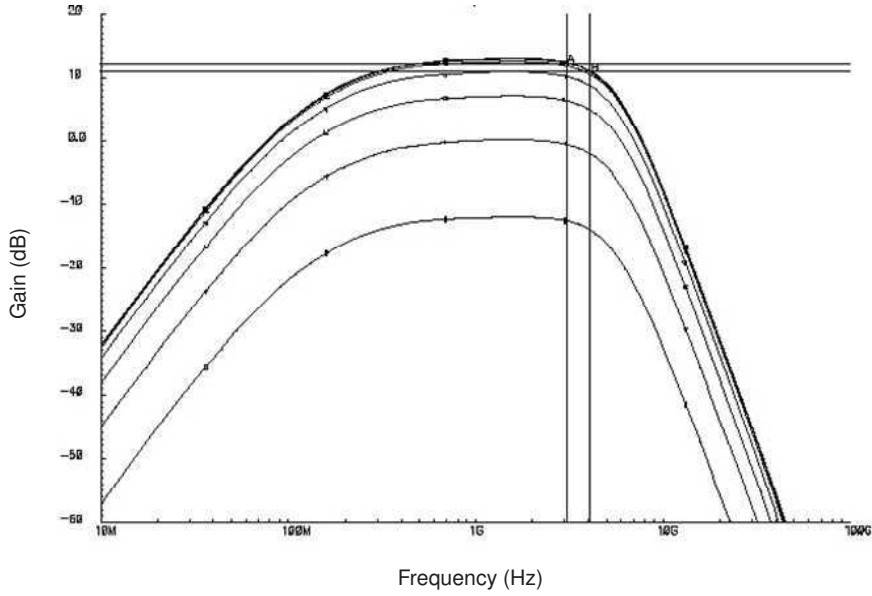
has a bandwidth of 1.5 GHz and samples the input signal at a rate of 8 Gsamples per second. The spectrum analyzer and the testbed have each been connected with the bow-tie antenna presented in Appendix II.



**Fig 58. Measured Spectrum of the Tested Receiver Front-End Section when VGA gain is set to 6 dB.**

The peak-to-peak voltage amplitude of the squared pulses is 83.3 mV which is a high enough signal to drive the integrators section.

The minimum detectable signal level at the input of the test section of the receiver was measured to be  $400 \mu\text{v}$  which is equivalent with a sensitivity level of -55 dBm. The variable gain amplifier response on different control voltages is shown in Figure 59. In Figure 59, the gain of the VGA versus its frequency is presented.



A: (3.10 GHz 12.42) delta: (998.43 MHz -1.44)      B: (4.09 GHz 10.97) slope: -1.44n

**Fig 59. Measured Gain vs. Control voltage of the VGA.**

After squaring, the signal is integrated by the bank of 8 integrators.

In Table 12, a comparison between the proposed transceiver and other UWB-IR transceivers presented in the open literature is presented.

**Table 12. Comparison Between Integrated UWB DS - SS, UWB Multiband Correlation based, UWB-IR Energy Detection Receivers and WCDMA Receivers.**

Process	Band	Data Rate	Power [mW]	Reference
0.18 $\mu\text{m}$ CMOS	3 - 5 GHz	200 Mbps	99@1.8 V	(140)
0.18 $\mu\text{m}$ CMOS	3.1 - 5 GHz	1 Gcps	385 @ 1.8 V	(44)
0.18 $\mu\text{m}$ CMOS	0 - 960 MHz	193 Kbps	280 @ 1.8 V	(20)
0.13 $\mu\text{m}$ CMOS	0 - 1 GHz	1 Mpulse/s	0.92 @ 1.1 V	(73) <sup>a</sup>
0.18 $\mu\text{m}$ CMOS	275 - 525 MHz	1 Mbps	1 @ 1.8 V	(116) <sup>b</sup>
0.35 $\mu\text{m}$ BiCMOS	5 MHz RF spacing@2 GHz	128 Kbps	110.7 @ 2.7 V	(78)
0.35 $\mu\text{m}$ BiCMOS	3.1 - 4.1 GHz	5 Mbps	140 @ 3.3 V	(105) <sup>c</sup>

<sup>a</sup>0.007 duty cycle

<sup>b</sup>simulated

<sup>c</sup>simulated

The UWB-IR transceiver presented in (140) was designed for interchip communications on a printed circuit board and not for wireless channels. Therefore, this transceiver can achieve data rates up to 200 Mbps while the current consumption of 50 mA is higher than the current consumption of 35 mA of the energy detection transceiver front-end. The UWB-IR transceiver presented in (44) operates in an wireless channel in the 3.1 - 5 GHz band while consuming 385 mW while using a voltage supply of 1.8 V. Therefore, the current consumption of this transceiver is much higher than the ED transceiver. The UWB-IR transceivers presented in (73), (116) and (20) are designed for the lower UWB band below 1 GHz. The power consumption of the transceiver presented in (116) is 1 mW because of the low duty cycle of 0.007% the transceiver is operating. The duty cycle of all the other transceivers presented in Table 12, is 100%. Therefore, this transceivers are not using power hungry RF stages to operate in the UWB band above 3.1 GHz. The voltage supply of these transceivers is also much lower than the supply value used in the design of the proposed energy detection transceiver. However, none of these transceivers include the baseband digital section which have been implemented on the FPGA. Among all the presented UWB receivers operating above 3.1 GHz, the energy detection transceiver has the lowest power consumption mainly due to the lower consumption of the LNA and ADC circuits.



### 5.6.1 Digital Baseband FPGA Simulation Results

Table 13 presents the area report after the place and route process with the Xilinx<sup>TM</sup> implementation tool. The largest number of resources taken by the digital baseband, are the IOs with 429 input-outputs used. This is because the digital baseband circuits have been implemented for maximum testability, which requires a great deal of IOs. The number of IOs used could be reduced at the expense of less testability. The area occupied by the digital baseband take much less of the of core area of the VIRTEX - 4<sup>TM</sup> device resources. Therefore, only 55% of slices are used and only 30% of total DFFs or latches are used. The total equivalent gate count for the design is 128752. The area of the digital baseband section is expected to be smaller by a factor of 10, when integrated into a digital IC.

**Table 13. Area Report After Place&Route of the Baseband Block Implemented in VIRTEX - 4<sup>TM</sup> Device.**

Resource	Used	Available	Utilization
IOs	429	448	95 %
Slice registers	6511	21504	30 %
4 input LUTa	11224	21504	52 %
Occupied slices	6013	10752	55 %

The timing report after place-and-route process, shows a maximum supported clock frequency of 223.3 MHz, while the lowest frequency path is rated at 117.49 MHz. After the place and route phase, the estimated power consumption of the digital baseband section is 450 mW. The total simulated power consumption of the whole transceiver is presented in Table 14.

**Table 14. Total Simulated Power Consumption of the 0.35  $\mu\text{m}$  BiCMOS Energy Detection Transceiver.**

Block	Value
Transmitter	20 mW
Receiver Front-End	117 mW
Baseband (FPGA)	450 mW
Total	587 mW

## 5.7 Conclusions

In this Chapter, the implementation of several blocks of the UWB-IR non-coherent energy collection receiver has been presented. The RF front-end receiver is implemented in a 0.35  $\mu\text{m}$  BiCMOS process. The receiver front-end chain implemented has a maximum overall gain of 46 dB with the overall power consumption of 117 mW with a voltage supply of 3.3 V. An LNA with a noise figure of 2 dB, a forward gain of 18 dB in a 3.1 - 5 GHz bandwidth was designed in a 0.35  $\mu\text{m}$  BiCMOS process. The current consumption of the LNA is only 6 mA using a voltage supply of 3.3 V. The ladder filter was used to transform the single-frequency reactive matching circuit used in a low-noise amplifier into a wideband circuit.

Using the same IC process, a lower noise figure can be obtained at the expense of a higher consumption or by using a lower capacitance value of the input pad  $C_{PAD}$ . Using an IC process which has transistors with higher  $f_T$ , the noise figure will improve. A systematic way of optimizing the parameters of the LNA was presented. Among all the BiCMOS compared LNAs, the LNA of the energy detection receiver has the lowest noise figure and a low current consumption.

The VGA has a maximum gain of 15 dB for 3.2 mA current consumption. The structure of the VGA is based on that of the Gilbert cell and occupies a lower die area. The squaring of the pulses is implemented with a classical Gilbert cell. The measured spectral power at the receiver output has been determined by measuring the signal at the output of the testbed presented in Figure 65 with the HP - INFINIUM<sup>TM</sup> oscilloscope. The receiver front-end is simplified when compared with correlation receiver, since there is no need for a LO or intermediate frequency downconversion stages. A systematic methodology was presented to optimize the frequency performance of the

OTA.

The input capacitive load of the ADC is kept low by using a relatively low number of comparators due to the low 4-bit resolution. The power consumption of the ADC is low due to the low sampling speeds and low power consumption of the latched based comparator. All the circuit blocks (RF + Analogue + Baseband) of the UWB-IR energy detection receiver operating above 3.1 GHz have been presented. The total simulated power consumption of the transceiver is 587 mW.

A thoroughly comparison with other receiver structures presented in the open literature has been presented. Based on the published results, the energy detection transceiver architecture has the lowest power consumption while operating in the UWB band above 3.1 GHz. This is largely because of the LNA low power consumption, simple energy collection scheme and low sampling speeds of the ADC. By using lower supply processes and low duty cycle operation, the power consumption of the transceiver is expected to be reduced even further.



## 6 Conclusions and future work

UWB systems offer unique advantages compared to existing RF systems. First, UWB allows unlicensed usage of an extremely wideband spectrum. The underlay spectrum approach increases spectral efficiency and paves the way for new wireless applications. UWB enables the design of adaptive transceivers which can optimize system performance as a function of the required data rate, range and power. UWB offers the possibility to trade data rates and range for power consumption. UWB signals offer high temporal resolution which results in low fading margins and therefore offers increased robustness against multipath. Due to the large number of resolvable paths many distinct multipath components are available at the receiver. Rake and non-coherent receivers can collect the energy of the multipath components, and hence improve performance. UWB-IR transceivers do not require up or down conversion stages which reduces the implementation complexity and the cost of the devices.

The signal properties of UWB means it has applications from wireless communications to localization and radar. The wireless communication application includes wireless sensor networks, wireless personal area networks, wireless telemetry, and telemedicine. UWB-IR ranging applications is a major breakthrough in sensor networks owing to its extremely high spectral accuracy and low cost. The ranging network can be viewed as a sensor network where the physical parameter to be sensed is location. The ultra wide bandwidth and hence the wide variety of material penetration capabilities allows UWB to be used for radar imaging, including ground penetration radars, wall radar imaging, through-wall radar imaging and surveillance systems.

Impulse radio based UWB transceivers are implementable in both CMOS and BiCMOS processes. The implementation of several transmitters and receivers architectures have been presented in the open literature, while other architectures, like transmitted reference and auto-correlation, are still in the evaluation phase.

### 6.1 Conclusions

UWB impulse radio non-coherent receivers and Gaussian transmitters were studied in this thesis. At the time of writing there was no other example of a complete implementation of a UWB-IR ED non-coherent receiver architecture. UWB-IR systems are

simple to implement because carrier modulation is not required, there is no need for an RF power amplifier and are robust in multipath fading. It was shown that the UWB-IR Gaussian transmitter has a low complexity of implementation and meets the specifications of the FCC indoor spectral mask, while consuming only 20mW when operating at 100 % duty cycle. The energy detection receiver has been chosen for a low complexity of implementation while still providing reasonable performance against other non-coherent receivers. It was shown that TR-BPAM and ED-BPPM structures provide identical performance. It was shown that the implementation complexity of the UWB-IR non-coherent receivers is greatly reduced compared with Rake receivers. The low complexity of implementation of the energy detection receiver arises from the simple synchronization scheme and low sampling rates. The drawback of the non-coherent approach is noise enhancement due to the squaring and the degradation in time resolution, which is proportional with the length of the integration time window. It was shown that when compared with other UWB-IR receivers, the power consumption of the energy detection receiver is not dominated by the power consumption of the ADC, which greatly improves the overall energy efficiency.

In this thesis we have presented the circuit design of a Gaussian monocycle pulse generator and an UWB-IR non-coherent energy detection receiver. The front-end receiver is implemented in a 0.35  $\mu\text{m}$  BiCMOS AMS process, while the transmitter is implemented in a 0.35  $\mu\text{m}$  CMOS process. The front-end chain has an overall gain of 46 dB with the overall power consumption of 117 mW and a voltage supply of 3.3 V. The active die area of the UWB transceiver is 2.65 mm<sup>2</sup>.

The LNA has a noise figure of 2 dB and a forward gain of 18 dB in the 3.1 - 5 GHz bandwidth. In order to transform the single-frequency reactive matching circuit used in a low-noise amplifier into a wideband circuit, a ladder filter was used. Compared with other published BiCMOS LNAs, the designed LNA has the lowest noise figure and one of the lowest values of current consumption. The energy collection process is based on a bank of 8 integrators and a digital timing section. The integrator structure is based on an OTA which integrates its output current on a capacitor. The OTA structure is differential which eliminates the common mode signal from being integrated. The current consumption of the OTA can be reduced at the expense of reduced output signal swing at its output. The power consumption of the ADC is low due to the low sampling speeds and low power consumption of the latch based comparator. The digital baseband section implemented on an FPGA includes the bit synchronization, preamble detection and the slot synchronization.

The simulated results have been validated by the Cadence SpectreRF<sup>TM</sup> and XILINX<sup>TM</sup> simulators. The measured results have been obtained by using the testbed presented in Figure 65, the Agilent-PSA-E4446A<sup>TM</sup> spectrum analyzer, the HP - INFINIUM<sup>TM</sup> oscilloscope and the bow-tie antenna presented in Appendix II. The UWB-IR energy detection transceiver has been designed in a low cost BiCMOS process. The power consumption of the energy detection transceiver is 587 mW, being the lowest power consumption among the other UWB-IR transceiver structures presented. In order to increase the effective range of communication, the sensitivity level of the receiver could be improved to be about -70 dBm. The UWB-IR Gaussian pulse generator can be modified to transmit any derivative of the Gaussian pulse. A variable clock multiplication factor will enable the generation of variable pulse repetition frequencies for the Gaussian pulse generator.

## 6.2 Future Research Directions

The main areas of future research includes power consumption, integration, low noise receiver components and reconfigurable receiver architectures.

The power consumption of the integrated UWB-IR transceivers can be decreased by using lower supply voltages and minimizing the parasitic capacitances. Unfortunately, lower power consumption must be traded-off with lower ranges and increased noise in the front-end receivers amplifiers. The power consumption of the full transceiver is expected to reduce by integrating the digital synchronization section on-chip. This is because the number of gates which implements the baseband section on an ASIC is much lower than on an FPGA.

As the UWB spectrum limits vary in different countries, the transmitter design must be adjusted accordingly. UWB standardization has been finalized in the US but the regulatory bodies from Europe and Japan will soon launch different spectral emission masks. This will lead to a need for more work on UWB pulse design and new transceivers architectures.

Operating at even higher ranges will require the transmitter to operate at the maximum allowed transmitted power, while the receiver will be required to operate in lower  $E_b/N_0$  regions. Further improvements of the transmitter includes the possibility of transmitting different pulse shapes and to modify the pulse amplitude and pulse width depending on the UWB regulations available in various countries. Employing pulse shaping, the transmitter would have the possibility to avoid transmitting the UWB sig-

nal over the frequencies of possible strong narrowband interferers. Transmitting different pulse shapes would be possible by replicating the digital delay stages and the cross-coupled differential pairs from the transmitter we have proposed in this thesis.

In order to combat narrowband interference, notch filtering before the pulse correlation could be used. However, this method requires a number of narrowband analogue filter banks, since the frequency and power of the narrowband interferers can vary. Therefore, employing analogue filtering adds complexity, cost and size to UWB receivers. Recent developments in the area of micro-electro-mechanical systems (MEMS) filters will add more flexibility to the receiver front-end because only one tuned filter could filter the varying interferers. Nowadays, integrated MEMS tunable RF filters still have a large insertion loss in the order of 6 - 7 dB, but in future the loss is expected to reduce.

Some of the most important areas to be addressed in future research on UWB-IR transceivers are the design of circuit blocks and the development of more complex receivers structures without increasing the power consumption. The receiver's performance could be improved by utilizing LNA circuit circuits with a lower noise figure and higher gain. Since the LNA is the first component of the integrated transceiver, its own noise figure will have the highest impact on the overall noise figure of the receiver. A lower noise figure of the receiver front-end will increase the SNR for the detection process. The energy detection process could be improved by utilizing digital timing circuits with variable timing for the control signals. Low sampling speeds coupled with lower resolution ADCs will also add to the possibility of designing low power consumption UWB-IR transceivers. However, by designing low noise LNAs and variable timing circuits, the receiver's implementation complexity and power consumption will also increase. One future research direction would be to investigate modalities of increasing the receiver's data rate at low voltage supply levels.

The latest developments of IC technologies will enable integration of the RF, analogue and digital sections on the same die and an increase of the receiver performance. Integrating the RF front-end of the receiver and digital synchronization section on the same die is a challenging task, since the switching noise generated by the digital part can disturb the sensitive receiver analogue components. One possible solution would be to manufacture two dies into the same package: one for the digital circuits, and one for the analogue circuits.

Further improvement of UWB-IR receiver architectures would be possible by employing additional a-priori information regarding the channel and noise characteristics. Future research should also focus on coherent receivers, by weighting the integrator in-



put with a function dependent on the channel power delay profile, which can be seen as partial channel-state information. As a downside of this approach, the implementation complexity will increase due to the estimation of this partial channel-state information. Since most of the channel estimation will be implemented in the digital domain, the highly complex estimation process will take advantage of the scaling of digital processes, leading to lower cost of implementation in terms of die area and power consumption.

The measured bit error rate and dynamic range performance of the energy detection receiver needs to be determined in future research work. Fully digital implementation of an UWB-IR receiver structures will be based on sampling the incoming pulses with discrete time-to-digital converters where discrete steps of 1 ps have already been presented. Fully digital implementations of analogue receivers will be realized in the near future to achieve design flexibility and maximally deliver processing capability of digital processors.

Another important issue to be considered for a fully integrated solution of the UWB-IR energy detection transceiver is System-on-a-chip (SoC). In this case, all the digital, analogue, mixed-signal and RF functions would be integrated into one single chip, which leads to a lower total die area and thus, to a low cost of implementation. The 1.8 V supply SoC implementation, could reduce the power consumption of the baseband section by at least 30% to 50%. However, testing and debugging a complex SoC is not a trivial task.

The power consumption of the transceiver can be reduced even further by using IC processes with low supply voltages, by integrating on-chip the digital baseband section and by operating the transceiver at low duty cycles.

Performance evaluation in a real field test and with a single integrated circuit which implements the full UWB-IR energy detection transceiver, would be a significant step forward towards the final goal - the integrated software radio based UWB- IR transceiver.



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# Appendix 1 Antennas

UWB-IR systems occupy large bandwidths, typically of a few gigahertz. Within the operating bandwidths, UWB antennas should have stable response in terms of impedance matching, gain, radiation patterns and polarization. Other important UWB antenna requirements include: small size, low cost and easy integration with other RF circuits.

## 1.1 Theoretical Antennas

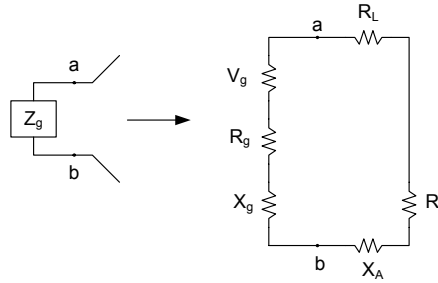
An antenna can be considered to be ultra-wideband if the upper frequency is at least six times greater than the lower frequency of the band (74). The bandwidth of an antenna is defined as the range of frequencies within which the performance of the antenna, with respect to some characteristic, conforms to a specified standard (13). When a short time pulse excites an antenna, the radiated signal will demonstrate a ringing effect, and the signal is no longer impulse like.

The impedance of the antenna  $Z_A$  at terminals  $a$  and  $b$  can be defined as (13):

$$Z_A = R_A + jX_A, \quad (62)$$

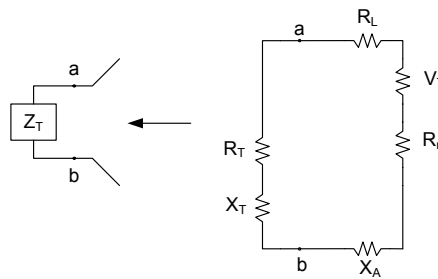
where  $R_A$  is the antenna resistance at terminals  $a$  and  $b$  and  $X_A$  is the antenna reactance between same terminals. The antenna resistance  $R_A = R_r + R_L$ , where  $R_r$  is the radiation resistance and  $R_L$  is the loss resistance of the antenna,

When the antenna is connected to a generator  $Z_g = R_g + jX_g$ , where  $R_g$  is the resistance of the generator impedance and  $X_g$  is the reactance of the generator impedance, the transmitting antenna and its Thevenin equivalent can be represented as shown in Figure 60 (13).



**Fig 60. Transmitting Antenna and Thevenin Equivalent.**

When the antenna is connected to a load  $Z_T = R_T + jX_T$ , where  $R_T$  is the resistance of the load impedance and  $X_T$  is the reactance of the load impedance, the receiving antenna and its Thevenin equivalent can be represented as shown in Figure 61 (13).



**Fig 61. Receiving Antenna and Thevenin Equivalent.**

To combat ringing, resistive antennas with low quality factors  $Q$  should be employed, as the resistive loading will attenuate the unwanted ringing signal. The antenna bandwidth increases as  $Q$  decreases because the antenna bandwidth is inversely proportional to  $Q$ . The quality factor of an antenna is described by (74):

$$Q = \frac{f_c}{f_h - f_l}, \quad (63)$$

where  $f_c$ ,  $f_h$  and  $f_l$  are the centre frequency and the upper and lower 3 dB frequency values of the antenna respectively.

The main difference between UWB and narrowband antennas is that while the latter are resonant elements tuned to a particular centre frequency and therefore have narrow



bandwidths, the UWB antennas have much broader bandwidth and do not require resonating operation.

## 1.2 UWB Antennas

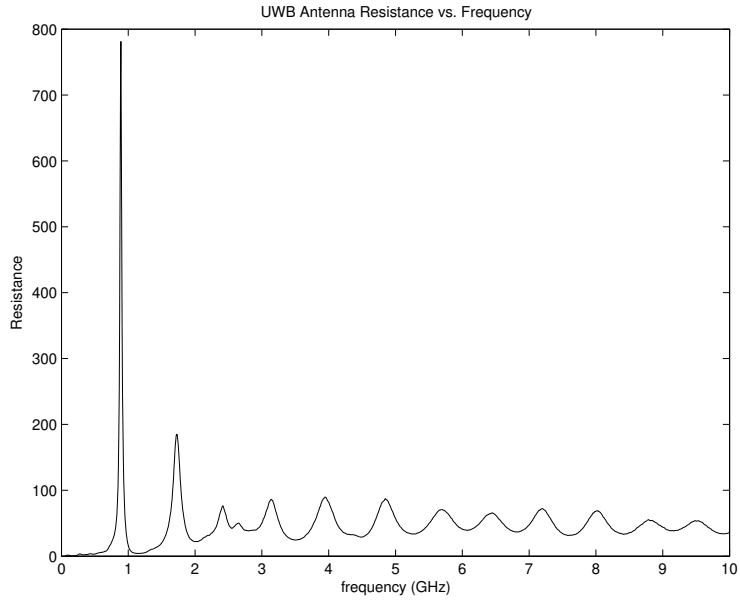
For UWB-IR systems there are three ways to shape the spectra of radiated signals. The first is to select the source pulses with spectrum shaping conforming to the emission limit mask. The second is to use RF filters to shape the spectrum of radiated signals. The third is to make use of the filtering function of the transmitting antenna (24).

In this section, several UWB portable antennas will be presented. The transmitted waveform will be differentiated when passing through the antenna. The antenna gain should be constant across the frequency band such that dispersion of the transmitted pulse is avoided (74). UWB antennas have been proposed following common designs such as the TEM horn, folded-horn antenna, biconical antenna or bowtie antenna.

The TEM horn is built with two tapered metal planes fed by a two-wire TEM-mode transmission line. TEM horn preserves very well the pulse shape and has a gain of 5 to 15 dB. The length of the TEM horn can be adjusted to modify the impedance matching, the radiation pattern and the transient behaviour of the antenna.

A folded-horn antenna is built by inserting sub-horns into a main horn (74). The main advantage of this is the reduced size of the antenna.

We have used a bow-tie antenna for our receiver testing since it is inexpensive, is small in size, has stable response in terms of impedance and is easy to integrate with the RF circuits. An inexpensive antenna will enable use in large numbers in WSN applications. A small size antenna enables the use of the integrated UWB-IR transceiver together with the antenna in mobile applications. A stable response is highly desirable since it will affect the amplitude of the transmitted pulse and the input reflection coefficient of the LNA. For smaller values than  $50 \Omega$ , lower amplitude pulses will be transmitted. When the antenna impedance is not equal with that of the LNA, the input reflection coefficient ( $S_{11}$ ) will degrade, increasing the signal loss at the input of the receiver.



**Fig 62. UWB Bow-tie Antenna Impedance.**

The beam width and input impedance of a bow-tie antenna depend directly on the antenna geometry, and they are nearly constant over the desired frequency range. The impedance of the antenna in the bandwidth of interest is approximately  $50 \Omega$ . In Figure 62, the antenna resistance in the DC - 10 GHz bandwidth is presented (79).

## Appendix 2 S parameters

Single and multi port networks enable the analysis of both passive and active circuits, irrespective of their complicated and often non-linear behaviour, by using simple input-output relations without the need to know the internal structure of the system (63). The scattering ( $S$ ) parameters are used when practical system characterizations can not be accomplished through open-circuit or short-circuit assumptions, as is the case with low-frequency applications. At high frequencies the short-circuit realized with a wire will show an inductance of substantial magnitude, while an open-circuit will provide a capacitive loading.

$S$  parameters have been used in this thesis as a basis of comparing receiver circuits in Section 3.4 and to characterize the performance of the LNA in Chapter 6.

A two-port network with four terminals and two ports are used to define the input and output of a circuit, as shown in Figure 63. Two terminals define a port if the current flowing into one terminal is the same as the current flowing out of the other terminal. At each port there are two variables (voltage and current), one of which will be independent, while the other will be dependent on the two-port network and the independent variables. At low frequencies, two common representations are the impedance matrix ( $Z$  parameters) and the admittance matrix ( $Y$  matrix).  $Z$  parameters and  $Y$  parameters are useful at low frequencies because they can be measured by applying either a test current or voltage to the input port and connecting the output port as a short or open circuit, depending on the definition. However, at RF frequencies,  $Z$  and  $Y$  parameters become very difficult to measure due to the need for broadband short and open circuits. Furthermore, an active two-port network might oscillate if one of its ports are short or open circuited. Thus, a different representation of the two-port network is needed at RF frequencies.

The representation that is used is the scattering, or  $S$ , parameters. Instead of relying on ports being open and short circuited,  $S$  parameters have the advantage that they can be measured by matching the source and the load impedance to the reference impedance. The normalized incident and reflected voltage waves  $a_i$  and  $b_i$  are related to the terminal voltage and currents at port  $i$  by equations (64) and (65), respectively:

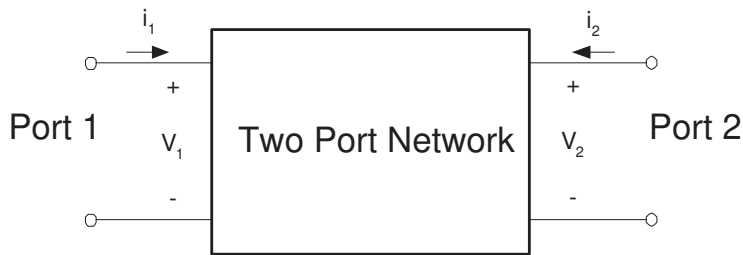
$$a_i = \frac{v_i + Z_o i_i}{2\sqrt{Z_o}}, \quad (64)$$

$$b_i = \frac{v_i - Z_o i_i}{2\sqrt{Z_o}}, \quad (65)$$

where  $Z_o$  is the reference impedance, usually real and equal to  $50\Omega$ . For the network shown in Figure 64, the contributions from the two ports can be combined to form the equation:

$$\begin{Bmatrix} b_1 \\ b_2 \end{Bmatrix} = \begin{Bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{Bmatrix} \begin{Bmatrix} a_1 \\ a_2 \end{Bmatrix}, \quad (66)$$

where  $S_{11}$ ,  $S_{12}$ ,  $S_{21}$ ,  $S_{22}$  are the scattering parameters measured across ports 1 and 2.



**Fig 63. Two-port Network Diagram.**

Scattering parameters are defined in equations (67), (68), (69), (70), (63):

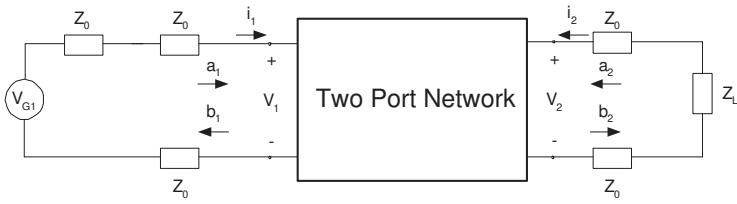
$$S_{11} = \frac{b_1}{a_1} \Big|_{a_2=0}, \quad (67)$$

$$S_{21} = \frac{b_2}{a_1} \Big|_{a_2=0}, \quad (68)$$

$$S_{22} = \frac{b_2}{a_2} \Big|_{a_1=0}, \quad (69)$$

$$S_{12} = \frac{b_1}{a_2} \Big|_{a_1=0}. \quad (70)$$

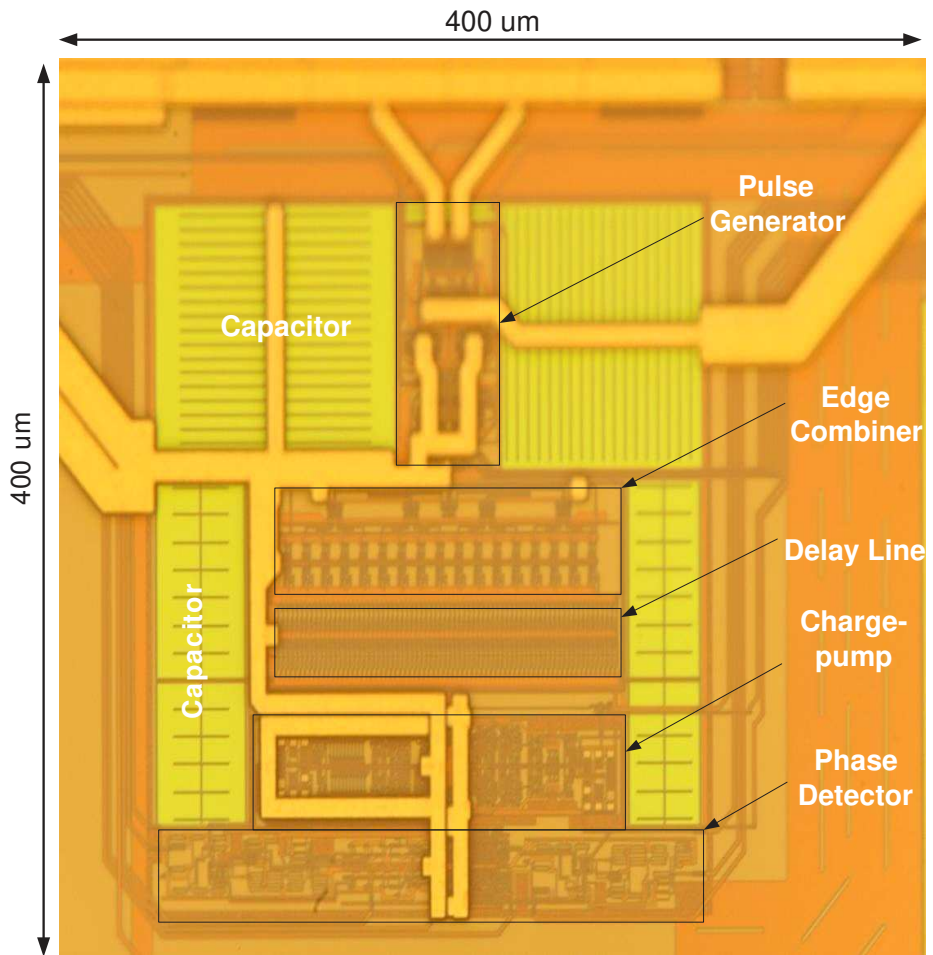
The condition for a port being properly terminated is that its load impedance must match the characteristic impedance  $Z_o$ . The output or input impedance of the two-port network does not have to match the characteristic impedance  $Z_o$ .



**Fig 64. S Parameter Representation of a Two-port Network.**







**Fig 66. Die Photo of the UWB-IR Gaussian Transmitter Designed in a  $0.35 \mu\text{m}$  CMOS process from AMS.**



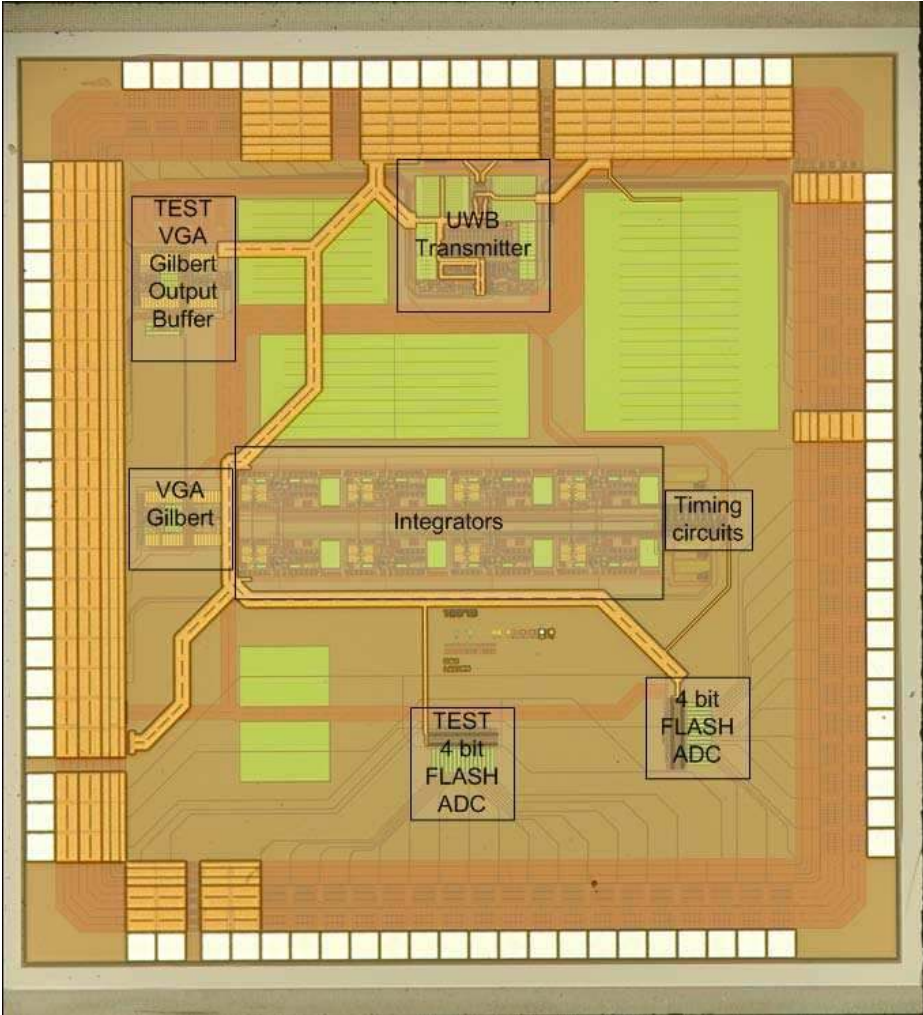
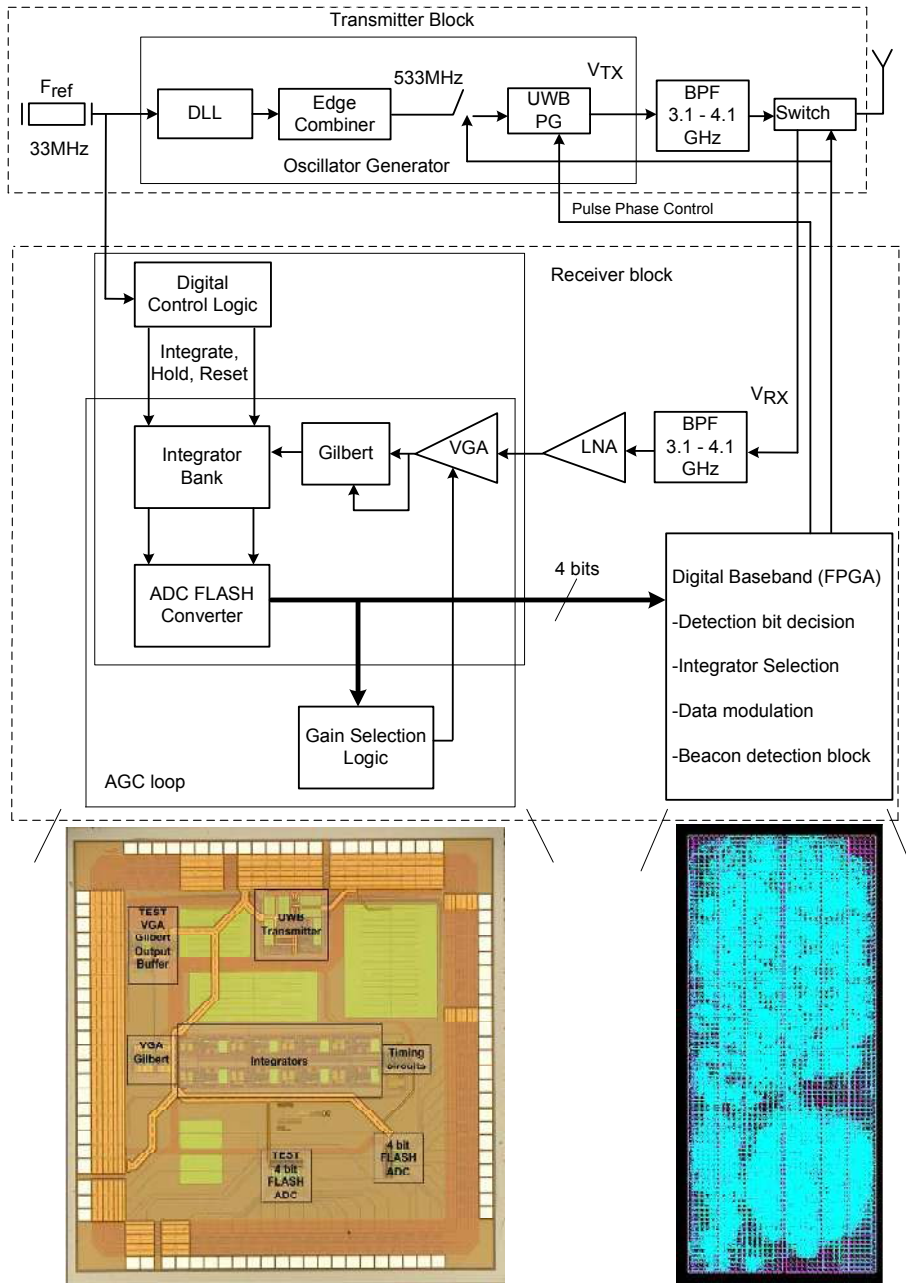


Fig 67. Die Photo of the IC UWB-IR Energy Detection Transceiver Designed in a 0.35  $\mu\text{m}$  BiCMOS process from AMS.



**Fig 68. Mapping of the Designed UWB-IR Energy Detection Transceiver to the IC and VIRTEX - 4<sup>TM</sup> Device.**

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