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# Non-Isolated High Step-Up DC/DC Converter with coupled inductor and switched capacitor

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**ABSTRACT** In this paper, a high-efficiency DC/DC converter with low voltage stress is designed for green power applications. The proposed non-isolated high step-up DC/DC converter combines the advantages of switched capacitors, coupling inductors, and voltage multiplier techniques. Adding the cells of the switched capacitor not only increases the voltage gain but reduces the voltage stress of the semiconductor devices. High voltage gain can be achieved by adding a coupled inductor method to adjust the turns ratio. When these are combined with a voltage multiplier circuit, the leakage energy of the coupled inductor is recirculated to the output terminal with lossless passive clamping performance. The leakage inductance of the coupled inductor controls the current dropping rate of the output diode turn OFF so that the reverse-recovery problem is mitigated. The proposed converter integrates these three techniques to achieve high voltage gain without operating at maximum duty cycle. In addition, switching loss reduction is realized through zero current switching turn ON soft switching performance with low voltage stress of semiconductor devices. Finally, this paper verifies the performance of the proposed converter for theoretical analysis by using a 35~45V input, 380V output, and 1kW power prototype circuit.

**INDEX TERMS** Boost converter, high step-up, coupled inductor, switched capacitor, voltage multiplier cell.

## I. INTRODUCTION

Recently, renewable energy sources are increasing in value worldwide due to energy shortage, environmental pollution, and climate change. High step-up converters are essential because renewable energy sources are photovoltaics, wind power, and fuel cell systems, which have low-voltage output characteristics [1]–[4]. Among renewable energy systems, photovoltaic systems are expected to play an important role in future energy production [5], [6]. The output voltage of most PV panels is lower than 50V, and a full-bridge inverter requires about 380V DC bus voltage to deliver energy to a single-phase 220V utility grid for grid-connected generation systems. High step-up DC/DC converters with voltage gains of more than ten times in the front-end stage are essential [7]. When multiple PV panels have a parallel connection configuration, these high step-up converters are expected to have a significant benefit in reducing system cost and increasing power density, along with greater voltage conversion rates and higher efficiencies. Fig. 1 shows a typical green power conversion system block diagram using renewable and alternative power sources. It consists of a green power supply with a 380~400V DC bus application for high step-up DC/DC conversion of low-voltage level renewable energy sources to a Load/DC-Microgrid or Load/Utility using a DC/AC inverter [8].

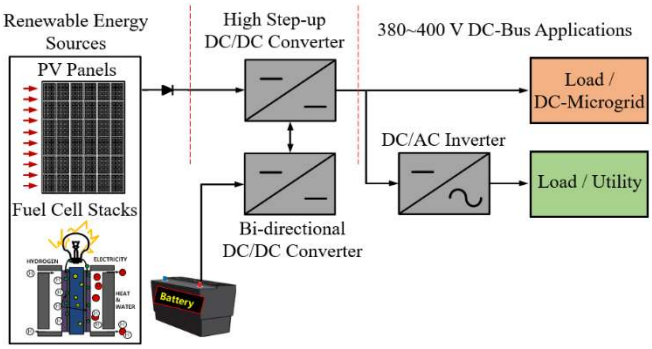


**FIGURE 1. Diagram of typical green power conversion system.**

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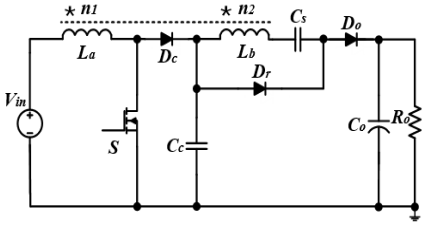
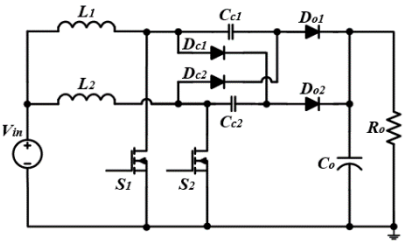
For DC/DC converters, high step-up is classified into two types: isolated and non-isolated. Isolated converters such as flyback, forward, push pull, half bridge, and full bridge can achieve high voltage gain by adjusting the transformer turns ratio [9], [10]. However, in addition to price increases, transformers also cause high switching voltages and significant losses due to transformer leakage inductance. For example, a flyback converter achieves high step-up voltage gain by adjusting the transformer turns ratio, but the primary side active switch and secondary side diode suffer from high voltage stress due to the leakage inductance of the transformer. This limits the use of flyback converters in high power applications. To solve this problem, an RCD snubber is used for reduction of the voltage stress on the switch. However, this method reduces efficiency [11], [12].

Non-isolated converters include buck, boost, and buck boost converters, which offer low cost, small size, low switching losses, and high efficiency [13]. Theoretically, a conventional boost converter can achieve a gain as high as ten times when the duty cycle is 0.9. However, in practice, the parasitic resistance of the inductor and the loss of the switch and the diode have the problem of reducing the output voltage as well as the efficiency [14]. Conventional boost converters operate under hard switching conditions of the switch and output diode. In particular, the output diode cannot achieve high efficiency because it causes serious reverse recovery problems. In order to solve the above-mentioned problems, various studies have been conducted in the literature [15]–[18].

Typically, a boost converter with a coupled inductor is divided into a cascaded boost converter in which the primary and secondary windings are connected in series and a stacked boost converter in which the secondary windings are stacked on the output side. These boost converters are similar to the principle of operation of flyback converters, the structure of the system is thin and the cost is low. They have high voltage gain and low voltage stress on the switch, and the leakage inductance of the coupled inductor helps to improve efficiency by mitigating the reverse recovery problem of the rectifier diode. However, the leakage inductance of a coupled inductor can cause severe resonances and high voltage spikes across switches and diodes. The higher the turns ratio, the larger the input current ripple. These high input current ripples not only increase conduction losses and lifetime, but can also have a detrimental effect on renewable energy devices. [19], [20].




(a)




(b)

**FIGURE 2. High step-up technology based on conventional boost converter. (a) High step-up converter with voltage multiplier circuit (VMC). (b) High step-up interleaved converter with inductors and switched capacitors.**

The high step-up conversion problem can be solved by combining switched capacitors, switched inductors, coupled inductors, switched coupled inductors, and switched diode capacitors with conventional boost converters [21]–[24]. The voltage multiplier circuit (VMC) combines a set of inductors, diodes, and capacitors to achieve the low voltage stress and zero current switching (ZCS) conditions of the main switch and diode, greatly reducing power loss and increasing efficiency [25]. Fig. 2 (a) is a high step-up converter of a VMC with coupled inductor and switched capacitor [26]. By using a clamp circuit, the voltage stress of the switch *S* can be reduced and the energy stored in the leakage inductance of the coupled inductor can be recycled. Fig. 2 (b) can increase the power level and voltage gain by combining a switched capacitor with an interleaved structure [27]. However, high efficiency cannot be obtained because the voltage stress of the switch is equal to the output voltage and operates in a hard-switching condition. Also, the power density cannot be improved due to the size of the capacitor bank. Recently, it has attracted attention in various applications through hybrid switched capacitor converters, which use both capacitors and inductors in voltage conversion and power transmission processes to improve the energy utilization of capacitors [28]–[30].

In this paper, a high step-up DC/DC converter is proposed by integrating coupled inductors, switched capacitor cells, and voltage multiplier circuits into a conventional interleaved boost converter. Coupled inductors increase the voltage gain by adjusting the turns ratio of the primary and secondary, and switched capacitor cells provide additional voltage gain. Switched capacitor cells and voltage multiplier circuits of the proposed converter can achieve low voltage stress on switches and diodes. These can increase the efficiency by using a semiconductor element with low conductivity. The lossless clamp performance of the VMC will not only allow the switch to operate as ZCS soft switching through the leakage inductance of the coupled inductor, but also alleviate the reverse recovery problem of the output diode.

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## II. OPERATION MODE OF PROPOSED CONVERTER

Fig. 3 shows a proposed high step-up converter circuit that combines switched capacitors, coupled inductors, and VMC technologies. The inductances $L_{a1}$ and $L_{a2}$ of the primary winding of the coupled inductors $L_1$ and $L_2$ are connected in parallel, and the inductances $L_{b1}$ and $L_{b2}$ of the secondary winding are connected in series. Fig. 4 depicts the equivalent circuit of the proposed converter. It is possible to adjust the high step-up gain by the turns ratio ($N$) of the primary side winding and the secondary side winding, and the two winding direction is divided into "•" and "*".

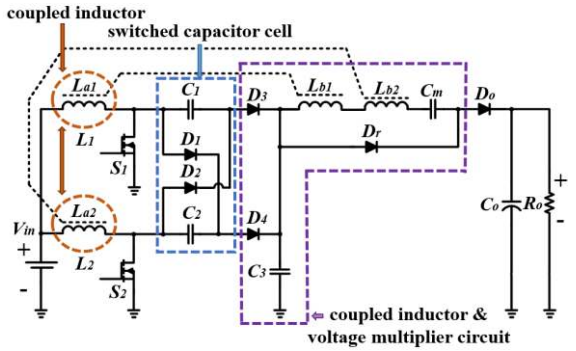


**FIGURE 3.** Proposed converter.

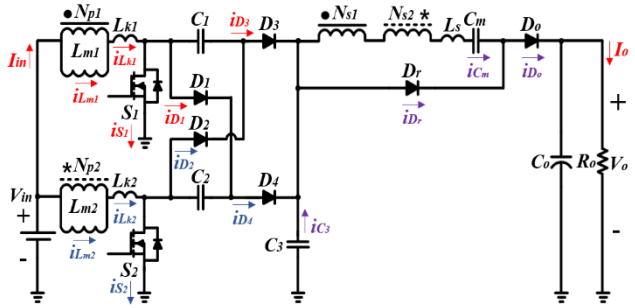


**FIGURE 4.** Equivalent circuit of proposed converter.

### A. CIRCUIT DESCRIPTION IN CCM OPERATION

The steady state operation of the proposed converter [CCM] consists of eight modes and Fig. 5 illustrates the theoretical key waveforms. Fig. 6 shows the operating modes for the steady state.

1) Mode 1 [$t_0$ - $t_1$]

At $t = t_0$, Mode 1 starts and it is shown in Fig. 6 (a). The switches $S_1$ and $S_2$ are ON and the diodes $D_1$, $D_2$, $D_3$, $D_4$, $D_r$, and $D_o$ are reverse biased. The diodes $D_1$ and $D_2$ are reverse biased due to the voltage difference between the capacitors $C_1$ and $C_2$. The diodes $D_3$ and $D_4$ are reverse biased due to the voltage difference between the capacitor $C_3$ and $C_1$ or $C_2$. Further, the diode $D_r$ is reverse biased by the voltage of the capacitor $C_m$ and the diode $D_o$ is reverse biased by the voltages of the capacitors $C_o$, $C_m$, and $C_3$. In this mode, the magnetizing inductances $L_{m1}$ and $L_{m2}$ as well as the leakage inductances $L_{k1}$ and $L_{k2}$ are charged by the input voltage $V_{in}$, which can be written as

$$i_{Lm1}(t) = I_{Lm1}(t_0) + \frac{V_{in}}{L_{m1} + L_{k1}}(t - t_0), \quad (1)$$

$$i_{Lm2}(t) = I_{Lm2}(t_0) + \frac{V_{in}}{L_{m2} + L_{k2}}(t - t_0). \quad (2)$$

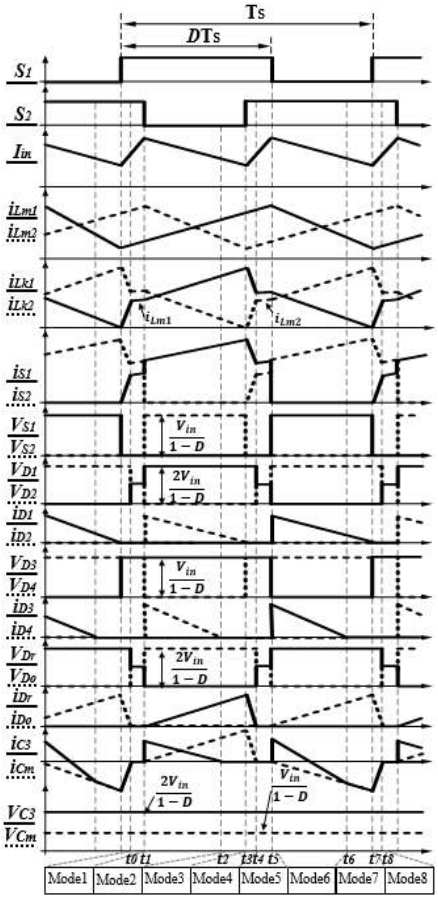


**FIGURE 5.** Key waveforms of proposed converter [CCM].

2) Mode 2 [$t_1$ - $t_2$]

At $t = t_1$, the switch $S_1$ is ON and the switch $S_2$ is turned OFF. The diodes $D_1$, $D_3$, and $D_o$ maintain a reverse bias state as shown in Fig. 6 (b). The energy stored in the magnetizing inductance $L_{m2}$ is transferred to the primary and secondary sides by coupled inductors. The energy stored in the magnetizing inductance is transferred to the primary and secondary sides by coupled inductors. The primary side of the coupled inductor transfers energy to capacitors $C_1$ and $C_3$ by forming $N_{p2}$–$D_2$–$C_1$ and $N_{p2}$–$C_2$–$D_4$–$C_3$ loops. In addition, the secondary side of the coupled inductor transfers energy to the capacitor $C_m$ by forming $N_{s2}$–$N_{s1}$–$D_r$–$C_m$ loop. The diode $D_1$ is reverse biased with the voltage of capacitor $C_3$, and diode $D_3$ and switch $S_2$ are applied with the voltage difference between capacitors $C_3$ and $C_2$. In this state, mode operation can use the following equations

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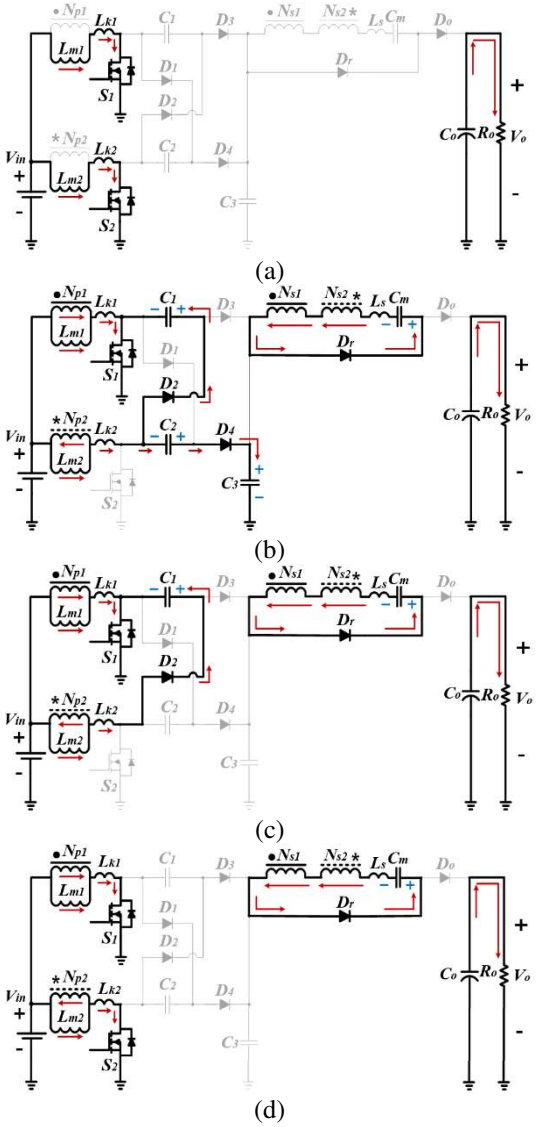
$$i_{D2}(t) = I_{D2}(t_1) - \frac{NV_{C1} - V_{Cm}}{N^2(L_{k1} + L_{k2})}(t - t_1), \quad (3)$$

$$i_{D4}(t) = I_{D4}(t_1) - \frac{N(V_{C3} - V_{C2}) - V_{Cm}}{N^2(L_{k1} + L_{k2})}(t - t_1), \quad (4)$$

$$i_{Dr}(t) = i_{Ls}(t) = i_{Cm}(t) = \frac{N(V_{C1} + V_{C3} - V_{C2}) - 2V_{Cm}}{N^2(L_{k1} + L_{k2})}(t - t_1), \quad (5)$$

$$\begin{aligned} i_{S1}(t) &= i_{Lm1}(t) + i_{D2}(t) + Ni_{Dr}(t) \\ &= I_{Lm1}(t_1) + I_{D2}(t_1) - \frac{NV_{C1} - V_{Cm}}{N^2(L_{k1} + L_{k2})}(t - t_1) \\ &\quad + \frac{N(V_{C1} + V_{C3} - V_{C2}) - 2V_{Cm}}{N(L_{k1} + L_{k2})}(t - t_1) \end{aligned} \quad . \quad (6)$$



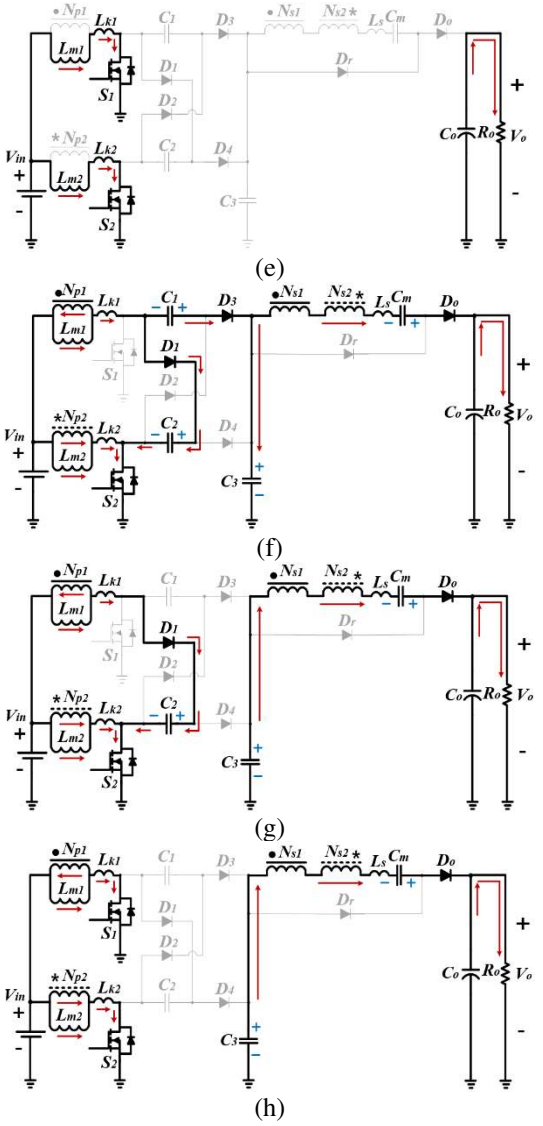




**FIGURE 6. Operating modes of proposed converter [CCM]. (a) Mode 1 [$t_0 - t_1$]. (b) Mode 2 [$t_1 - t_2$]. (c) Mode 3 [$t_2 - t_3$]. (d) Mode 4 [$t_3 - t_4$]. (e) Mode 5 [$t_4 - t_5$]. (f) Mode 6 [$t_5 - t_6$]. (g) Mode 7 [$t_6 - t_7$]. (h) Mode 8 [$t_7 - t_8$].**

3) Mode 3 [$t_2$ - $t_3$]

At $t = t_2$, the current ($i_{D4}$) of the diode $D_4$ is linearly reduced to zero by the leakage inductance $L_{k2}$ and the diode $D_4$ is turned OFF. Therefore, there is no reverse recovery problem of the diode $D_4$. The operating mode in this mode is shown in Fig. 6 (c). In this mode, all switches and diodes except diode $D_4$ retain their previous state and the current flow can be written by

$$i_{Dr}(t) = i_{Ls}(t) = i_{Cm}(t) = I_{Dr}(t_2) + \frac{NV_{C1} - V_{Cm}}{N^2(L_{k1} + L_{k2})}(t - t_2), \quad (7)$$

$$i_{S1}(t) = i_{Lm1}(t) + i_{D2}(t) + Ni_{Dr}(t), \quad (8)$$

$$i_{Lk1}(t) = i_{Lm1}(t) + Ni_{Dr}(t), \quad (9)$$

$$i_{Lk2}(t) = i_{Lm2}(t) - Ni_{Dr}(t). \quad (10)$$

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4) Mode 4 [$t_3$ - $t_4$]

At $t = t_3$, the switch $S_1$ remains ON and switch $S_2$ starts to turn ON. The diode $D_2$ is also reverse biased as shown in Fig. 6 (d). The current ($i_{Lk2}$) flowing through the primary side leakage inductance $L_{k2}$ linearly increases, but the current ($i_{Lk1}$) flowing through the primary side leakage inductance $L_{k1}$ linearly decreases. Therefore, the current ($i_{S2}$) of the switch $S_2$ is linearly increased through the leakage inductance energy to the primary side of the coupled inductor. The diode $D_r$ is ZCS turned OFF and which can mitigate the reverse recovery problem of the diode. In this state, mode operation can use the following equations

$$i_{Dr}(t) = i_{Cm}(t) = i_{Ls}(t) = I_{Dr}(t_3) - \frac{V_{Cm}}{N^2(L_{k1}+L_{k2})}(t-t_3). \quad (11)$$

5) Mode 5 [$t_4$ - $t_5$]

At $t = t_4$, the switches $S_1$ and $S_2$ are ON and all diodes are reverse biased. This mode is shown in Fig. 6(e) and the operation of Mode 1 is repeated.

6) Mode 6 [$t_5$ - $t_6$]

At $t = t_5$, the switch $S_1$ is ON and the switch $S_2$ is turned OFF. The diodes $D_1$, $D_3$, and $D_o$ maintain a reverse bias state as shown in Fig. 6 (f). The energy stored in the magnetizing inductance $L_{m1}$ is transferred to the primary and secondary sides by coupled inductors. The primary side of the coupled inductor transfers energy to capacitors $C_2$ and $C_3$ by forming $N_{p1}$–$D_1$–$C_2$ and $N_{p1}$–$C_1$–$D_3$–$C_3$ loops. The diode $D_2$ is reverse biased with the voltage of capacitor $C_3$ and the diode $D_4$ and switch $S_1$ are applied with the voltage difference between capacitors $C_3$ and $C_1$. The diode $D_r$ is reverse biased due to the voltage difference between the capacitors $C_o$ and $C_3$. The equation in this mode can be obtained as

$$i_{D1}(t) = I_{D1}(t_5) - \frac{V_{C1}+V_{C2}-V_{C3}}{N^2(L_{k1}+L_{k2})}(t-t_5), \quad (12)$$

$$i_{D3}(t) = I_{D3}(t_5) - \frac{NV_{C2}+V_{C3}+V_{Cm}-V_o}{N^2(L_{k1}+L_{k2})}(t-t_5), \quad (13)$$

$$i_{Do}(t) = -i_{Ls}(t) = -i_{Cm}(t) = \frac{(N+1)V_{C2}+V_{C1}+V_{Cm}-V_o}{N^2(L_{k1}+L_{k2})}(t-t_5), \quad (14)$$

$$i_{Lk2}(t) = i_{Lm2}(t) + Ni_{Do}(t), \quad (15)$$

$$i_{S2}(t) = i_{Lm2}(t) + Ni_{Do}(t) + i_{D1}(t). \quad (16)$$

7) Mode 7 [$t_6$ - $t_7$]

In the case of $t = t_6$, the current ($i_{D3}$) of the diode $D_3$ decreases linearly to zero by the leakage inductance $L_{k1}$. Therefore, the diode $D_3$ is turned OFF to ZCS, so there is no reverse recovery problem. The energy stored in the magnetizing inductance $L_{m1}$ is transferred to the output side by forming a $C_3$–$N_{s1}$–$N_{s2}$–$C_m$–$C_o$ loop through the secondary side of the coupled inductor. The operating mode of this mode is shown in Fig. 6 (g) and the current flow can be written as

$$i_{Do}(t) = -i_{Ls}(t) = -i_{Cm}(t) = I_{Do}(t_6) + \frac{V_{Cm}+NV_{C2}+V_{C3}-V_o}{N^2(L_{k1}+L_{k2})}(t-t_6), \quad (17)$$

$$i_{D1}(t) = I_{D1}(t_6) - \frac{V_{Cm}+NV_{C2}+V_{C3}-V_o}{N^2(L_{k1}+L_{k2})}(t-t_6), \quad (18)$$

$$i_{Lk2}(t) = i_{Lm2}(t) + Ni_{Do}(t), \quad (19)$$

$$i_{S2}(t) = i_{Lk2}(t) + i_{D1}(t) + Ni_{Do}(t). \quad (20)$$

8) Mode 8 [$t_7$ - $t_8$]

At $t = t_7$, the switch $S_1$ is turned ON and the mode operation is shown in Fig. 6 (h). In the previous mode, the current of diode $D_1$ is ZCS turned OFF by linearly decreasing the leakage inductance current ($i_{Lk1}$) of the couple inductor. In this mode, the current of the switch $S_1$ increases linearly by the primary leakage inductance ($i_{Lk1}$) of the coupled inductor. Also, the diode current ($i_{Do}$) through the linear reduction of the leakage inductance current ($i_{Ls}$) is limited and the ZCS is turned OFF. Therefore, the problem of reverse-recovery of the diode can be alleviated. The proposed converter can reduce the problem of switch loss and diode reverse recovery, and this mode is given as

$$i_{Do}(t) = -i_{Ls}(t) = -i_{Cm}(t) = I_{Do}(t_7) + \frac{V_{Cm}+V_{C3}-V_o}{N^2(L_{k1}+L_{k2})}(t-t_7). \quad (21)$$

### B. CIRCUIT DESCRIPTION IN DCM OPERATION

The steady state operation of the proposed converter [DCM] consists of eight modes and Fig. 7 illustrates the theoretical key wave forms. Fig. 8 shows the operating modes. In this mode, Mode 1 [$t_0 - t_1$], Mode 2 [$t_1 - t_2$], Mode 5 [$t_4 - t_5$], and Mode 6 [$t_5 - t_6$] are similar to [CCM]. Therefore, only four operating modes of [DCM] were discussed.

1) Mode 3 [$t_2$ - $t_3$]

At $t = t_2$, the leakage inductance current ($i_{Lk1}$) of the coupled inductor decreases to zero, and the diodes $D_1$ and $D_2$ turn OFF naturally. The operating mode is shown in Fig. 8 (a). The current of the magnetizing inductance ($i_{Lm2}$) decreases linearly and the secondary side of the coupled inductor maintains the $N_{s2}$–$N_{s1}$–$D_r$–$C_m$ loop. Also, the current of the switch $S_1$ and the leakage inductance $L_{k1}$ is equal to the summation of the currents of the magnetizing inductances $L_{m1}$ and $L_{m2}$. This mode is similar to Mode 7 [$t_6 - t_7$] in Fig. 8 (c) and the equation can be written as

$$i_{Dr}(t) = i_{Cm}(t) = \frac{i_{Lm2}}{N}(t), \quad (22)$$

$$i_{Lk2}(t) = i_{D2}(t) = i_{D4}(t) = 0. \quad (23)$$

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2) Mode 4 [$t_3 - t_4$]

At $t = t_3$, the mode starts when the magnetizing inductance current ($i_{Lm1}$) of coupled inductor is zero, as shown in Fig. 8 (b). The switch $S_1$ is OFF and all diodes are in reverse bias. This mode is similar to Mode 8 [$t_7 - t_8$] in Fig. 8 (d) and the equation can be written as

$$i_{Lm1}(t) = I_{Lm1}(t_3) + \frac{V_{in}}{L_{m1} + L_{k1}}(t - t_3). \tag{24}$$

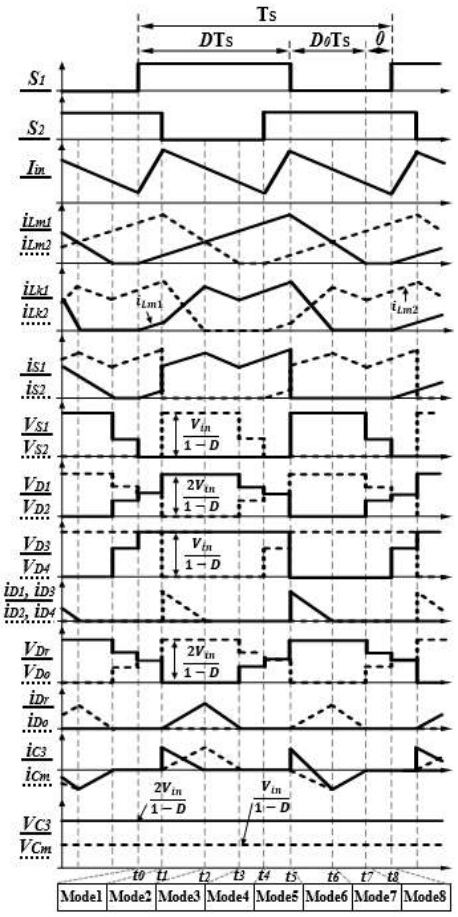
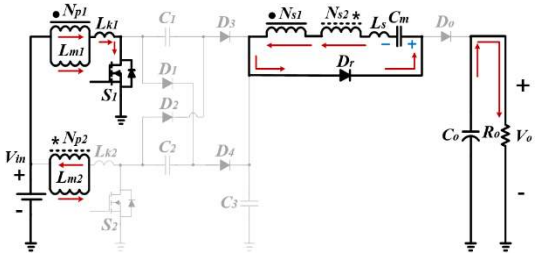
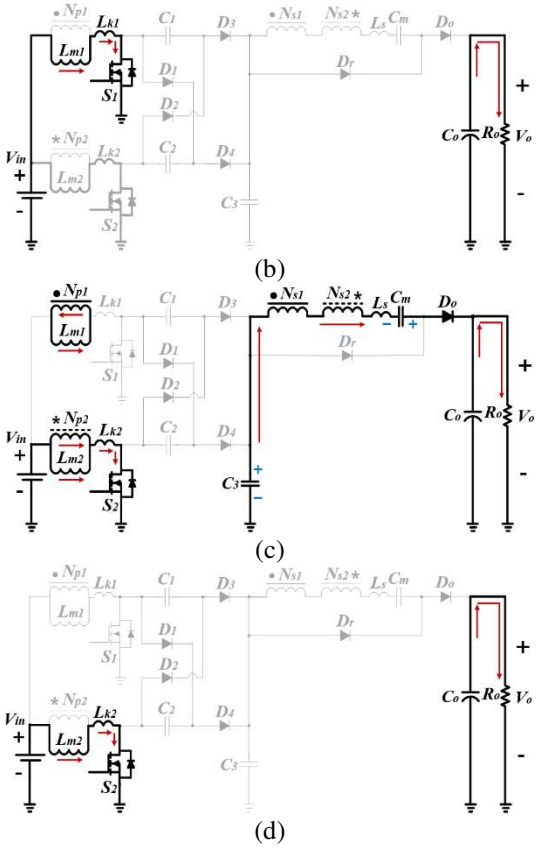



**FIGURE 7.** Key waveforms of proposed converter [DCM].



(a)



(b) (c) (d)

**FIGURE 8.** Operating modes of proposed converter [DCM]. (a) Mode 3 [$t_2$ - $t_3$]. (b) Mode 4 [$t_3$ - $t_4$]. (c) Mode 7 [$t_6$ - $t_7$]. (d) Mode 8 [$t_7$ - $t_8$].

## III. STEADY-STATE ANALYSIS OF PROPOSED CONVERTER

To simplify the circuit performance analysis of the proposed converter, the transient characteristics of the circuit are ignored. The turns ratio ($N$) of the coupled inductor is given by

$$N = \frac{N_s}{N_p}. \tag{25}$$

Also, the coupling coefficient ($k$) of the coupled inductor is defined

$$k = \frac{L_m}{L_m + L_k}. \tag{26}$$

### A. HIGH STEP-UP GAIN ANALYSIS

In the proposed converter [CCM] operation, two sections of ON (Mode 2=*II*) and OFF (Mode 6=*VI*) of the switch $S_1$ in Fig. 6 were selected to simplify the steady-state analysis. When switch $S_1$ is ON, Mode 2 can be written as

$$V_{Lk1}^{II} = \frac{L_{k1}}{L_{m1} + L_{k1}} V_{in} = (1 - k) V_{in}, \tag{27}$$

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$$V_{Np1}^{II} = \frac{L_{m1}}{L_{m1}+L_{k1}} V_{in} = kV_{in}\,, \tag{28}$$

$$V_{Ns1}^{II} = V_{Ns2}^{VI} = NkV_{in}\,. \tag{29}$$

Applying a voltage-second balance to the primary and secondary sides of a coupled inductor can be written as

$$\int_0^{DT_s} V_{Lk1}^{II} dt + \int_{DT_s}^{T_s} V_{Lk1}^{VI} dt = 0\,, \tag{30}$$

$$\int_0^{DT_s} V_{Np1}^{II} dt + \int_{DT_s}^{T_s} V_{Np1}^{VI} dt = 0\,, \tag{31}$$

$$\int_0^{DT_s} V_{Ns1}^{II} dt + \int_{DT_s}^{T_s} V_{Ns1}^{VI} dt = 0\,. \tag{32}$$

Substituting (27)–(29) into (30)–(32) can be written as

$$V_{Lk1}^{VI} = -\frac{D(1-k)}{1-D} V_{in}\,, \tag{33}$$

$$V_{Np1}^{VI} = -\frac{Dk}{1-D} V_{in}\,, \tag{34}$$

$$V_{Ns1}^{VI} = -\frac{NDk}{1-D} V_{in}\,. \tag{35}$$

The voltage of the clamp capacitor $C_1$ is equal to the voltage gain of the conventional boost converter given by

$$V_{C1} = V_{C2} = V_C = V_{in} - V_{Lk1}^{VI} - V_{Np1}^{VI} = \frac{1}{1-D} V_{in}\,. \tag{36}$$

The clamp capacitor $C_m$ is given by

$$V_{Cm} = V_{Ns2}^{VI} - V_{Ns1}^{VI} = \frac{kN}{1-D} V_{in}\,. \tag{37}$$

The power is delivered only when the switch $S_2$ is ON and the switch $S_1$ is OFF. The voltage gain ($M_{CCM}$) of the proposed converter can be derived as follows:

$$V_o = V_{in} - V_{Lk}^{VI} - V_{Np1}^{VI} + V_{C1} - V_{Ns1}^{VI} + V_{Ns2}^{VI} + V_{Cm} = \frac{2+2kN}{1-D} V_{in}\,, \tag{38}$$

$$M_{CCM} = \frac{V_o}{V_{in}} = \frac{2+2kN}{1-D}\,. \tag{39}$$

If the coupling coefficient ($k$) is equal to 1, it is given as

$$\therefore M_{CCM} = \frac{V_o}{V_{in}} = \frac{2+2N}{1-D}\,. \tag{40}$$

Fig. 9 illustrates the result of comparing the voltage gains according to the coupling coefficient ($k$=1, 0.9, 0.8) and the duty cycle ($D$) of the proposed converter. The proposed method can give a high voltage gain ($M_{CCM}$) by adjusting turns ratio ($N$). It should be noted that the proposed method gives a voltage gain ($M_{CCM}$) of ten times when the application ratio $D$ = (is equal to) 0.6 and the turns ratio $N$ = (is equal to) 1.

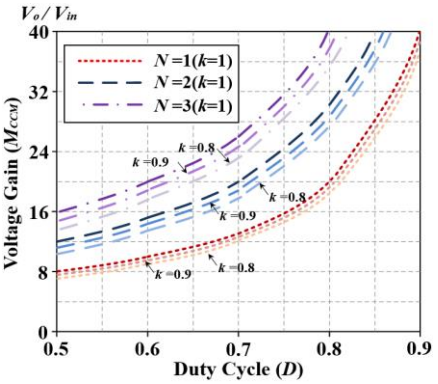


**FIGURE 9. Voltage gain comparison according to turns ratio and duty cycle.**

The DCM operation is similar to the CCM operation, and two sections of ON (Mode 2=*II*) and OFF (Mode 6=*VI*) of switch $S_1$ in Fig. 7 are selected. The coupling coefficient ($k$) is assumed to be 1 and applying the voltage-second balance principle, it can be written as

$$\int_0^{DT_s} V_{Np1}^{II} dt + \int_{DT_s}^{(D+D_0)T_s} V_{Np1}^{VI} dt + \int_{(D+D_0)T_s}^{T_s} V_{Np1}^{VIII} dt = 0\,, \tag{41}$$

$$\int_0^{DT_s} V_{Ns1}^{II} dt + \int_{DT_s}^{(D+D_0)T_s} V_{Ns1}^{VI} dt + \int_{(D+D_0)T_s}^{T_s} V_{Ns1}^{VIII} dt = 0\,. \tag{42}$$

In the DCM mode, the voltages of the clamp capacitors $C_1$, $C_m$, and $C_3$ are given as

$$V_{C1} = V_{C2} = \frac{D+D_0}{D_0} V_{in}\,, \tag{43}$$

$$V_{Cm} = N\left(\frac{D+D_0}{D_0}\right) V_{in}\,, \tag{44}$$

$$V_{C3} = 2\left(\frac{D+D_0}{D_0}\right) V_{in}\,. \tag{45}$$

The output voltage $V_o$ and the duty cycle $D_0$ can be expressed as

$$V_o = (2+2N)\left(\frac{D+D_0}{D_0}\right) V_{in}\,, \tag{46}$$

$$D_0 = \frac{2(1+N)DV_{in}}{V_o - 2(1+N)V_{in}}\,. \tag{47}$$

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Also, the time constant and maximum current value of the magnetizing inductance ($L_m$=$L_{m1}$=$L_{m2}$) are given as

$$\tau_{Lm} = \frac{Lm}{RT_s}, \tag{48}$$

$$I_{Lmp} = \frac{V_{in}}{L_m} DT_s . \tag{49}$$

In the steady state, the average current value of the capacitor is zero, which can be written as

$$\frac{1}{2} D_0 \frac{I_{Lmp}}{2+2N} - I_o = 0 . \tag{50}$$

As a result, from (40) and (47)–(50), the voltage gain ($M_{DCM}$) of the DCM and the boundary normalized time constant of the magnetized inductance are given as

$$M_{DCM} = \frac{V_o}{V_{in}} = 1 + N + \sqrt{(1+N)^2 + \frac{D^2}{\tau_{Lm}}}, \tag{51}$$

$$\tau_{Lm} = \frac{D^2}{\frac{2+2N}{1-D}\left(\frac{2+2N}{1-D} - 2(1+N)\right)} . \tag{52}$$

### B. VOLTAGE STRESS ANALYSIS OF POWER DEVICES [CCM]

The voltage stress applied to the switching devices of the proposed converter has to be minimized because it greatly affects the performance, price, and lifetime of the converter as a whole. According to the proposed converter Modes 2, 3, 6 and 7, the voltage stress of the switches $S_1$ and $S_2$ is equal to the voltages of the clamp capacitors $C_1$ and $C_2$, and it is given by

$$V_C = V_{S1} = V_{S2} = \frac{1}{1-D} V_{in} . \tag{53}$$

From (40) and (53), the relationship between the output voltage and the switch voltage can be obtained a

$$V_{S1} = V_{S2} = \frac{1}{2+2N} V_o . \tag{54}$$

which means that the voltage stress can be reduced by increasing the turns ratio ($N$).

Since the switch voltage is inversely proportional to ($2N$ + 2) in (54), the rated value of the switch voltage can be lowered by increasing the turns ratio ($N$). Therefore, it becomes possible for the proposed method to use a switching device with a low conduction resistance, which is advantageous in conduction loss and price reduction. Since the voltages of the diodes $D_1$ and $D_2$ are equal to the voltage of the capacitor $C_3$, the followings can be obtained

$$V_{D1} = V_{D2} = \frac{2}{1-D} V_{in} . \tag{55}$$

The voltages of the diodes $D_3$ and $D_4$ are the same as the voltages of the clamp capacitors $C_1$ and $C_2$ and the switch voltages $V_{S1}$ and $V_{S2}$. Therefore, the voltages of the diodes $D_1$, $D_2$, $D_3$, and $D_4$ are given by

$$V_{C3} = V_{D1} = V_{D2} = \frac{1}{1+N} V_o , \tag{56}$$

$$V_C = V_{D3} = V_{D4} = \frac{1}{2+2N} V_o . \tag{57}$$

From (56) and (57), it can be seen that the voltage of the diode $D_1$ or $D_2$ is half of the output voltage $V_o$ and the voltage of the diode $D_3$ or $D_4$ is a quarter of $V_o$ when the turns ratio ($N$) is 1, i.e. $N$=1. Therefore, by increasing the turns ratio ($N$), the diode voltage can be reduced and the voltage gain ($M_{CCM}$) can be increased. The voltage stresses of the diodes $D_r$ and $D_o$ are given by

$$V_{Dr} = V_{Do} = V_o - V_{C3} = \frac{N}{1+N} V_o . \tag{58}$$

The above equation (58) implies that the voltage of the diodes $D_r$ and $D_o$ becomes lower than the output voltage when the turns ratio ($N$) is increased. Fig. 10 depicts the relationship between the voltage applied to all semiconductor devices of the proposed converter and the turns ratio ($N$).

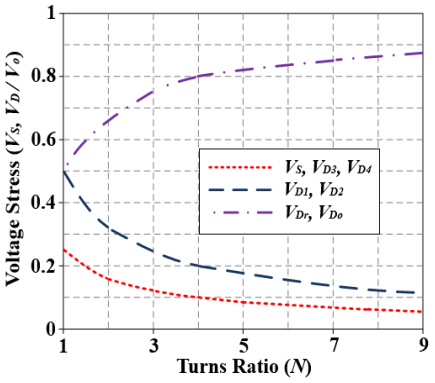


**FIGURE 10. Voltage stresses on semiconductor devices versus turns ratio.**

### C. CURRENT STRESS ANALYSIS OF POWER DEVICES

Summarizing the amp-second balance based on Modes 2 and in Fig. 6, it is possible to indicate the current magnitude of the semiconductor device (switch $S_1$ is ON and OFF). The diodes $D_2$, $D_4$, and $D_r$ operate during the period in which the switch $S_1$ is ON, and the average current is expressed as follows

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$$I_{D1} = I_{D2} \simeq I_{D3} = I_{D4} \simeq I_{Dr} = I_{Do} = \frac{1-D}{2+2N} I_{in} . \quad (59)$$

During the period in which the switch $S_1$ is turned OFF, the diodes $D_1$, $D_3$, and $D_o$ operate and the average current is given by

$$I_{D1} = I_{D2} \simeq I_{D3} = I_{D4} \simeq I_{Dr} = I_{Do} = \frac{2}{1-D} I_o . \quad (60)$$

The average current of switches $S_1$ and $S_2$ is expressed by

$$\begin{aligned} I_{S1} = I_{S2} &= I_{Lm1} + I_{D2} + NI_{Dr} = I_{Lm2} + NI_{Do} + I_{D1} \\ &= \frac{1}{2} I_{in} + \frac{1-D}{2+2N} I_{in} + N \frac{1-D}{2+2N} I_{in} \\ &= \frac{(2-D)(1+N)}{2+2N} I_{in} = \frac{(2-D)(1+N)}{1-D} I_o \end{aligned} . \quad (61)$$

Also, the peak currents of switches $S_1$ and $S_2$ can be written by

$$\begin{aligned} I_{S1} = I_{S2} &= I_{Lm1} + I_{D2} + NI_{Dr} = I_{Lm2} + NI_{Do} + I_{D1} \\ &= \frac{1+N}{1-D} I_o + \frac{DV_{in}}{2L_m} T_s + \frac{2}{1-D} I_o + N \frac{2}{1-D} I_o \\ &= \frac{3+3N}{2+2N} I_o + \frac{DV_{in}}{2L_m} T_s \end{aligned} . \quad (62)$$

### D. COUPLED INDUCTOR ANALYSIS

The proposed coupled inductor method was applied to increase the voltage gain ($M_{CCM}$). For normal energy transfer, the turns ratio ($N$) of the coupled inductor is limited as follows

$$N \le \frac{1}{4} M_{CCM} - 1 . \quad (63)$$

The turns ratio ($N$) design of the coupled inductor through voltage gain ($M_{CCM}$) and duty cycle ($D$) is given by

$$N = \frac{M_{CCM}(1-D)}{2} - 1 . \quad (64)$$

Also, the conditions for operating with the BCM can be written as

$$I_{Lm} - \frac{1}{2} I_{Lmp} = 0 . \quad (65)$$

As a result, the minimum magnetization inductance ($L_{min}$) is given by

$$L_{\min} = \frac{V_{in}}{2I_{Lm}} DT_s = \frac{D(1-D)^2 R_o}{4(1+N)^2} T_s . \quad (66)$$

Fig. 11 depicts the current mode by the magnetization inductance value under the conditions of turns ratio ($N$=1, 2, 3), switching frequency ($f_S$=100kHz), and load resistance ($R_o$=2kΩ). The proposed converter operates with DCM at the bottom and CCM at the top based on BCM.

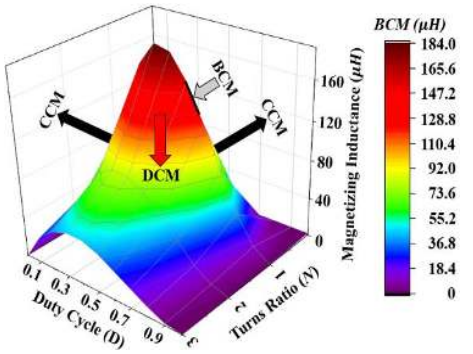


**FIGURE 11. Voltage gain comparison according to turns ratio and duty cycle.**

**TABLE 1. Characteristics by leakage inductance.**
($V_{in}$=40V, $V_o$=400V, $P_o$=1kW, $N$=1, $f_S$=100kHz, $L_m$=100μH)

| $L_k$ | $V_S$ | $i_S$ | $V_o$ |
|---|---|---|---|
| 0.1μH | 73.7V | 7A | 399V |
| 0.5μH | 36V | 3.6A | 395V |
| 1μH | 15V | 1.5A | 388V |
| 5μH | 8V | 0.8A | 348V |
| 10μH | 0.67V | 0.06A | 307V |

Table 1 shows the switch voltage, current, and output voltage according to the leakage inductance ($L_{k1}$=$L_{k2}$=$L_k$) change using PSIM simulation software. When the leakage inductance is increased, the ZCS condition is improved due to the falling rate of the switch current, but the voltage gain ($M_{CCM}$) is lowered. Therefore, an appropriate design according to the tendency to trade off is required.

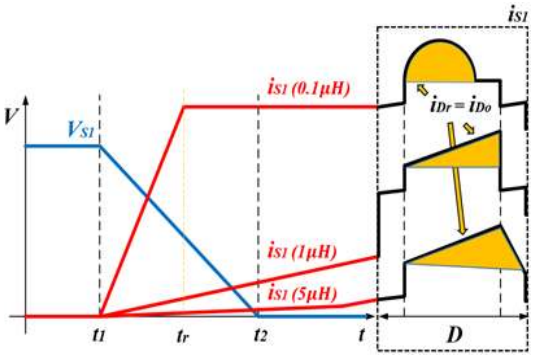


**FIGURE 12. Waveforms due to leakage inductance change.**

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**TABLE 2. Comparison of high step-up converters ([31], [32], [33], [34], [35]) with the proposed converter.**

| High step-up converter | | Converter in [31] | Converter in [32] | Converter in [33] | Converter in [34] | Converter in [35] | Proposed Converter |
|---|---|---|---|---|---|---|---|
| Voltage gain | | $\frac{2+2N}{1-D}$ | $\frac{2+2N}{1-D}$ | $\frac{2+2N}{1-D}$ | $\frac{2+2N}{1-D}$ | $\frac{1+3N}{1-D}$ | $\frac{2+2N}{1-D}$ |
| Voltage stress | switches | $\frac{1}{2(1+N)}V_o$ | $\frac{1}{2(1+N)}V_o$ | $\frac{1}{2(1+N)}V_o$ | $\frac{1}{2(1+N)}V_o$ | $\frac{1}{1+3N}V_o$ | $\frac{1}{2(1+N)}V_o$ |
| | output diodes | $\frac{1+2N}{2(1+N)}V_o$ | $\frac{1+2N}{2(1+N)}V_o$ | $V_o$ | $\frac{N}{1+N}V_o$ | $\frac{2N}{1+3N}V_o$ | $\frac{N}{1+N}V_o$ |
| Quantities of Switches | switches | 2 | 2 | 4 | 2 | 2 | 2 |
| | diodes | 6 | 6 | 4 | 6 | 8 | 6 |
| | cores | 2 ($N_1$:$N_2$:$N_3$) | 2 ($N_1$:$N_2$:$N_3$) | 3 ($N_1$:$N_2$:$N_3$) | 3 ($N_1$:$N_2$) | 2 ($N_1$:$N_2$:$N_3$) | 2 ($N_1$:$N_2$) |

Fig. 12 shows the switch ($S_1$=$S_2$=$S$) voltage, current, and diode current based on Table 1. The leakage inductance can reduce the reverse recovery problem by determining the ZCS condition of the switches and limiting the falling slope of the diodes. It is as follows

$$L_k \geq \frac{V_{Lk}}{2\Delta I_S} t_r \cdot \tag{67}$$

### E. CAPACITOR ANALYSIS

The capacitors of the VMC and the switched capacitor are responsible for clamping the switch voltage to the capacitor voltage, storing and recycling the leakage inductance energy. The values of these capacitors ($C_x$=$\Delta q/V_{Cx}$) must be chosen large enough to prevent the formation of a resonant tank circuit due to leakage inductance during one switching period ($T_s$). It is also possible to reduce the power loss (ESR) by connecting the capacitors in parallel, but an appropriate design is required due to the increase in size, volume and cost [32], [37]. Considering the output power, switching frequency ($fs$), and maximum voltage ripple ($\Delta V_{Cx}$) of the capacitors, the capacitance should satisfy the following conditions

$$C_{1,2} \geq \frac{I_o}{2\Delta V_{C1,2} \cdot f_s}, \; C_{3,m} \geq \frac{I_o}{\Delta V_{C3,m} \cdot f_s} \cdot \tag{68}$$

### F. CIRCUIT PERFORMANCE COMPARISON

To clearly illustrate the advantages of the proposed converter circuit, the conventional high step-up converters [31]–[35] and the proposed converter are compared through Table 2. The proposed method requires two power switches, six diodes, and two cores as the same as [31] and [32]. However, the conventional converters require additional coils [31], [32], [35] or cores [33], [34]. As a result, if the coil and the core are added, there is a problem that not only complicated wiring but also loss, volume and cost increase. It should be noted that the converter of [35] uses eight diodes whereas the proposed method and the methods of [31], [32], and [34] imploy six or less diodes.

If an additional active clamp switch is used then the corresponding gate driver circuit is required to control the switch, so the high step-up converter [33] is the most complex. Based on Table 2, the proposed converter can be considered to be the most advantageous in terms of design cost. From Table 2 it can be seen that for the usual case of $N$=1 the maximum voltage stress of output diodes of the proposed method is $0.5V_o$ as the same as those of [34], [35] whereas those of [31]–[33] are lager than or equal to $0.75V_o$. The maximum voltage stress of swiches of the proposed method is $0.25V_o$ as the same as the conventional methods [31]–[35] for the usual case of $N$=1. Generally, the low voltage stress of the output diode has a great advantage in improving efficiency in high power applications.

### G. LOSS ANALYSIS

The total loss of the proposed converter can be written as

$$P_{Total\_Loss} = P_{D\_Loss} + P_{S\_Loss} + P_{L\_Loss} \cdot \tag{69}$$

Diode losses ($P_{D\_Loss}$) are classified into two types : conduction losses ($P_{D\_con.}$) and reverse recovery losses ($P_{D\_rev.}$). Since the diodes of the proposed converter have no reverse recovery loss, it can be written as ($V_F$ = 0.87mV; $I_{D1\_avg}$ = $I_{D2\_avg}$ =2A; $I_{D3\_avg}$ = $I_{D4\_avg}$ =2.63A; $I_{Dr\_avg}$ = $I_{Do\_avg}$ =2.96A)

$$\begin{aligned} P_{D\_Loss} &= P_{D\_con.} + P_{D\_rev.} \\ &= V_F \cdot I_{D\_avg} + R_D \cdot I_{D\_rms}^2 \simeq V_F \cdot I_{D\_avg} \end{aligned}, \tag{70}$$

$$\begin{aligned} P_{D\_Loss} &= P_{D1\_con.} + \ldots + P_{Dr\_con.} \\ &= 1.74 + 1.74 + + 2.29 + 2.29 + 2.58 + 2.58 \cdot \\ &= 13.21W \end{aligned} \tag{71}$$

Switch losses ($P_{S\_Loss}$) are divided into conduction losses ($P_{S\_con.}$) and switching losses ($P_{S\_ON/OFF}$). Since the proposed converter has no switching loss (turn ON), it can be written as ($R_{DS(ON)}$ = 20mΩ; $I_{D\_rms}$ = 7.16A; $V_{DS}$ = 100V; $I_{D(OFF)}$ = 12.5A; $tri$ = 139ns; $tfv$ = 18ns)

$$\begin{aligned} P_{S\_Loss} &= P_{S\_con.} + P_{S\_OFF} \\ &= R_{DS(ON)} \cdot I_{D\_rms}^2 + [V_{DS} \cdot I_{D(OFF)} \cdot \frac{(tri + tfv)}{2}] \end{aligned}, \tag{72}$$

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$$P_{S\_Loss} = P_{S1\_con.} + P_{S2\_con.} + P_{S1\_OFF} + P_{S2\_OFF} = 1.09 + 1.09 + 9.91 + 9.91 = 21.98W \quad (73)$$

The losses of a coupled inductor ($P_{L\_Loss}$) are divided into core ($P_{L\_core}$) and copper losses ($P_{L\_copper}$).

$$P_{L\_Loss} = P_{L\_core} + P_{L\_copper}. \quad (74)$$

The core loss can be expressed as
($P_c(f(\triangle B)) = 0.136\text{W/cm}^3$; $V_L = 21.3\text{cm}^3$)

$$P_{L\_core} = P_c(f(\Delta B))V_L, \quad (75)$$

$$P_{L\_core} = 2(21\times 0.136) = 5.84W. \quad (76)$$

The copper losses are divided into the primary and the secondary sides of the coupled inductor, which are expressed as
($I_{L1\_pri.\_rms} = I_{L2\_pri.\_rms} = 8.76\text{A}$; $I_{L1\_sec.\_rms} = I_{L2\_sec.\_rms} = 6.45\text{A}$; $R_{dc} = 32\ \text{m}\Omega$)

$$P_{L\_copper} = I^2_{L\_rms} \cdot R_{dc}, \quad (77)$$

$$P_{L\_copper} = 2\cdot P_{L1\_pri.\_copper} + 2\cdot P_{L1\_sec.\_copper} = 4.99 + 2.71 = 7.7W. \quad (78)$$

The total losses of the coupled inductor can be written as

$$P_{L\_Loss} = 5.84 + 7.7 = 13.54W. \quad (79)$$

The loss analysis diagram of the proposed converter can be given as Fig. 13 based on the theoretical analysis and the parameters in Table 3

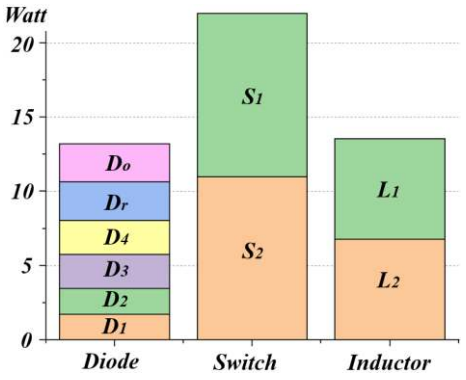


**FIGURE 13.** Device theoretical loss analysis of proposed converter.

## IV. EXPERIMENTAL VERIFICATION

The proposed topology is composed of front-end applications through $V_{in}$ and $V_o$ prototypes as shown in Table 3.

**TABLE 3.** Prototype circuit specifications of the proposed topology [CCM].

($V_{in}$=40V, $V_o$=380V, $P_o$=1kW, $N$=1, $f_S$=100kHz, $R_o$=125Ω)

| | | | |
|---|---|---|---|
| $L_{m1}$ / $N$ | 123.66μH/30:30 | $S_1$, $S_2$ | IRFP4227 |
| $L_{m2}$ / $N$ | 123.17μH/30:30 | $D_1$, $D_2$, $D_3$, $D_4$, $D_r$, $D_o$ | RF1001 |
| $L_{m1}$ / $N$ | 68.47μH/22:22 | $C_1$, $C_2$ | 4μF |
| $L_{m2}$ / $N$ | 68.35μH/22:22 | $C_3$ | 4.7μF |
| $L_{m1}$ / $N$ | 22.3μH/12:12 | $C_m$ | 40μF |
| $L_{m2}$ / $N$ | 22.27μH/12:12 | $C_o$ | 100μF |

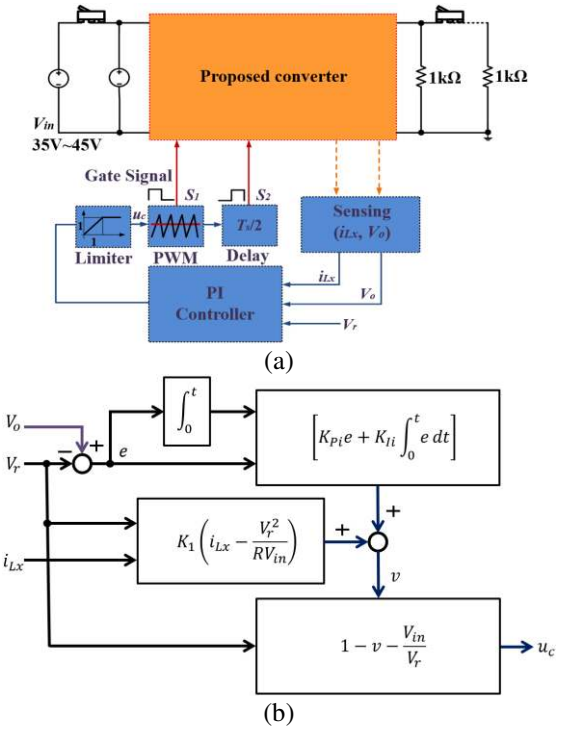


**FIGURE 14.** Control circuit of the proposed converter. (a) Schematic diagram of PI-type control system for hardware. (b) Block diagram of PI-type control algorithm for controller.

Two coupled inductors of the proposed prototype circuit use a toroidal core (OD508), and the primary and secondary windings are 22:22; $N$=1. Fig. 14(a) depicts the system schematic diagram for the hardware and controller of the proposed converter. The experiment was conducted by connecting a power supply (100V/15Ax2set) on the input side and a resistor (1kΩx8set) on the output side through a switch in parallel. Also, the PI controller (closed loop control) for the PWM gate signal was implemented on the DSP TMS320F28335 chip. Fig. 14(b) depicts a block diagram of the control algorithm for the PI controller. The PI controller used a general voltage control algorithm to stabilize the output voltage ($V_o$=380V).

Fig. 15 shows the input voltage $V_{in}$ and leakage inductance current according to the magnetizing inductance value of the proposed converter. The current change rate of the magnetizing inductance is similar to that given in Fig. 12, and the ZCS condition is formed through the falling rate of the current.

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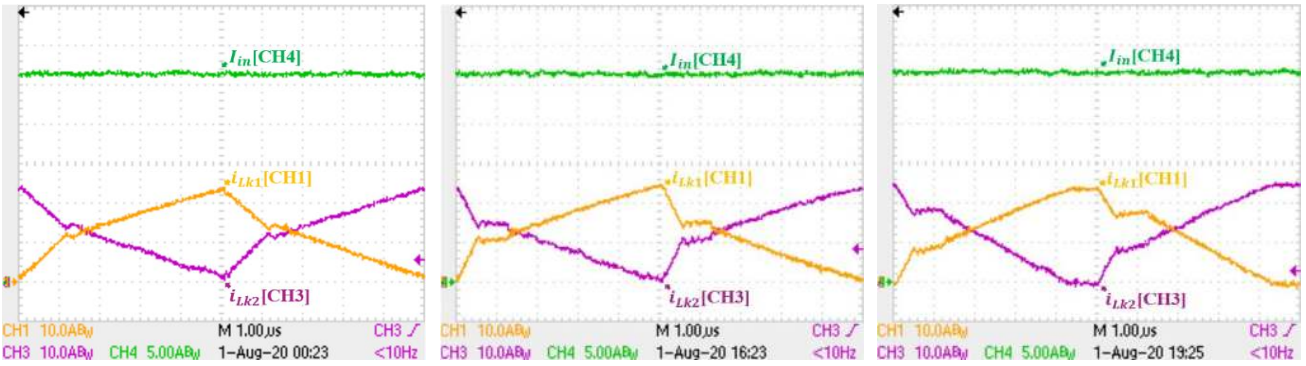


**FIGURE 15.** The experimental waveforms of the proposed converter ($V_{in}$=40V; $I_{in}$, $i_{Lk1}$, $i_{Lk2}$; $P_o$=1kW). (a) $N$=30:30, (b) $N$=22:22, (c) $N$=12:12.

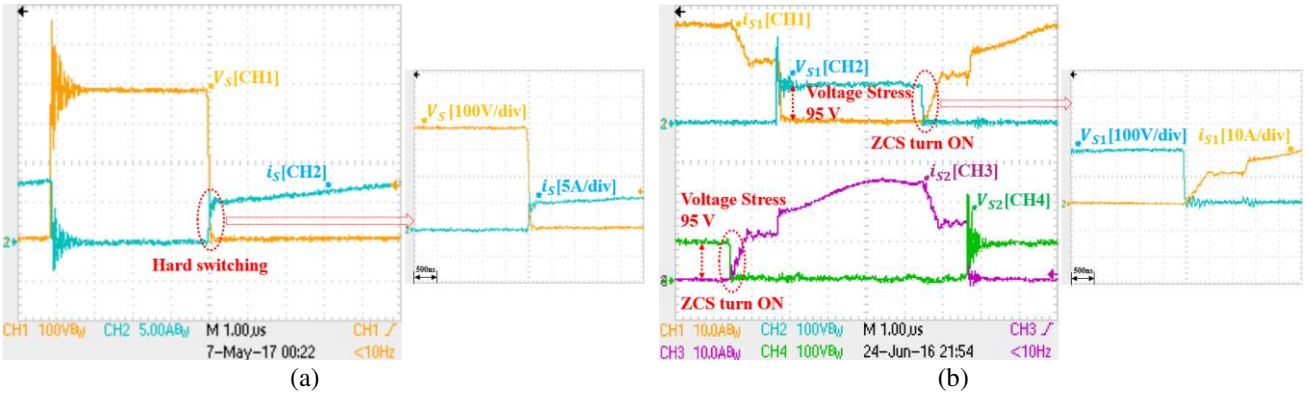


**FIGURE 16.** The experimental waveforms of the converter under CCM ($V_o$=380V; $P_o$=1kW). (a) Conventional boost converter ($V_{in}$=160V), $V_S$, $i_S$, (b) Proposed converter ($V_{in}$=40V), $V_{S1}$, $V_{S2}$, $i_{S1}$, $i_{S2}$.

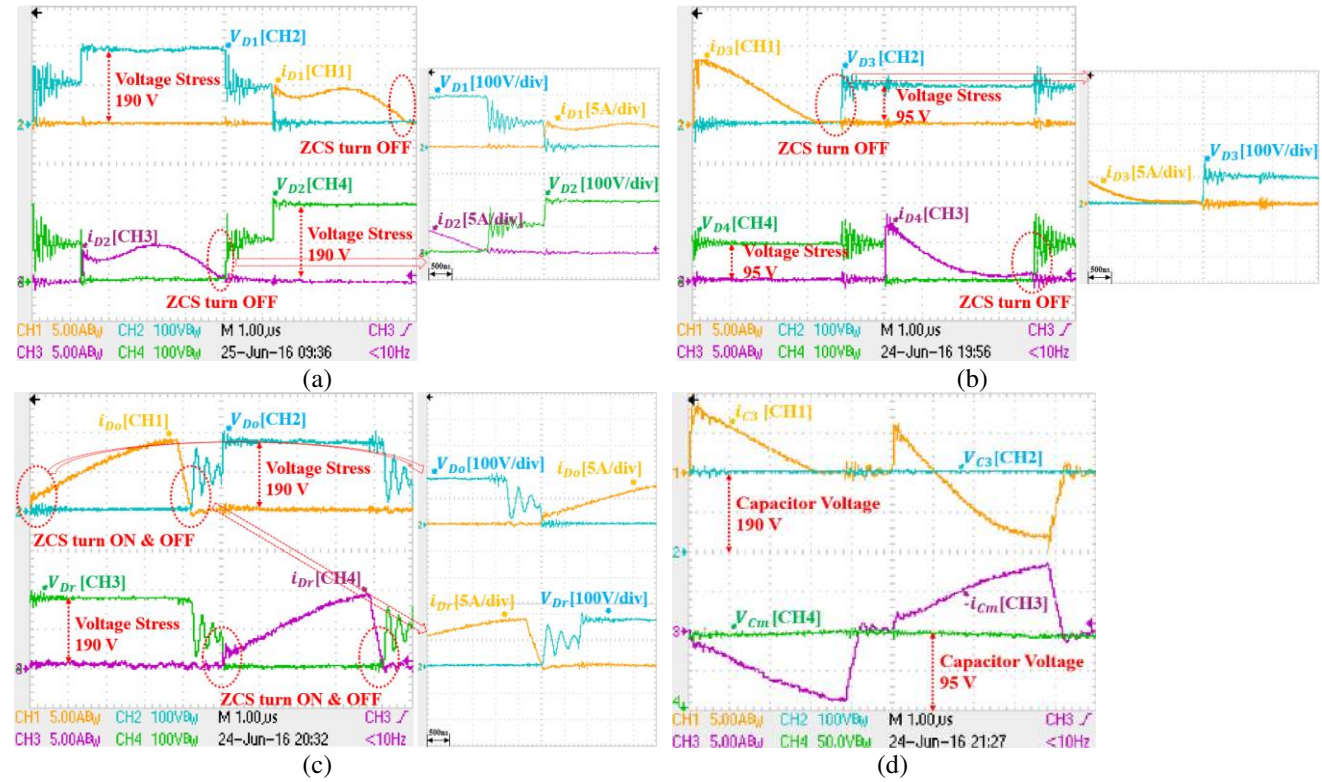


**FIGURE 17.** The experimental waveforms of the proposed converter under CCM. ($V_{in}$=160V; $P_o$=1kW; $N$=22:22). (a) $V_{D1}$, $V_{D2}$, $i_{D1}$, $i_{D2}$. (b) $V_{D3}$, $V_{D4}$, $i_{D3}$, $i_{D4}$, (c) $V_{Do}$, $V_{Dr}$, $i_{Do}$, $i_{Dr}$. (d) $V_{C3}$, $V_{Cm}$, $i_{C3}$, $-i_{Cm}$.

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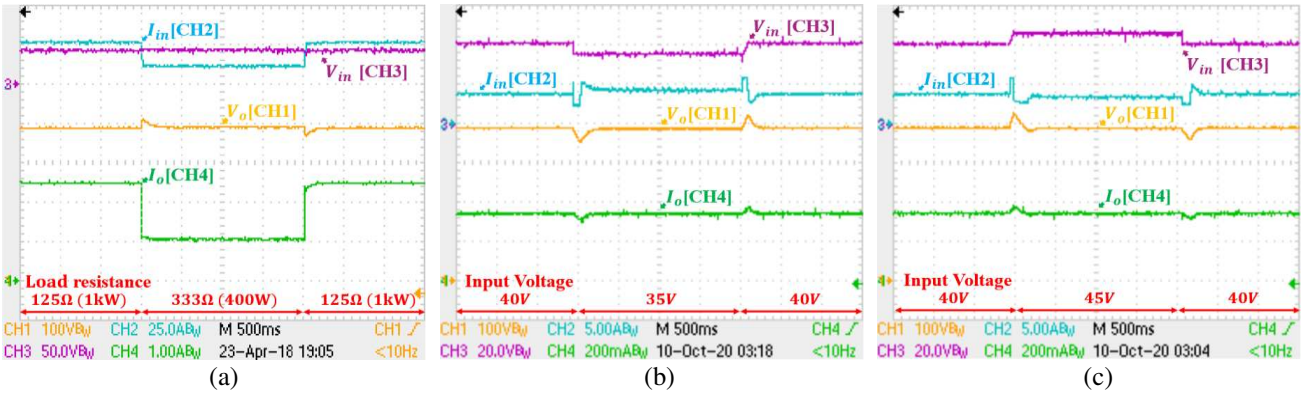


**FIGURE 18.** **Transient response under load resistance and input voltage variation. (a) $R_o$=125Ω→333Ω→125Ω. (b) $V_{in}$=40V→35V→40V. (c) $V_{in}$=40V→45V→40V.**

Fig. 16 (a) shows the voltage and current waveforms of the switch $S$ in a conventional boost converter. In the case of input voltage 160V and duty cycle ($D$=0.6) it achieves 380V equal to the output voltage of the proposed converter. Also, it shows the switching loss through hard switching. Fig. 16 (b) shows the voltage and current waveforms of the switches $S_1$ and $S_2$ in the proposed converter. The switch voltage exhibits about 95V at one quarter of the output voltage during the steady state period and the switches are ZCS turned ON under soft switching conditions. Therefore, high efficiency can be achieved by selecting an active switch having a low voltage rating and a low ON-state resistance level. Fig. 17 (a) illustrates the voltage and current waveforms of diodes $D_1$, $D_2$ under a voltage stress of 190V. Fig. 17 (b) shows the voltage and current waveforms for diodes $D_3$ and $D_4$ with a voltage stress of 95V. Therefore, the diodes $D_1$, $D_2$, $D_3$, and $D_4$ can be applied to the proposed converters with low-voltage rated diodes. Also, when the switch is turned OFF, the current passing through the diode automatically turns OFF according to the mode and becomes ZCS turn OFF. Fig. 17 (c) portrays the voltage and current waveforms for the diodes $D_o$ and $D_r$. The maximum voltage stress is 190V and it is half of the output voltage. Because the current falling slew rate is controlled by the leakage inductance of the coupled inductor, the diodes $D_o$ and $D_r$ turn ON and OFF. Therefore, all diodes in the proposed converter implement soft switching to minimize reverse recovery losses and suppress EMI noise. Also, the voltage stress of all diodes is clamped below the output voltage $V_o$, which is in good agreement with the analysis given in the previous section III. Fig. 17 (d) depicts the experimental waveforms of the voltage and current of the capacitors $C_m$ and $C_3$. During the OFF period of the switch $S_2$, the voltage of $C_m$ charged by the secondary side of the coupled inductor is equal to the output voltage of the conventional boost converter, and a higher charged voltage can be obtained when the turns ratio ($N$) is increased.

Fig. 18 (a) illuminates the transient response waveform of the proposed converter under step load variation. The output voltage 380V is maintained while the load changes abruptly from 1kW→400W→1kW. Fig. 18 (b) and (c) show the transient response waveform of the proposed converter under step input voltage variation. The output voltage 380V is maintained while the input voltage changes abruptly from 40V→35V→40V or 40V→45V→40V. Fig. 19 is the hardware picture of the proposed converter.

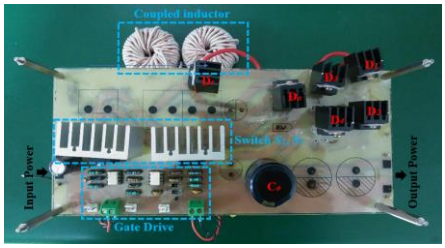


**FIGURE 19.** **The proposed converter hardware used in the experiment.**

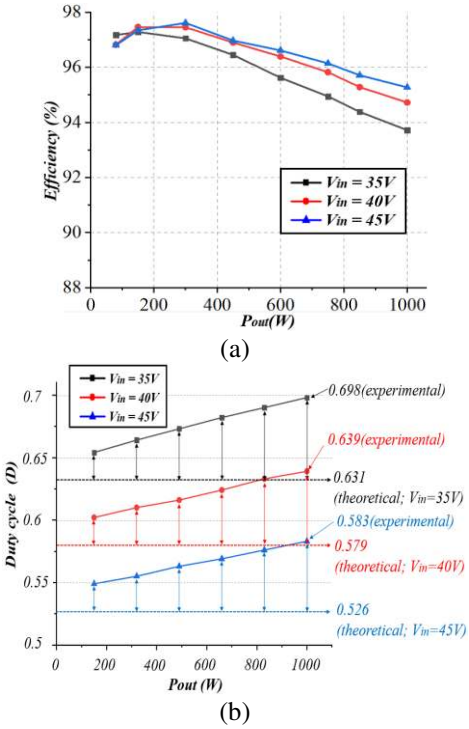


**FIGURE 20.** **Measured values in the experiment of the proposed converter ($V_o$=380V). (a) Measured efficiency at different input voltage and power values. (b) Duty cycle experimental data for voltage gain at different input voltage and power values.**

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Fig. 20 (a) illustrates the efficiency of the proposed converter at different input and load conditions. The voltage and current of the input and output are measured and calculated using the power analyzer PM3000A. When the input voltage is 35V, the maximum efficiency is 97.28 % and the average efficiency is 95.82%. When the input voltage is 40V, the maximum efficiency is 97.46% and the average efficiency is 96.35%. When the input voltage is 45V, the maximum efficiency is 97.61% and the average efficiency is 96.55%. Therefore, the proposed converter achieves high efficiency within a wide input range and a wide load range including light load. Fig. 20 (b) depicts the difference between the theoretical duty cycle value and the duty cycle value applied in the experiment based on the voltage gain. At light loads, the duty cycle increases by 2.3% and increases with increasing power. At the maximum power, the duty cycle increases by about 6%.

Fig. 21 depicts the switch ($V_{S1}$, $V_{S2}$, $i_{S1}$, $i_{S2}$) and the leakage inductance ($i_{Lk1}$, $i_{Lk2}$) waveforms of the proposed converter under light load. Due to the high output voltage, the diodes (CSD10060) in Table 3 prototype circuit specifications were replaced and tested. The switches are automatically ZCS turned ON because the BCM and DCM naturally increase the current of the switches from zero due to the magnetizing inductance. DCM is affected by duty cycle ($D$), inductor and load resistance ($R_o$), but CCM has the advantage of being able to control a wide range with only duty cycle ($D$). In addition, since the inductor and the output side capacitor tend to vibrate during the switch OFF period in DCM, a large ripple current due to the inductor current and parasitic ringing of the semiconductor devices have a problem.

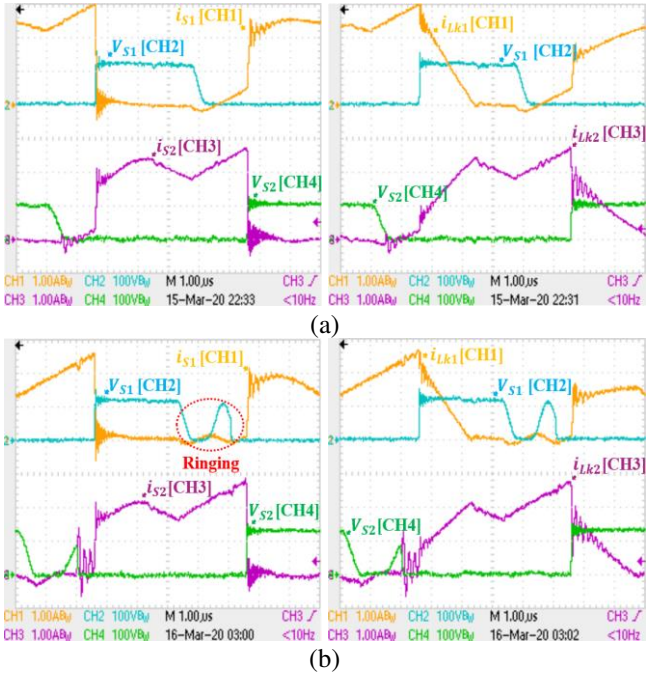


**FIGURE 21. The experimental waveforms of the proposed converter under light load. (a) $V_{S1}$, $V_{S2}$, $i_{S1}$, $i_{S2}$, $i_{Lk1}$, $i_{Lk2}$, [$R_o$=2kΩ, BCM]. (b) $V_{S1}$, $V_{S2}$, $i_{S1}$, $i_{S2}$, $i_{Lk1}$, $i_{Lk2}$, [$R_o$=3kΩ, DCM].**

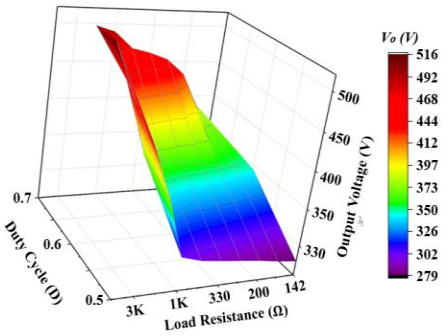


**FIGURE 22. Output voltage by load resistance under duty cycle.**

Fig. 22 is obtained by measuring the output voltage ($V_o$) according to the duty cycle ($D$) and load resistance ($R_o$). In the case of low light loads at $D$ = 0.5; $R_o$ = 3kΩ; $V_o$ = 442V and $D$ = 0.6; $R_o$ = 3kΩ; $V_o$ = 516V, a rapid drop in voltage characteristics is observed as the load resistance increases with high output voltage.

Table 4 compares the devices of the proposed converter and high step-up converter [31]–[35]. The proposed converter implements high step-up voltage gain with the lowest magnetizing inductance through a high switching frequency. The interleaved coupled inductor boost converters help to reduce inductor and capacitor size by effectively doubling the switching frequency through parallel connection [20]. Therefore, by increasing the switching frequency, the inductor and capacitor can be selected with a small number of products and the size is reduced. This contributes to space saving because the mounting area and height are reduced. Switching losses increase due to the high switching frequency, but the proposed converter can be an effective choice because the switches are ZCS turned ON under soft switching conditions as shown in the experimental results. The voltage stress of the switches is proportional to the output voltage, and switches with lower breakdown voltage are used compared to [31] and [35]. Compared to [33], the number of switches is small. This means that the corresponding gate driver, PCB area, and cost are small. The proposed converter is designed with a margin of 150% because it is driven with a maximum of 500V or more in the DCM. Compared with [31]–[35], diodes with 100%~200% lower breakdown voltage were used. The proposed converter fully implements the theory and validity of the design values experimentally.

## V. CONCLUSION

In this paper, a non-isolated high step-up DC/DC converter suitable for green power system applications was proposed. The proposed converter was designed by combining a coupled inductor method and a switched-capacitor method. This paper analyzed the steady-state performance of the proposed converter and this paper compared the proposed method with conventional methods. Experimental verification was carried out with a 35~40V input, 380V output, 1kW power prototype circuit. The analysis and experimental results imply that the proposed

converter achieves high efficiency within a wide input range and a wide load range including light load.

The characteristics of the proposed converter can be summarized as follows.

1) The voltage gain is high enough for application in green power systems.

2) The voltage stress of the switches and diodes is reduced by the voltage clamped on the switched capacitor.

3) The proposed method requires fewer components than most conventional methods and thus the proposed method is cost effective.

4) The ZCS performance of semiconductor devices is realized by using leakage inductance energy. The proposed method gives performance and efficiency comparable to conventional methods.

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**TABLE 4. Device comparison of high step-up converters ([31], [32], [33], [34], [35]) with the proposed converter.**

| High step-up converter | Converter in [31] | Converter in [32] | Converter in [33] | Converter in [34] | Converter in [35] | Proposed Converter |
|---|---|---|---|---|---|---|
| Converter specifications | 20~30V→365V | 30~45V→380V | 35~45V→380V | 24V→380V | 60V→590V | 35~45V→380V |
| Switching frequency/ magnetizing inductance | 50kHz/100μH | 50kHz/95μH | 100kHz/794μH | 50kHz/119μH | 23.5kHz/320μH | 100kHz/68μH |
| Switches | IXTK62N25x2 ($V_{DS}$=250V) | IRF250Nx2 ($V_{DS}$=200V) | IRFP4227Pbfx4 ($V_{DS}$=200V) | IRFP4310x2 ($V_{DS}$=100V) | STW45NM50x2 ($V_{DS}$=550V) | IRFP4227Pbfx2 ($V_{DS}$=200V) |
| diodes | RURG1540Cx2 ($V_{RRM}$=400V) MUR1560Tx4 ($V_{RRM}$=600V) | RURG1540Cx2 ($V_{RRM}$=400V) MUR1560Tx4 ($V_{RRM}$=600V) | RURG1540Cx4 ($V_{RRM}$=400V) | MBR20200x4 ($V_{RRM}$=200V) MUR1640x2 ($V_{RRM}$=400V) | MUR1560x8 ($V_{RRM}$=500V) | RF1001x6 ($V_{RRM}$=200V) |
| Maximum efficiency | About 97.2 % at 400 W | About 95.8 % at 450 W | About 96.2 % at 600 W | About 96.3 % at 600 W | About 97 % at 500 W | About 97.4 % at 300 W |
| Full-load efficiency | About 93 % at 1 kW | About 95.1 % at 1 kW | About 96% at 1 kW | About 95.2 % at 1 kW | About 95.2 % at 870 W | About 94.7 % at 1kW |

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