Research Article

Non-volatile SRAM memory cells based on ReRAM technology

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Abstract
Static Random-Access Memories (SRAMs) are very common in today's chip industry due to their speed and power consumption but are classified as volatile memories. Non-volatile SRAMs (nvSRAMs) combine SRAM features with non-volatility. This combination has the advantage to retain data after power off or in the case of power failure, enabling energy-efficient and reliable systems under frequent power-off conditions. In this work, several nvSRAMs architectures based on Oxide Random-Access Memory (OxRAM) technology are presented and compared. OxRAMs are non-volatile memories considered as a subset of Resistive RAM (ReRAM) technology.

Keywords 1T1R ReRAM · Static Random-Access Memory (SRAM) · Non-volatile Static Random-Access Memory (nvSRAM) · Power consumption

1 Introduction

The rapid growth in the field of portable electronic devices has been driven by integrated circuits continuous decrease in power consumption and cost. In this context, emerging memories and specifically Non-Volatile Memories (NVM) based on new materials and technologies have flourished [1]. The promising flow of NVM technology is expected to be the pioneer technology for the upcoming years [2]. In the recent years, the interest shifted from Flash memories to alternative NVM technologies based on new materials. These technologies show signs of future success towards enhancing the memory performance and increasing the capability of scaling [3]. Among the different alternative memory technologies, Resistive RAM based on metal oxides known as Oxide Random-Access Memory (OxRAM) have attracted a lot of attention [4]. Indeed, OxRAM devices feature faster READ/WRITE operations, better energy conservation and high endurance than classical Flash memories [5].

Traditional Static Random-Access Memories (SRAMs) are volatile, which is a major handicap regarding power-down operation where non-volatile memory is needed. OxRAM can be an integral part of the well-known SRAM. This combination called non-volatile SRAM (nvSRAM) integrates both structures in a single cell [6]. nvSRAM offers a direct bit–bit connection to guarantee a fast switching speed and a high rate of data transfer [7]. This concept allows the structure to achieve genuine data retention and low power consumption with small area. Moreover, the non-volatile capability is integrated on the BackEnd-Of-Line (BEOL) [8]. Classical low power techniques including clock gating and power gating are commonly used for MCUs power reduction. Clock gating technique is used for reducing dynamic power by controlling switching activities on the clock path [9]. In the case of power gating, certain areas of the chip are idle and other parts are activated only for certain operations [10]. In this context, emerging Non-Volatile Memory (NVM) devices can act as key enablers in the development of ultra-low power (ULP) MCUs [11]. This development opens new area of improvements

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in the ability of computing and energy conservation of existing systems including IoT applications [11]. The rapid expansion of emerging memories reached SRAMs technology that really needs a push to overcome serious problems including the reduction of the power supply and in the transistor size, leading to an increase of leakage currents [12].

Proposed nvSRAM designs are implemented in a high voltage 130-nm technology from STMicroelectronics. In section II, the basic OxRAM model used in this work is presented along with the 1T1R OxRAM cell considered in this study. Section III proposes a detailed overview of OxRAM-based nvSRAM structures, with a deep looking on the ability of the nvSRAM to STORE and RESTORE data. In section IV, a discussion and a comparison of the different nvSRAM cells are proposed. At the end of this paper, the conclusion summarizes all the concepts of previous sections.

2 ReRAM technology

2.1 OxRAM model

The OxRAM model approach used in this work is based on the formation and destruction of oxygen vacancies by the induced electric field inside the insulator layer [5]. In this model, SET and RESET (operations used to switch between high and low resistive stats) are constantly managed by a distinct equation where the radius of the conductive filament controls the resistance [13]. This equation is given as:

$$\frac{dr_{CF}}{dt} = \left(r_{CF}\max - r_{CF}\right) \cdot 10^{\beta_{RedOx}} \cdot e^{-\frac{Ea - q \cdot \alpha_{red} \cdot V_{cell}}{k_b \cdot T}} - r_{CF} \cdot 10^{\beta_{RedOx}} \cdot e^{-\frac{Ea + q \cdot \alpha_{ox} \cdot V_{cell}}{k_b \cdot T}} \quad (1)$$

where β_{RedOx} is the nominal oxide reduction rate, E_a is the activation energy, α_{red} and α_{ox} are the transfer coefficients (ranging between 0 and 1), k_b is the Boltzmann constant, r_{CFmax} is the maximal size of the conductive filament radius, T is the temperature and V_{cell} the voltage across the cell.

Furthermore, some assumptions are considered in the model including a uniform electric field and radius of the conductive filaments. Also, the acceleration of the oxide reactions is triggered by the temperature. Lastly, two components are included in the OxRAM total current, which are the current linked to the conductive species (I_{CF}) and the current related to the conduction through the oxide (I_{OX}). The two equations for I_{CF} and I_{OX} are formulated as follow:

$$I_{CF} = \frac{V_{Cell}}{L_x} \cdot \left(\pi \cdot r_{CF}^2 \cdot \left(\sigma_{CF} - \sigma_{OX}\right) + \pi \cdot r_{CF}^2 \max \cdot \sigma_{OX}\right) \quad (2)$$

$$I_{OX} = A_{HRS} \cdot S_{Cell} \left(\frac{V_{Cell}}{L_x}\right)^{\beta_{HRS}} \quad (3)$$

where Lx is the oxide thickness, S_{Cell} is the total area of the device, σ_{Ox} the oxidation rate and σ_{CF} the reduction rate. The two parameters A_{HRS} and β_{HRS} alongside the power law between the bias applied and the cell current are considered, thus I_{OX} trap assisted current can be taken into account. Finally, the total current passing through the cell is expressed as follow:

$$I_{Cell} = I_{CF} + I_{OX} \quad (4)$$

This model is calibrated on silicon (130 nm technology from STM) with no convergence issues when used in combination with CMOS technology. Also, it is considered as one of the few model taking into account the FORMING operation, which is a crucial factor when targeting the fabrication of the proposed devices. Moreover, the 130 nm technology provides High Voltage (HV) transistors needed for the FORMING operation. The need of a HV option (around 3 V) prevents the use of more advanced technology nodes. Indeed, a prospective study in more advanced technology node is pertinent as the resistive element can be integrated in the BEOL between metal lines. The work in [14] demonstrates a 16 Gb ReRAM designed in a 27 nm node, with a 1 GB/s DDR interface and an 8-bank concurrent DRAM-like core architecture.

2.2 1T1R structure

The OxRAM cell consists of three layers, including the insulator layer (switching layer) working as the storage medium which is located between two metallic electrodes (top electrode TE and bottom electrode BE). This Metal–Insulator-Metal (MIM) structure is integrated over a Metal 4 copper layer (Cu) as shown in Fig. 1a. First, the TiN BE is deposited. Then, a 10 nm-HfO_2/10 nm-Ti/TiN stack is added to form a capacitor-like structure [15].

One of the common selector used with ReRAM devices is the CMOS transistor. In this context, the 1 transistor-1 resistor (1T1R) structure has been widely used, where the OxRAM cell is connected on the top of the transistor as shown in Fig. 1b. In addition, the transistor controls the compliance current passing through the OxRAM cell during programming operations to prevent memory cell damage.

Figure 2a, b present 1T1R OxRAM I-V characteristics in linear scale and logarithmic respectively extracted from actual OxRAM devices [16]. The principle operation of OxRAM based memory cells consists of several stages [17]. The first step is the Forming operation which is executed

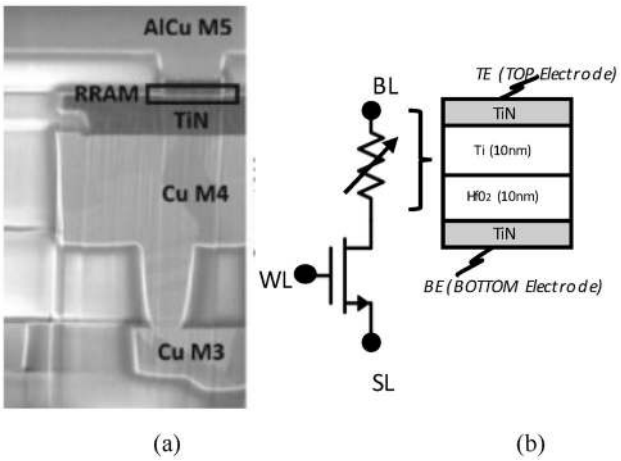

Fig. 1 **a** MIM structure and **b** Basic 1T-1R OxRAM cell

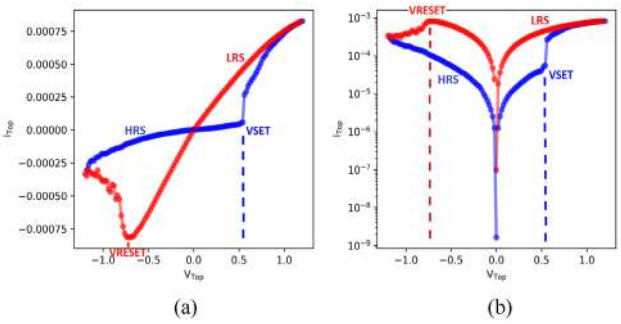

Fig. 2 I–V characteristic of the OxRAM model in **a** linear and **b** log scale

once in the life of OxRAM cell, where a high voltage is induced to switch from High Resistance State (HRS, or pristine state) to Low Resistance State (LRS) [18]. After Forming, the cell can be switched between HRS and LRS by applying specific voltages across the electrodes of the OxRAM cell (i.e. V_{SET} and V_{RESET}) [19]. Based on the linear curve presented in Fig. 2a, V_{SET} value needed to switch to LRS state is equal to 0.57 V, while the V_{RESET} value required to switch back to HRS state is equal to -0.7 V. Note that the log curve is the classical representation of the OxRAM I-V hysteresis as it amplifies low current values. Regarding reliability, as demonstrated in [20], SET/RESET endurance was evaluated up to 10^8 cycles showing that the oxide-based technology is in agreement with SRAM operation.

The behavior of a ReRAM is subject to various deviations, somewhat different from the ones affecting traditional CMOS components. The realization of ReRAM is affected by the manufacturing process. Process variations such as variations in size or ion concentration, environmental conditions (e.g., ambient temperature) or circuit parameters (e.g., variations in power supply) [21, 22] may cause the deviation of the actual electrical behavior of ReRAM from the original design and result. Therefore, it is very important to understand and characterize the impact of process variations on the electrical behaviors of the ReRAM and its implication to the circuit design. Moreover, as the process technology scales, device parameter fluctuations induced by process variations are such as line-edge roughness (LERs) caused by uncertainties in the process of lithography and etching [23], oxide thickness fluctuations (OTFs) caused during sputtering or atomic layer deposition, and random discrete doping (RDDs). The effect of process variations on resistance is similar for both HRS and LRS resistances.

Note that for most nvSRAM cells architectures, extra reliability is provided by the symmetry of the memory cell architectures. Indeed, since the cell is differential, the 2 OxRAMs are affected the same way by variability. Also, as the OxRAM cells are disconnected from the SRAM core cell during the read operation, they are not involved in the read operation, so the read operation is not directly impacted by OxRAM variability.

Concerning the degradation of the OxRAM devices, it is possible to reach an outstanding endurance of twenty billion cycles with the technology considered in the paper [24], which motivates the use of OxRAMs for nvSRAM applications. Figure 3 presents the evolution of the ON/OFF (LRS/HRS) resistance ratio during cycling for 2 OxRAM devices.

Recently, the retention mechanism of ReRAM has attracted considerable attention. At lower temperatures, the conductivity mechanism follows $T^{-1/4}$, describing variable range hopping conductivity. On the other hand, the conductivity mechanism follows T^{-1} at higher temperatures, describing fixed range hopping conductivity [25]. In this context, several works have exploited the data retention of ReRAM with different temperature [26]. In [25], a ReRAM based memory with long-term retention exceeding 10 years at 85 °C is successfully demonstrated. Figure 4. represents the time to retention failure with respect to temperature (1000/T).

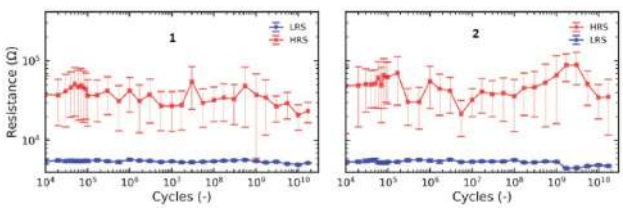

Fig. 3 SET/RESET endurance evaluated for 2 OxRAM devices [24]

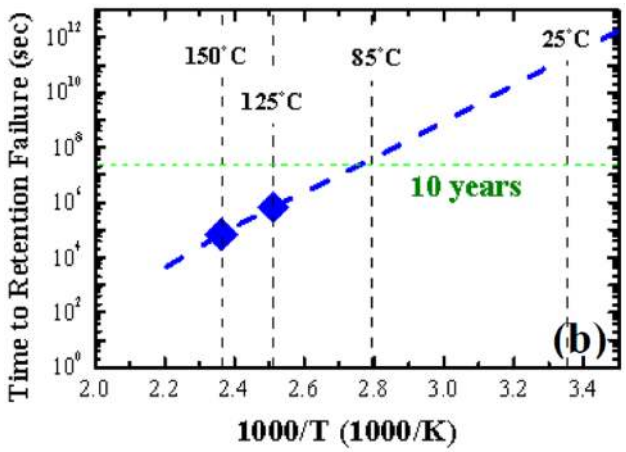

Fig. 4 Time to retention failure [25]

3 1T1R OxRAM cell simulation

The OxRAM model used for simulations is a compact model calibrated on silicon well suited to simultaneously describe SET and RESET operations [27]. Figure 5 presents timing waveform of the 1T1R cell presented in Fig. 1b during FORMING, RESET & SET operations. The duration of these 3 operations are 13 µs, 4 µs and 1 µs respectively.

V(TE,BE) represents the voltage across the OxRAM device. The voltage at the gate of the transistor V(WL) is kept high. During FORMING, the voltage at the top electrode V(BL) is also set high (3.5 V), and the voltage at the bottom electrode V(SL) is 0 V. After FORMING, OxRAM device is RESET with V(BL) = 0 V and V(SL) = 2.7 V. During the SET operation, V(BL) is set to 1.8 V.

4 Non-volatile SRAM

4.1 NVSRAM memory cells

As already mentioned in the introduction, one of the solution to reduce/eliminate standby power in SRAM cells since it to turn the traditional volatile SRAM non-volatile. The addition of this feature is important to eliminate the standby leakage currents. Indeed, the memory can operate in a conventional way in active mode and can be powered OFF in standby mode to prevent standby power consumption without losing its data. Therefore, NVSRAM and SRAM cells have similar data retention time when working in the conventional way (HOLD mode). In the non-volatile mode, NVSRAM cells follows the data retention time of the ReRAM devices used.

In the next sections, five different types of nvSRAMs are presented. These architectures include Majumdar's 4T2R cell [28], Wei's 7T1R cell [29], Turkyilmaz's 8T2R cell [30], Sheu's 7T2R cell [31], and Chiu's 8T2R cell [32].

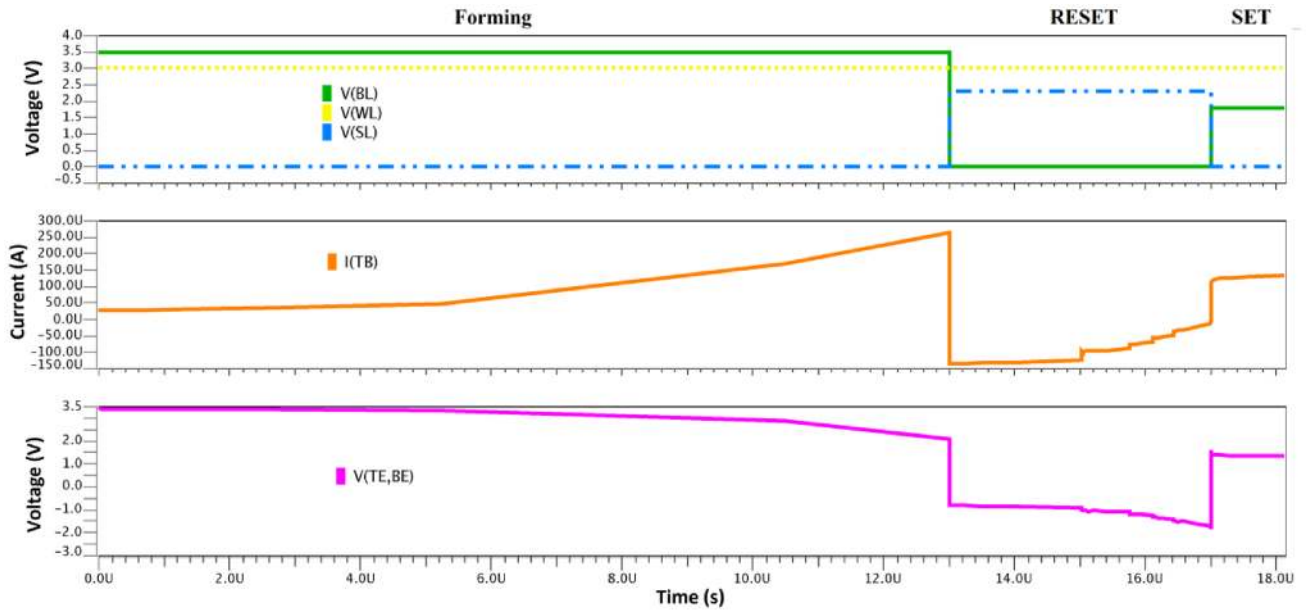

Fig. 5 1T1R timing waveforms

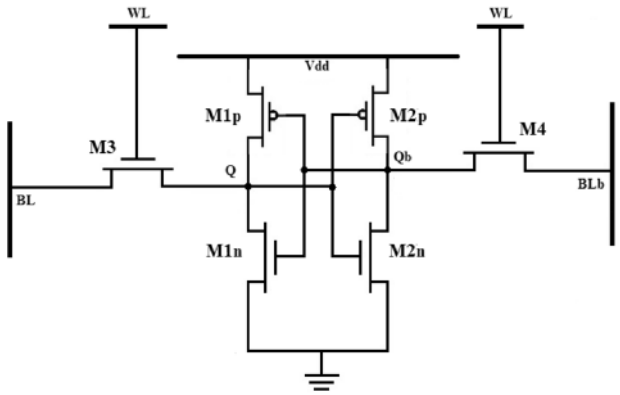

Fig. 6 6T SRAM Cell

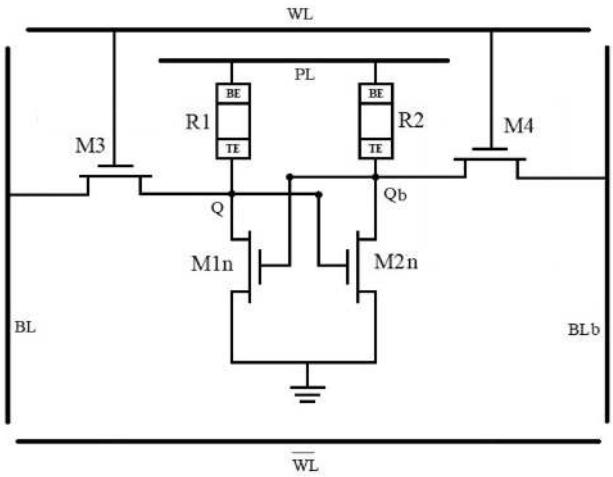

Fig. 7 4T2R nvSRAM Cell

Each nvSRAM cell is based on the conventional SRAM structure. The conventional SRAM structure follows the cross coupled inverters structure presented in Fig. 6. The 3 main operations in a SRAM are HOLD, READ and WRITE. At an SRAM memory array level, rows are called Word Lines (WLs) and columns are called Bit Lines (BLs). WLs are connected to the gates of the select transistors (M5 and M6).

WRITE and READ operations in the memory cells are accomplished through the bit lines. During a HOLD operation, the WL is deactivated to disconnect BL and BLb from the SRAM cell. As a result, data is held in the latch structure on nodes Q and Qb. When WL is activated, READ and WRITE operations can be executed.

5 4T2R cell [28]

The 4T2R nvSRAM cell [28] is presented in Fig. 7. It consists of 2 OxRAMs, 4 Transistors, where M3 and M4 act as access transistors connecting the bit lines to Q and Qb nodes. FORMING operation is mandatory before operating the nvSRAM. Note that OxRAM devices R1 and R2 need a high voltage on the top electrodes to be formed. Note that a STORE operation (SET or RESET operation of the OxRAM cell) is associated with a WRITE operation. During WRITE/STORE, the bit lines are connected to the nodes Q and Qb. The potential difference between TE (Q or Qb) and BE (PL line) of the OxRAM element will either induce a SET (ON state) or RESET (OFF state) operation of the cell. After WRITE/STORE operation the cell data remains unchanged as well as the cell resistances provided that no sufficient voltage potential difference is seen across the OxRAM cells. After power shutdown, the nvSRAM last state can be restored as the data is saved in a non-volatile resistance value. The restored nvSRAM value can be checked during a READ operation after powering on the cell. PL line is connected to V_{DD} and a certain amount of current will pass through the OxRAM devices depending on their resistance values.

Figure 8 presents timing waveforms of the 4T2R Cell. During FORMING, BL and BLb are high and WL and PL low. After FORMING, R1 is RESET while R2 stays in LRS state with BLb and PL high and BL low. The next following 2 steps are Pre-charge and READ to check the memory state. BL and BLb are pre-charged to $V_{DD}/2$ and PL is set to 1 V to not affect R1 and R2 resistance values during the next read operation.

During READ, WL is turned ON thus the data on the nodes can transmitted to the bit lines to reach the reading circuitry. After that, R1 device is SET and R2 is RESET consecutively following the same programming scheme of the previous STORE operation. Since the nvSRAM is non-volatile, the memory cell is powered down to test the ability of the cell to recover the data. The shutdown is followed by a RESTORE operation where a 1 V voltage is applied to PL to get the data back to the storage nodes. After RESTORE, a Pre-charge and READ are performed to check Q and Qb values.

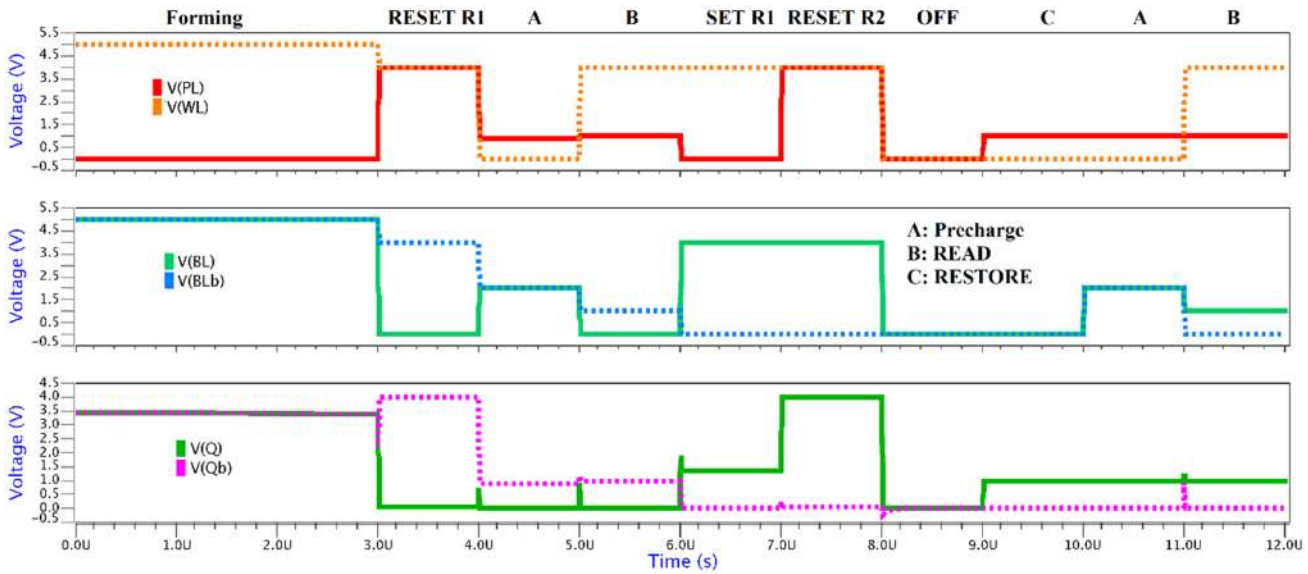

Fig. 8 4T2R timing waveforms

6 7T1R cell [29]

The 7T1R nvSRAM cell [29] is presented in Fig. 9. The structure of this cell consists of 1 OxRAM, 7 Transistors, including 2 CMOS inverters and 2 access transistors. M5 access transistor acts as switch controlling the STORE operation. In this configuration, one OxRAM device is directly connected to the memory nodes Q which is used to store logic states "0" and "1". The resistance of the OxRAM switches between HRS and LRS depending on the data stored at nodes Q and Qb. As the previous structure, FORMING is executed at the beginning but only through BL since there is only 1 OxRAM device.

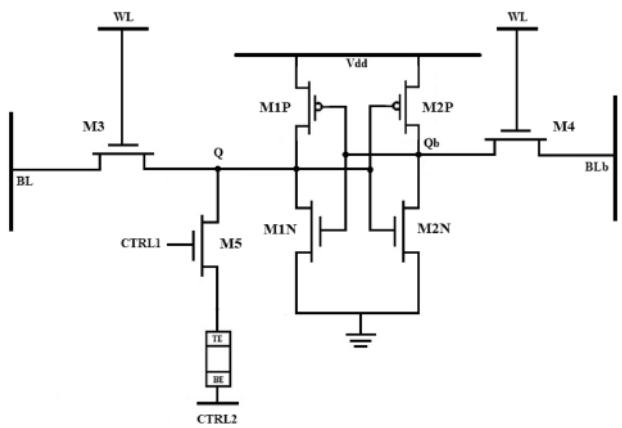

Fig. 9 7T1R nvSRAM Cell

During the STORE operation, the data on the bit line is transferred to the node Q, while CTRL1 is high and CTRL2 is grounded. For instance, if the node Q data is "1", the potential difference across the OxRAM changes the resistance from HRS to LRS. This setup is mandatory to program the device depending on node Q voltage. At the end of this operation, the resistance state of the OxRAM matches the logic states stored at the data nodes (Q and Qb). Note that before STORE, node Q is grounded to discharge any voltage left at this node.

During power-down stage, all the voltage sources are shutdown. During RESTORE operation, the current from CTRL2 passes through the OxRAM device depending on the resistive state. For instance, if the OxRAM is in LRS, the node Q stays at "1" and Qb is discharged through the NMOS transistor M2n.

During READ operation, WL and CTRL1 are high, thus the current passes in the OxRAM device depending on its resistance value. Node Q is connected to BL to sense the memory cell state.

Timing waveforms of the 7T1R cell presented in Fig. 10 differ from the 4T2R cell as WRITE and STORE operations are executed separately. During FORMING, BL is high with WL and CTRL1 set high. RESET is preceded by a WRITE "0" operation where node Q data is stored in the OxRAM device. Note that this the 7T1R architecture can work as a traditional SRAM when M5 is OFF (i.e. independently from the OxRAM cell). BL is high during FORMING and WRITE "1" operation. CTRL1 is high during Forming, SET, RESET and RESTORE operations. The value of the current passing through R1 I(TB) is only considered when CTRL1 (Vctrl) is

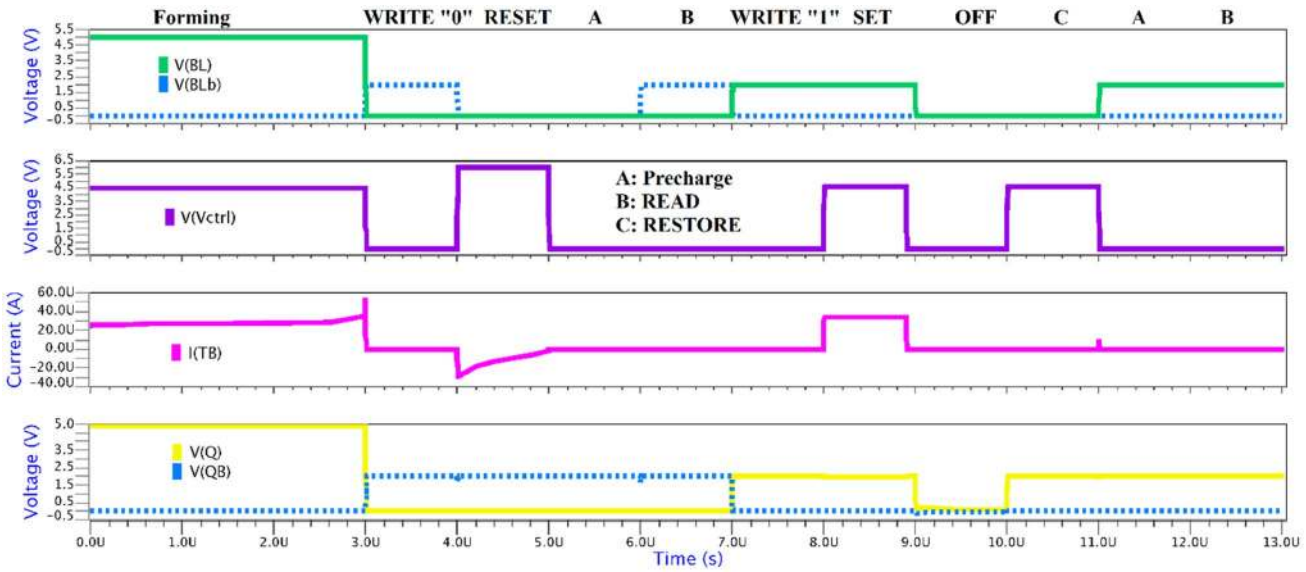

Fig. 10 7T1R timing waveforms

ON, since no current flows in the device when it is OFF. I(TB) increases gradually during FORMING.

RESET operation is performed by applying a high voltage on CTRL1 and CTRL2, while WL is grounded. During this operation, I(TB) decreases to nearly 0 V since the OxRAM switched to the HRS. On the other hand, during SET I(TB) increases as the OxRAM is in LRS state. In RESTORE, CTRL1 is high and the restore voltage is applied on CTRL2 where the current I(TB) will pass through the OxRAM depending on the resistive state (HRS or LRS). After RESTORE, a Pre-charge and READ are performed to check Q and Qb values.

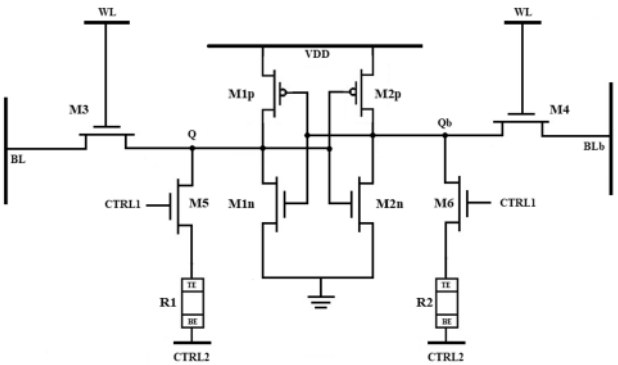

Fig. 11 8T2R nvSRAM Cell

7 8T2R cell [30]

The design proposed in Turkyilmaz paper [30] is very similar to 7T1R cell [29], as two OxRAM devices are used instead of one. However, OxRAMs are accessed using two transistors M3 and M4 controlled by CTRL1 signal as shown in Fig. 11. Regarding the operation principle, the same procedure used for the 7T1R structure can be followed but considering 2 OxRAM cells. SET and RESET are performed by activating M5 and M6. In case of SET, CTRL1 is high and CTRL2 is grounded and according to the data stored in the nvSRAM cell, either R1 or R2 is set to LRS. During RESET CTRL2 is SET to V_{DD} and according to the data stored in the nvSRAM cell, either R1 or R2 is set to HRS.

During RESTORE, if R1 is in LRS, node Q is "refreshed" with logic '1'. If R1 is in HRS, node Q is "refreshed" with logic '0'. R2 follows the same procedure.

After RESTORE, R1 and R2 are disconnected from the rest of the circuit and the SRAM is not effected by the OxRAM cells (i.e. M5 and M6 isolate the OxRAM from the SRAM core to avoid the degradation of the cell performance in the normal mode operation).

Timing waveforms presented in Fig. 12 are practically the same as the 7T1R memory cell [29], but since the 7T1R design is built using 2 OxRAM devices, 2 FORMING operations are needed. During the FORMING stage, BL is set high to form OxRAM R1 (current I1(TB) increases). Then, BLb is set high to form OxRAM R2 (current I2(TB) increases). After FORMING, the 8T2R cell follows the same programming routine as the 7T1R cell but considering two OxRAM devices instead of one. Currents I1(TB) and I2(TB) change depending on the executed operation. During RESTORE, CTRL1 is ON and CTRL2 is set to 1 V. During READ operation, WL and CTRL1 are set high.

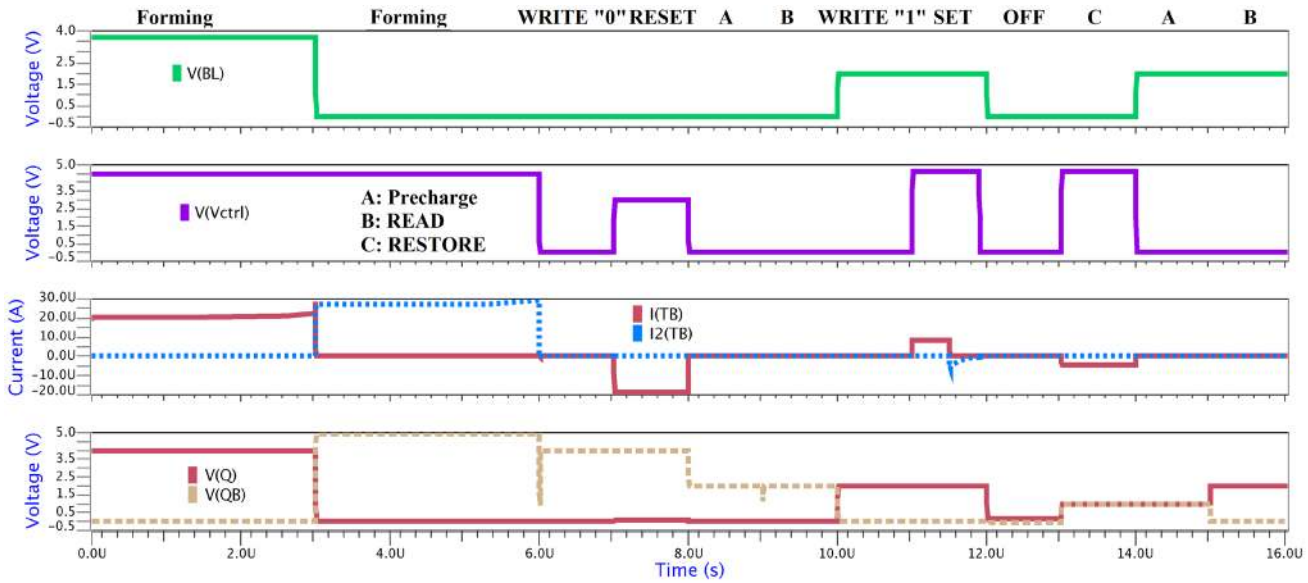

Fig. 12 8T2R timing waveforms

8 7T2R cell [31]

The design proposed in Sheu paper [31] is close to 8T2R cell, excepted that a single signal SWL controls STORE/RESTORE operations as presented in Fig. 13. The 8T2R consists of 2 OxRAMs, 7 transistors including 2 CMOS inverters and 3 access transistors. M_{NSW} transistor controls STORE/RESTORE operations. Also, OxRAMs bottom electrodes (BE) are connected to M3 and M4 which connect the cell to the bit lines.

FORMING operation in the 7T2R cell follows this sequence: WRITE "0" on node Q, R_L FORMING, WRITE "1" on node Q, and R_R FORMING. Note that FORMING operation is performed through BL for both OxRAMs.

During STORE, OxRAMs resistance changes from LRS and HRS respectively depending on Q and Qb node voltages provided that SWL signal is set high. During READ operation, WL is high and SWL low, disconnecting R_L and R_R from the core SRAM cell.

Timing waveforms are presented in Fig. 14. FORMING operation in 7T2R cell [31] is divided into 2 stages (R_L and R_R FORMING). The first stage starts with WRITE "0" with BL and SWL set low and WL set high. Then, R_L is formed with BL and SWL set high and WL set low. In the second stage, R_R FORMING is achieved starting with WRITE "1" operation with BL and WL set high and SWL set low. Note that BL, SL and SWL have the same programming levels during R_L and R_R FORMING.

RESET is performed after WRITE "1" operation, where I1(TB) decreases to approximately 0 V (R1 in HRS state). WL is high and SWL is low during WRITE, and the opposite during RESET operation. WRITE "0" operation is needed before SET. WL and SWL follows the same pattern as in (WRITE/RESET) sequence. During programming, WRITE "0" on the node Q and "1" on Qb are executed simultaneously. During the STORE operation, BL is high to SET R1 and low to RESET R2. Note that BL is the only bit line participating in this operation. During RESTORE, the data retained at node Q is "1" if the OxRAM device is in LRS state and "0" if it is in HRS state. During READ operation, WL is set high and SWL is set low.

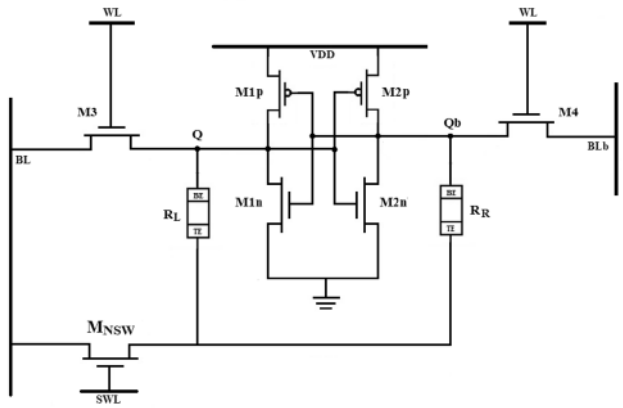

Fig. 13 7T2R nvSRAM Cell

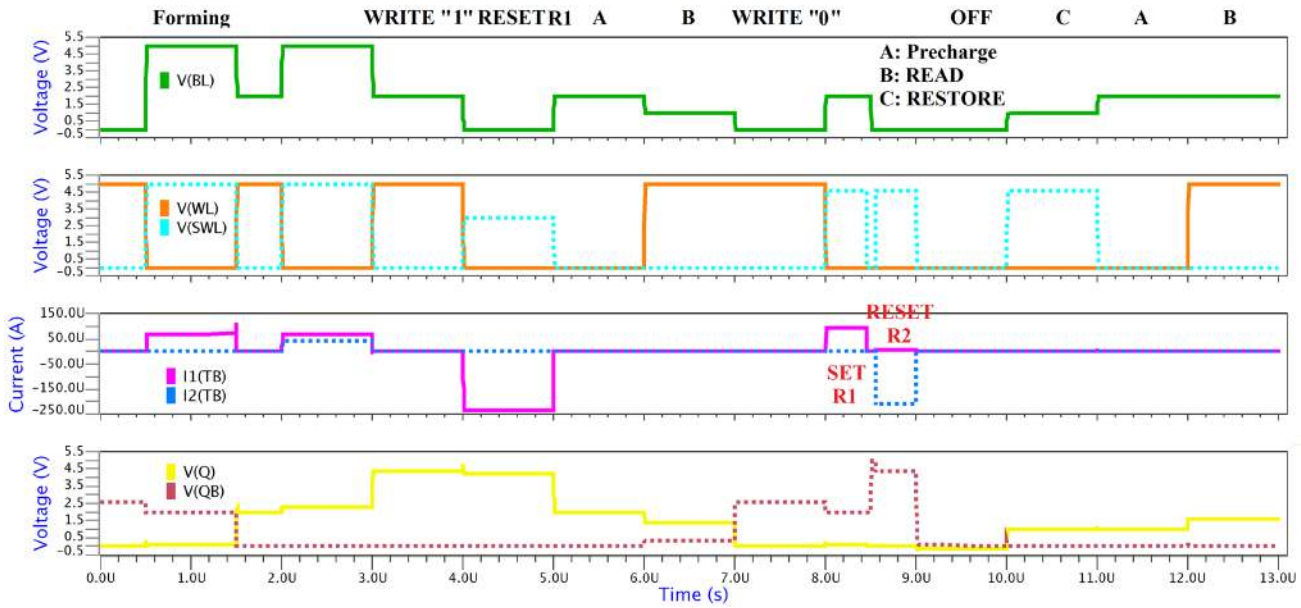

Fig. 14 7T2R timing waveforms

9 8T2R cell [32]

The design proposed by Chiu [32] is based on the 7T2R structure presented in Fig. 13 except that the top electrodes of the OxRAM cells are connected to the different bit lines. The 8T2R cell is depicted in Fig. 15.

The proposed nvSRAM cell spares on control signal as M5 and M6 transistors are controlled by BL and BLb respectively. In this design, FORMING is executed through both bit lines (BL and BLb).

After FORMING, the corresponding bit line is used to STORE (SET/RESET) data on the OxRAM. The switch-line (SWL) is grounded to turn off the selector transistors connected to the bit lines and to prohibit any potential disturbance that affects the stability of the SRAM cell. FORMING operation in this design is performed through the bit lines BL and BLb connected to R_L and R_R respectively. During RESTORE, data stored on the OxRAM devices are recalled to the nodes (Q and Qb).

Timing waveforms of this structure are close to that of 7T2R cell [31] as shown in Fig. 16. During FORMING both BL and BLb are high to form the 2 OxRAM devices at the same time, thus the currents (I1(TB and (I2(TB)) increase simultaneously. The currents I1(TB) and I2(TB) will react depending on the operation executed.

BLb is low during WRITE "1", and high during WRITE "0". During RESTORE, SWL is high and WL is low with restore voltage is applied at the bit lines.

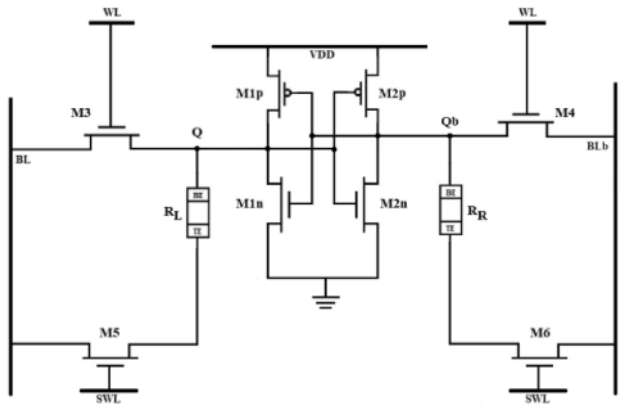

Fig. 15 8T2R nvSRAM Cell (CHIU)

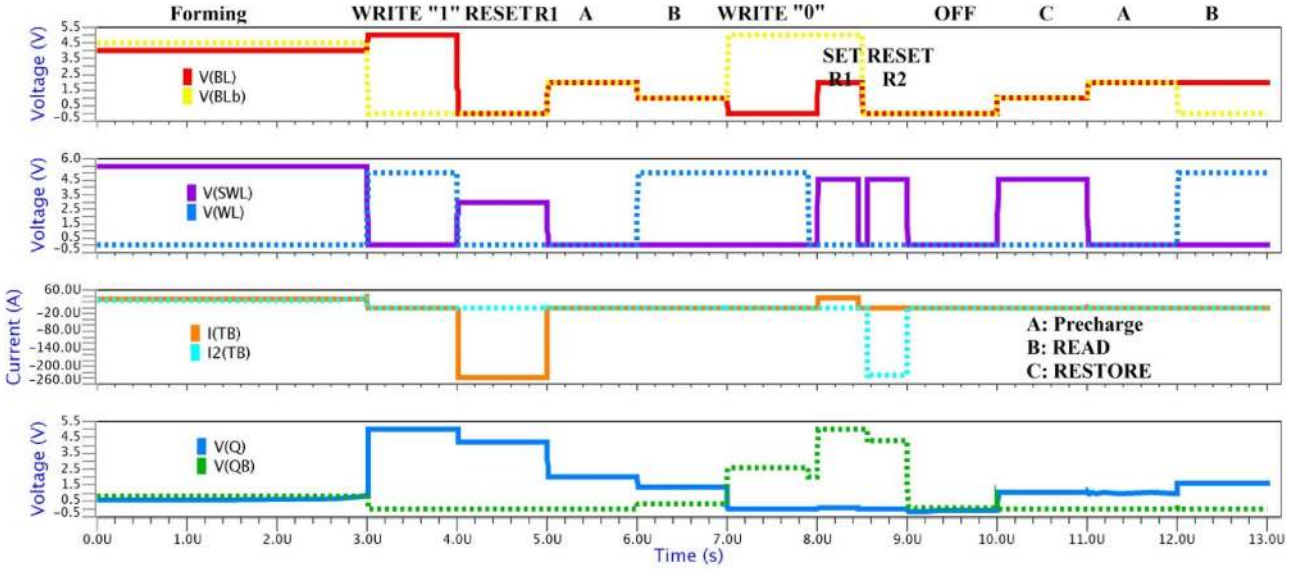

Fig. 16 8T2R timing waveforms (CHIU)

10 Structure comparison and discussions

In this section, 5 nvSRAM cells are discussed and compared showing their advantages and limitations. Table 1 presents nvSRAM cells original CMOS and ReRAM technology used to build the structures. Table 2 illustrates advantages/drawbacks of all nvSRAMs in terms of STORE/RESTORE time, RESTORE method, non-volatility mode, STORE/RESTORE energy, area and silicon verification. All the simulations are completed with the same temperature (27 °C), and supply voltage (2 V).

4T2R nvSRAM cell [28] presents a real-time non- volatility with both WRITE and STORE executed simultaneously. This cell follows the differential sensing approach as

Table 1 NVSRAM cells original CMOS and ReRAM technology

	4T2R [28]	7T1R [29]	8T2R [30]	7T2R [31]	8T2R [32]
CMOS Technology	90 nm	32 nm	22 nm FDSOI	0.18 µm TSMC	0.18 µm TSMC
ReRAM Technology	3 nm thick HfOx	10×10 nm^2 Hf/HfOx	10 nm HfO2	HfOx	ITRI BEOL Hf2O
ReRAM Model	Spice Model [33]	unknown	Spice Model [34]	unknown	unknown

Table 2 Comparison between NVSRAM designs in term of different parameters

	4T2R [28]	7T1R [29]	8T2R [30]	7T2R [31]	8T2R [32]
STORE Time	1.45 ns	0.24 ns	0.24 ns	1 ns	0.87 ns
RESTORE Time	20 ps	0.22 ns	0.22 ns	0.37 ns	0.36 ns
RESTORE Method	Differential	Single-ended	Differential	Differential	Differential
Non- Volatility	Real- time	Before Shutdown	Before Shutdown	Before Shutdown	Before Shutdown
STORE Energy	0.49 nJ	30 pJ	50 pJ	90 pJ	87 pJ
RESTORE Energy	30 fJ	50 fJ	80 fJ	25 fJ	52 fJ
Forming Energy	1.7 nJ	0.35 nJ	0.77 nJ	1 nJ	6.345 nJ
Area	Small	Medium	Large	Medium	Large
Silicon Verified	No	No	No	Yes	Yes

Table 3 NVSRAM parameters variation with temperature

	4T2R [28]			7T1R [29]			8T2R [30]			7T2R [31]			8T2R [32]		
	27 °C	65 °C	100 °C	27 °C	65 °C	100 °C	27 °C	65 °C	100 °C	27 °C	65 °C	100 °C	27 °C	65 °C	100 °C
STORE Time	1.45 ns	1.3 ns	1.2 ns	0.24 ns	0.19 ns	0.16 ns	0.24 ns	0.19 ns	0.16 ns	1 ns	0.85 ns	0.76 ns	0.87 ns	0.8 ns	0.7 ns
RESTORE Time	20 ps	18 ps	16 ps	0.22 ns	0.18 ns	0.15 ns	0.22 ns	0.18 ns	0.15 ns	0.37 ns	0.32 ns	0.26 ns	0.36 ns	0.3 ns	0.24 ns
STORE Energy	0.49 nJ	0.45pJ	0.41pJ	30 pJ	24pJ	24pJ	50 pJ	47pJ	42pJ	90 pJ	84pJ	72pJ	87pJ	80 pJ	70 pJ
RESTORE Energy	30 fJ	27 fJ	22 fJ	50 fJ	46 fJ	40 fJ	80 fJ	76 fJ	71 fJ	25 fJ	23 fJ	20 fJ	52 fJ	50 fJ	48 fJ

RESTORE method (2 OxRAMs). The structure of this design has a low area overhead, since the OxRAM devices replace the pMOS transistors. STORE/RESTORE times measured for this cell are 1.45 ns and 20 ps respectively. This cell is slower than conventional 6T SRAM due to programming of the OxRAM cell which occurs during each WRITE cycle. On the other hand, this design offers a real time non-volatility, and not a last-bit (or power-down) non-volatility as a trade-off for speed drawback. Also, this structure suffers from high power consumption as a STORE operation comes with a WRITE operation. STORE energy including SET and RESET operations is 0.49 nJ. RESTORE energy is around 30 fJ. The energy dissipated by the OxRAM device during Forming is 1.7 nJ.

7T1R [29] and 8T2R [30] nvSRAM cells are based on 6T SRAM core unlike 4T2R cell [18]. Although 7T1R cell [29] suffers from a slight increase of the variability in resistance and process, but this issue does not corrupt the normal operation of the nvSRAM design. The advantage of 7T1R cell [29] is its low power consumption and area, knowing that only one OxRAM is used. The STORE energy is 30 pJ [29] which is slightly less than [30] with 50 pJ. Forming energy for the 7T1R cell is approximately half of that for 8T2R.

Both structures scored similar numbers for RESTORE energy (50 and 80 fJ). Regarding STORE/RESTORE times, they follow the same scheme with 0.24 ns and 0.22 ns respectively. The asymmetric design (single-ended sensing as RESTORE method) makes the structure more susceptible to READ disturb, but it is not considered a significant drawback. 8T2R cell [30] is more consistent in the READ operation, but at the expanse of more occupied area and power consumption.

7T2R [31] and 8T2R [32] non-volatile SRAMs have achieved fast bit-to-bit parallel STORE/RESTORE operations (1 ns and 0.37 ns respectively), low energy requirements, and low READ/WRITE VDD enabling mobile chips to achieve low active-mode power consumption. Furthermore, low-energy STORE/RESTORE operation (90 pJ & 25 fJ for [31], and 0.87 nJ & 52 fJ for [32]) prevents data loss in mobile devices resulting from rapid power failure. Forming energy for [31] is 1 nJ and 6.345 nJ for [32].

Table 3 presents nvSRAM parameters changes with the temperature, including STORE/RESTORE time and energy. The STORE/RESTORE time and energy have decreased with the increase of the temperature. This time decrease is due to the effect of rising the temperature in accelerating the formation of the conductive filament in the switching medium [35]. As the energy has a linear relation with the time, any time change has a direct effect on the energy. Therefore, STORE energy for all cells have decreased. As for RESTORE energy, the variation was minimal since the

RESTORE operation does not include a switching in the resistive state of the OXRAM device [36, 37].

Finally, it should be noted that the STORE time of the OxRAM devices is not constant as it depends on the programming conditions which are different for each memory cell. The same applies for the Forming time.

11 Conclusion

SRAM memory cells based on OxRAM are proposed as an enhanced structure to boost SRAM performances in terms of power consumption. In this context, the 1T1R OxRAM structure is used as a basic cell in different nvSRAM topologies, offering a large band of benefits while keeping a low design complexity. nvSRAM architectures have been explored, showing their advantages and drawbacks. As a conclusion, it appears that 4T2R nvSRAM cell offers real time non-volatility with low area with more power consumption compared to other nvSRAM architectures. The other architectures present a last-bit non-volatility with low power consumption.

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Compliance with ethical standards

Conflict of interest The authors declare that they have no conflict of interest.

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