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Nonvolatile memory characteristics associated with oxygen ion exchange in thin-film transistors with indium-zinc oxide channel and HfO_{2-x} gate oxide

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Non-charge-storage-based nonvolatile memory characteristics associated with oxygen ion exchange are demonstrated in a thin-film transistor (TFT) composed of an indium-zinc oxide (IZO) channel and an oxygen-deficient HfO_{2-x} gate oxide. A nonvolatile increase in drain current and a reduced threshold voltage are obtained upon application of positive gate voltage, with the opposite characteristics upon application of negative voltage. The device shows nonvolatile retention properties and suitable endurance properties after repeated operations. Modulation of channel conductance occurs as a results of oxygen ion exchange between the HfO_{2-x} gate oxide and the IZO channel, which consequently alters the oxygen vacancy concentration in the IZO channel; these vacancies act as n-type dopants. For comparison, a device with a thin SiO_2 layer inserted between the HfO_{2-x} gate oxide and the IZO channel to prevent oxygen ion exchange shows only the increased threshold voltage upon application of a positive gate voltage as a result of electron charging. These results verify the conductance modulation mechanism associated with oxygen ion exchange at the interface of the HfO_{2-x} gate oxide and the IZO channel. In addition, the nonvolatile memory characteristics of the device are indicative of its potential for non-charge-storage-based nonvolatile memory application.

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1. Introduction

Nonvolatile memories are used in a variety of electronic systems and have been attracting particular attention for use in emerging data-centric applications such as artificial intelligences, the Internet of Things, and automated driving systems, which operate with vast amounts of data. For these applications, a nonvolatile memory device is required to have a high data storage capacity and to offer high performance characteristics, e.g., high speed and low power operations. To date, higher storage capacities have been pursued by scaling down the individual memory cells and placing them closer together to increase the integration density. Among various types of nonvolatile memories such as resistive random access memory (RRAM), phase change random access memory (PRAM), and magnetic random access memory (MRAM), flash memory devices using floating gate (charge storage node or charge trap layer) memory cells are regarded as the most representative high-density nonvolatile memory with a low bit cost particularly employing three-dimensional vertical architectures [1]. The floating-gate memory (or called charge trap memory) cell uses a metal-oxide-semiconductor field-effect transistor (MOSFET) structure with a floating gate (charge trap layer) located inside the gate oxide. This cell operates based on the threshold voltage shift that occurs as a result of electrical charging of the floating gate (or charge storage node) upon voltage application to the control gate. Because the threshold voltage shift is determined by the charge density in the floating gate and the consequent change in the electrostatic potential, the number of charges in the floating gate must be controlled precisely.

Although the memory capacity of existing flash memory devices

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has been successfully increased by scaling down the device structure, precise control of the electrical charging of the floating gate will become increasingly difficult as the device is scaled down further. In principle, electrical charging of the floating gate is achieved by tunneling of the electrons from the channel to the floating gate through the tunneling oxide, which is inherently a statistical phenomenon. Additionally, the stored charges will inevitably leak over time even if the floating gate is isolated by the insulating tunneling oxide and control oxide layers [2,3]. This leakage causes an unintended shift in the threshold voltage with a wide distribution, thus causing the reliability problem of memory loss. The approach in which a thicker gate oxide is used to reduce the charge loss brings the drawbacks of increased operating voltage requirements and reduced operating speeds. In addition, repeated tunneling of the electrons through the tunneling oxide for charging and discharging of the floating gate causes the insulating properties of the tunneling oxide to degrade [4]. Furthermore, the electrostatic crosstalk between adjacent cells in high-density memory architectures generated by the stored charges causes threshold voltage drift [5]. These reliability issues in high-density floating-gate memories and the associated performance limitation come from use of an electrical charge storage-based operating principle to store the data.

From this viewpoint, a non-charge-storage-based nonvolatile memory that uses the same MOSFET-based architecture as the existing flash memory has the potential to realize high-density memory that mitigates the reliability issues coming from charge storage-based operation. It employs the gate voltage-driven modification of electrical parameters to change the channel conductance or shift the threshold voltage for the memory function. In this study, we demonstrate non-charge-storage-based nonvolatile memory characteristics, i.e., channel conductance modulation via gate voltage application, in an oxide semiconductor thin-film transistor (TFT) without a floating gate structure, and reveal that the channel conductance modulation is driven by oxygen ion exchange between the gate oxide and the channel layers.

Oxide semiconductor TFTs are compatible with Si technology, which is advantageous given that these nonvolatile memories are likely to be integrated on Si-based platforms [6]. In general, oxide semiconductor TFTs have been investigated to ensure that they can achieve normal transistor function, i.e., that they can operate stably without drift in their threshold voltage and on-state current. However, the nonvolatile memory should be able to perform controllable changes in the threshold voltage and on-state current through application of programming and erasing biases. There have been several reports that oxide semiconductor TFTs have shown the channel conductance modulation without the aid of electrical charging. This modulation has been interpreted to be caused by oxygen ion exchange between the oxide semiconductor channel and the gate insulator [7–9], by redistribution of the oxygen ions inside the gate oxide [10], by tunable polarization of the gate insulator [11,12], and by proton incorporation into the channel [13,14].

Because oxygen vacancies act as n-type dopants in oxide-semiconductors such as ZnO, indium-zinc oxide (IZO), indium-gallium-zinc oxide (IGZO), and indium-tin oxide (ITO) [15], the redistribution of these vacancies under application of the gate bias can be used to tune the channel conductance [7–9]. The channel conductance modulation driven by oxygen ion exchange between the oxide semiconductor channel and the oxygen-deficient gate oxide is recognized to be a non-charge-storage-based operation without use of a floating gate structure. Use of this operation would simplify device fabrication requirements and also relieve the reliability issues that come from the charge-storage-based operating mechanism. Because oxygen ion exchange can modulate the channel conductance in simple MOSFET or TFT structures similar to those used in current flash memory devices, the same high-density flash memory architectures could be used, e.g., the three-dimensional vertical integration structure (3D NAND architecture). Although oxygen ion exchange is a slower process than electronic transport, it has been reported previously that the switching time for a resistive random access memory (RRAM) that uses oxygen vacancy filament formation caused by oxygen ion migration inside its insulating oxides is in the nanosecond range [16]. Therefore, oxygen ion exchange at the interface of gate insulator and channel layer could be used to achieve operating speeds in the same range, which would be faster than the speeds of floating-gate memories that use electron charging through the tunneling process. In addition, compared to the devices using the exchange of protons or some metallic cations, the present device using oxygen ion exchange is more compatible to Si technology and free from the reliability issues coming from possible damages by those ions.

In this study, nonvolatile memory characteristics with a channel conductance that is tunable by a few orders of magnitude upon application of a gate voltage are demonstrated in a TFT composed of an IZO channel layer and an oxygen-deficient hafnium oxide (HfO_{2-x}) layer acting as a gate oxide, i.e., the HfO_{2-x}/IZO TFT-memory. Additionally, the channel conductance modulation mechanism is revealed to be associated with the oxygen ion exchange between the HfO_{2-x} gate oxide and the IZO channel by performing comparison studies with references devices that prohibit oxygen ions exchange between these layers.

2. Experimental

A nonvolatile memory device with an inverted staggered TFT structure containing a HfO_{2-x} gate oxide and an IZO channel layer, called the HfO_{2-x}/IZO TFT-memory, was fabricated with the configuration shown in Fig. 1(a). First, a bottom Al gate layer was deposited by e-beam evaporation as a patterned line with a width of 500 μm on a SiO_2/Si substrate. Then, a 40-nm-thick SiO_2 blocking layer was deposited by radio-frequency (RF) magnetron sputtering to prevent the flow of high gate leakage currents in the device. The approximately 100-nm-thick HfO_{2-x} gate oxide was deposited by RF magnetron sputtering using a HfO_2 target in an Ar ambient. The IZO channel layer was then deposited with a thickness of ~~45 nm by RF magnetron sputtering using an IZO target with a composition that contained 10 wt% of ZnO in an ambient of an Ar/O_2 gas mixture with a flow rate ratio of 1/4. After deposition of the IZO channel, the structure was subsequently annealed at 200 °C for 1 h in air. To form the source and drain electrodes, Mo was then deposited by RF magnetron sputtering with a gate length and width of 100 μm. A 40-nm-thick SiO_2 passivation layer was deposited by the same sputtering process using a SiO_2 target. Finally, post-annealing was performed at 350 °C for 1 h in air.

In addition to the HfO_{2-x}/IZO TFT-memory device, two reference devices were also prepared to verify the memory operation mechanism associated with oxygen ion exchange. The first device contained a thin SiO_2 layer inserted between the HfO_{2-x} gate oxide and the IZO channel layer with a thickness of ~20 nm to prevent oxygen ions exchange between these layers. The second device contained a thicker SiO_2 blocking layer with a thickness of 100 nm between the HfO_{2-x} gate oxide and the Al gate to prevent electron transport between these layers. The electrical characteristics of these devices, including output and transfer curves, retention performances, and endurance properties were examined using an Agilent 4156B semiconductor parameter analyzer. The capacitance-voltage (C–V) characteristicscharcateristics were analyzed using Agilent 4284A LCR meter in the frequency of 1 MHz. The structural

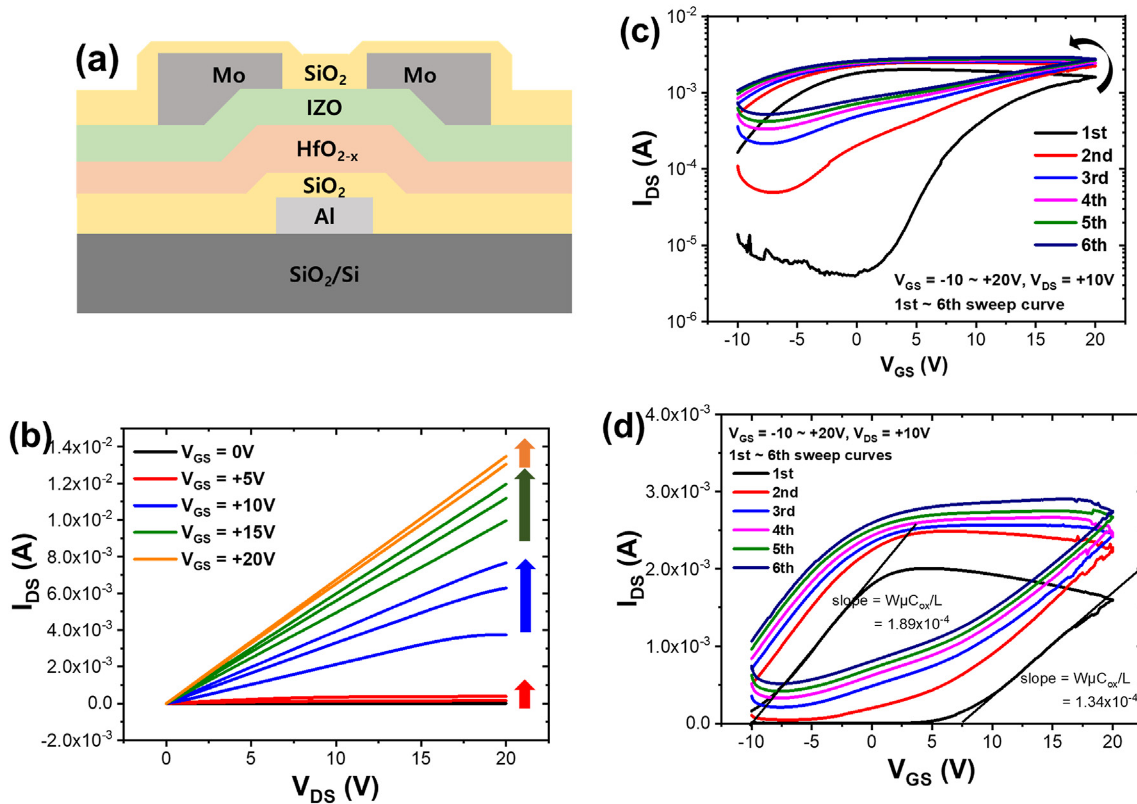

Fig. 1. (a) Schematic illustration of the HfO_{2-x}/IZO TFT-memory structure, (b) its output curves, (c) its transfer curves, and (d) replots of the transfer curves in the form of I_{DS} vs. V_{GS}.

and compositional analyses of the devices were performed using transmission electron microscopy (TEM; JEM 2100F, JEOL) and energy-dispersive spectroscopy (EDS). The chemical bonding states of HfO_{2-x} and IZO layers were analyzed using x-ray photoelectron spectroscopy (XPS; K-alpha, ThermoFisher).

3. Results and discussion

Fig. 1(a) shows a schematic illustration of the HfO_{2-x}/IZO TFT-memory structure. The IZO channel layer and the HfO_{2-x} gate oxide are in direct contact with each other and these layers exchange oxygen ions upon application of a gate voltage. The SiO_2 blocking layer between the HfO_{2-x} and the Al gate reduces the leakage current to the gate for an ordinary TFT operation. Unlike conventional floating-gate memory devices, the device presented here does not have a floating gate structure because it does not use electrical charges to modulate the channel conductance. The output curves of the HfO_{2-x}/IZO TFT-memory are shown in Fig. 1(b). The drain current (I_{DS}) increases with increasing drain voltage (V_{DS}) in proportional to the gate voltage (V_{GS}), which is a normal n-channel output characteristic. However, it can be distinguished that I_{DS} increases sequentially upon repeated V_{DS} sweeps under the same V_{GS} conditions.

The modulation of I_{DS} can also be observed clearly in the transfer curves shown in Fig. 1(c). I_{DS} was measured by sweeping V_{GS} from -10 to $+20$ V in the forward and backward directions under a fixed V_{DS} of $+10$ V. Fig. 1(d) shows replots of Fig. 1(c) in the form of I_{DS} vs. V_{GS} because the measurement condition under which V_{DS} is $+10$ V corresponds to that of the nonsaturation region of I_{DS} in the output curves except at a low V_{GS}, as formulated in Equation (1) [17].

$$I_{DS} = \frac{W \cdot \mu \cdot C_{OX}}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right] \quad (1)$$

As Equation (1) shows, I_{DS} is dependent on several parameters, including the gate length (L) and width (W), the channel layer mobility (μ), the capacitance of gate oxide per unit area (C_{ox}), and the threshold voltage (V_T) at the given values of V_{DS} and V_{GS}. The slope of the curve and the x-axis intercept represent the values of $\mu \times C_{ox}$ and V_T, respectively, assuming that the device geometry (L and W) remains unchanged. The transfer curves in Fig. 1(c) show counter-clockwise hysteresis. At the first sweep, I_{DS} was in the 10^{-6} A range in the off-state and in the 10^{-3} A range in the on-state with a V_T of approximately $+7$ V. During the backward sweep from $+20$ to -10 V, the I_{DS} value remained higher than that during the forward sweep with a significantly reduced V_T of approximately -10 V. It is noticeable that the standby source-to-drain leakage current at $V_{GS} = 0$ V was increased as repeating the measurements due to the increased oxygen vacancy concentration in the IZO channel layer that made the channel more conducting. Although not shown here, the gate leakage current resulting from electron escape to Al gate was not changed as low as on the range of 10^{-6} A at $V_{GS} = +20$ V even after the increase of I_{DS}. Thus, the effect of gate leakage current on the measured I_{DS} is regarded to be negligible. The slopes shown in Fig. 1(d) also increased from 1.34×10^{-4} to 1.89×10^{-4}, which implies an increase in the value of $C_{ox} \times \mu$. The curves in the subsequent sweeps show identical counter-clockwise hysteresis with a continuously increasing I_{DS} and a reduced $V_T < -15$ V. Therefore, the I_{DS} value measured at a V_{GS} of 0 V for a read operation was found to have increased from ~4 μA to 2.6 mA upon repeated V_{GS} sweeps. The reduced V_T that occurs during the backward sweeps could be explained by increased dopant concentration in the IZO channel, i.e., oxygen vacancy concentration, caused by oxygen ion migration

from the IZO channel to the HfO_{2-x} gate oxide after the forward sweep with application of $+V_{GS}$, as will be further discussed later in the paper. The increased dopant concentration is believed to result in the increase in μ through passivation of the shallow traps that act as scattering centers [18].

The gate voltage polarity-dependent I_{DS} modulation behavior is shown clearly in Fig. 2, where the $+V_{GS}$ and $-V_{GS}$ sweeps were repeated separately. The first set of five $+V_{GS}$ sweeps from $0 \rightarrow +10 \rightarrow 0$ V shows a continuously increasing I_{DS} with decreasing V_T, e.g., the I_{DS} measured at the V_{GS} of 0 V increased from 0.14 mA to 0.91 mA (red color). Subsequent $-V_{GS}$ sweeps from $0 \rightarrow -10 \rightarrow 0$ V caused I_{DS} to decrease gradually to the 10^{-5} A range, with V_T increasing. The subsequent repeated $+V_{GS}$ and $-V_{GS}$ sweeps then reversibly increase and decrease the I_{DS}, respectively. The range of these I_{DS} changes reaches up to two orders of magnitude. These wide range and gate voltage polarity-dependent I_{DS} changes demonstrate the potential of the device for use in nonvolatile memory operation with a sufficient memory window. In addition, the changes of I_{DS} and V_T in an analog manner upon repeating voltage applications appear to be feasible for the multi-level memory application. The off-state current in 10^{-5} A range at $-$V is relatively higher than those of the reference devices (Figs. 8 and 9), which is thought to be due to possible interaction between IZO channel and HfO_{2-x} gate oxide increasing oxygen vacancy concentration in the channel during post-annealing process. Further reduction of off-state current by engineering IZO channel, source and drain electrodes, and gate oxide layer needs to be performed to implement integrated memory array. It should be noted here that the dependence of the I_{DS} changes on gate voltage polarity, i.e., the decrease in I_{DS} and increase in V_T that occurs upon $-V_{GS}$ application for programming, is the opposite to that of conventional flash memory operation, in which V_T is increased upon application of $+V_{GS}$. Therefore, programming and erasing operations should be performed using the opposite polarity gate biasing characteristics within the same architecture that is used for current flash memory.

Fig. 3(a) presents the retention properties of the programmed and erased states over time. Following convention of flash memory operation, the programming operation is denoted by the reduction in I_{DS} and the erasing operation is by an increase in I_{DS}. A programming operation performed by repeating application of a $V_{GS} = -15$ V pulse with a pulse width of 20 ms twenty times reduced I_{DS} from 23 to 1.26 μA under the read condition of $V_{GS} = 0$ V and $V_{DS} = +5$ V. It is then found that this reduced I_{DS} was little increased in an hour and retained stably to be about 6.4 μA after 24 h hours. Also, I_{DS} was increased from 17.3 μA to 1.1 mA by the corresponding erasing operation with $V_{GS} = +15$ V and is retained at 5.2 mA after 24 hours with negligible decay. It verifies the nonvolatile characteristics of memory states with a memory window ~10^3, which is defined as the ratio of the I_{DS} values in the programmed and erased states. It should be noted that the relatively high operation voltages of ±15 V and pulse widths of 20 ms are due to the use of a thick gate oxide stack with a total thickness of 140 nm. Nevertheless, this operation conditions are comparable with those of conventional flash memory using much thinner gate stack with about 20 nm in thickness [19]. Therefore, the pulse amplitude and width are expected to be further reduced by scaling down the gate stack thickness. The decrease of HfO_{2-x} gate oxide thickness may limit the amount of oxygen ions that can be exchanged with IZO channel. However, the V_T shift was as high as to exceed 15 V by oxygen ion exchange in the device with 100 nm thick HfO_{2-x}, as shown in Fig. 1(b), it is thought that there is an opportunity to reduce the thickness of HfO_{2-x} as sustaining sufficient V_T shift and I_{DS} change.

In order to evaluate the retention at elevated temperature, I_{DS} was measured over time at the read condition of $V_{GS} = 0$ V and $V_{DS} = +5$ V after applying the gate pulse of $V_{GS} = +15$ V with a width of 20 ms pulse twenty times. I_{DS} measurement was carried out at room temperature after the device was placed on a hot plate for a duration time at 85 °C, which is a typical temperature adopted to evaluate high-temperature retention property in flash memory. Compared to Fig. 3(a) showing negligible decay of I_{DS} over time at room temperature, the increased I_{DS} after applying $+V_{GS}$ pulses gradually decreased over time. The decay at a higher temperature is thought to be due to diffuse-out of oxygen ions, some of which might return back to the IZO channel, then decreased I_{DS}. Nevertheless, the I_{DS} after decay for 1 hr (3600 s) remained to be still higher than initial I_{DS} by an order of magnitude. In order to improve retention properties, the gate stack engineering is requited such as inserting diffusion barrier or microstructural modification of the layers to prevent diffuse-out of oxygen ions causing retention loss over time.

The endurance properties were also studied by performing repeated transfer characteristics measurements and programming and erasing operations by voltage pulsing, as illustrated in Fig. 3(c) and (d), respectively. The V_{GS} sweep was repeated from -10 to $+20$ V in the forward and backward directions under a fixed V_{DS} of $+10$ V a hundred times, during which the hysteresis remained almost the same with ΔV_T of ~15 V. For the pulse operations, the device was first erased by applying a $V_{GS} = +20$ V pulse once with a pulse width of 20 ms, which caused I_{DS} to increase from 0.17 to 2.4 mA, as measured under the read conditions of $V_{GS} = 0$ V and $V_{DS} = +10$ V. Then, a programming operation was conducted successively by applying a $V_{GS} = -20$ V pulse with a 20 ms pulse width, which reduced I_{DS} to 35 μA. The memory window remains ~10 during repetition of these operations up to 100 times, confirming that the programming and erasing operations are reliable and reversible. The programmed state with lower I_{DS} is in the same range of the off-state I_{DS} shown in Fig. 2, whereas the erased state with higher I_{DS} does not reach to on-state I_{DS} range. As a result, the memory window was reduced as the operations are repeated, which is believed to stem from the lower efficiency of the erasing operation performed by $+V_{GS}$ application when compared with the programming operation performed by $-V_{GS}$ application. This is caused by the asymmetric oxygen ion exchange efficiency for I_{DS} modulation and will be discussed later. In order to improve the memory performance, it is required to optimize electrical and

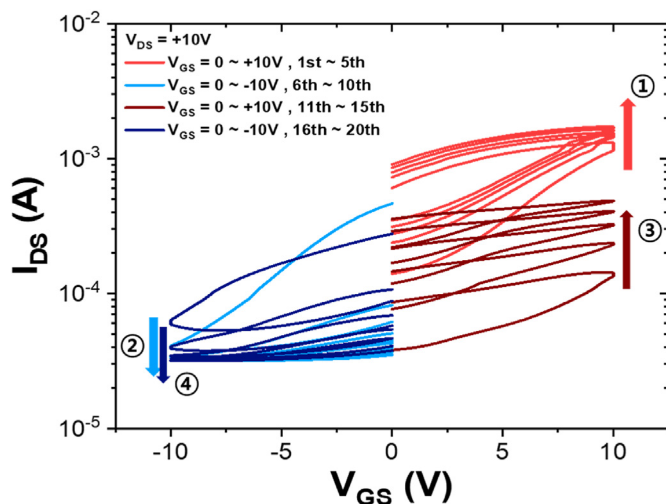

Fig. 2. Transfer curves of the HfO_{2-x}/IZO TFT-memory obtained by repeated sweeping of V_{GS} from $0 \rightarrow +10 \rightarrow 0$ V and $0 \rightarrow -10 \rightarrow 0$ V.

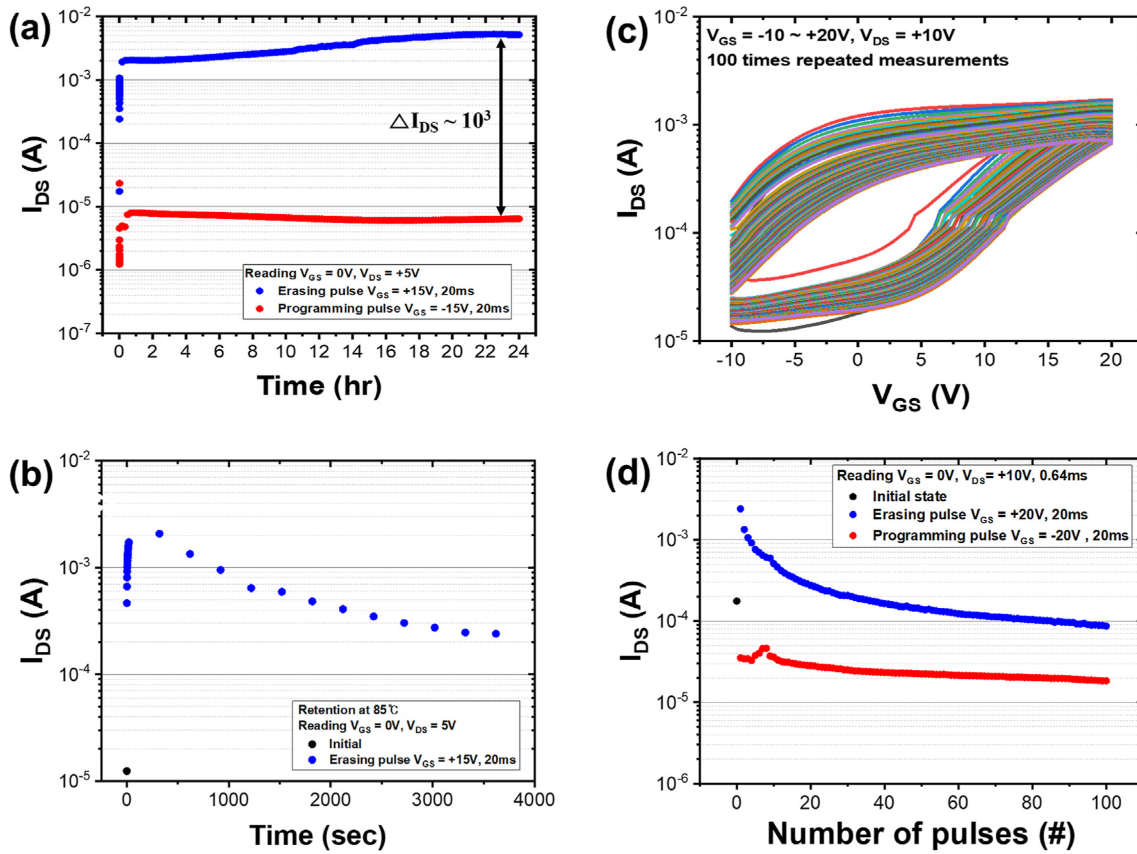

Fig. 3. (a) Retention of the programmed and erased states over time at room temperature, (b) retention of the erased state over time at 85 °C, and (c) endurance properties by repeating transfer characteristics measurements a hundred times, and (d) endurance acquired by repeating programming and erasing pulse operations a hundred times.

physical properties of IZO channel and HfO_{2-x} gate oxides, device structure such as the thickness of each layer, as well as electrical operation conditions such as pulse amplitude and width.

The reversible change in I_{DS} upon application of V_{GS} with respect to the latter's polarity is believed to come from gate voltage-driven migration of the oxygen ions between the IZO channel and the HfO_{2-x} gate oxide, as illustrated schematically in Fig. 4. As mentioned earlier, because the oxygen vacancies (V_O) act as n-type dopants in the IZO channel, the migration of the oxygen ions alters the doping concentration in the IZO channel and consequently modulates I_{DS}. Upon application of $+V_{GS}$, the oxygen ions then migrate from the IZO channel toward the HfO_{2-x} gate oxide. As a result, the charged oxygen vacancy ($V_O^{\bullet\bullet}$) concentration is increased in the IZO channel layer. These charged oxygen vacancies accept electrons from both the source and drain electrodes, and then release them into the IZO channel. This leads to an increase in I_{DS} with a reduction in V_T, which coincides with the results for the device electrical properties. At the same time, the electrons must pass through a SiO_2 blocking layer into an Al gate to sustain charge neutrality in the HfO_{2-x} gate oxide. Otherwise, the electric field caused by the negative charges in the gate oxide would limit further migration of the oxygen ions, which would then result in the opposite tendency of a reduced I_{DS}, as confirmed by the results shown in Fig. 9. Therefore, the gate oxide is not electrically charged, in contrast to the charging in the floating gate in a conventional flash memory. The gate leakage current I_{GS} measured by V_{GS} sweep from 0 to +15 V at V_{DS} = +20 V was in the range of 10^{-8} A, whereas I_{DS} ranged from 10^{-4} to 10^{-3} A (not shown here). The I_{GS} level was much lower than I_{DS}, so the gate leakage would not affect I_{DS} levels. Because the I_{GS} level was not negligible, it is thought that the gate leakage current resulted from electron escape to Al gate, as illustrated in Fig. 4. In that sense, the proper control of electron transport through SiO_2 blocking layer between the HfO_{2-x} and the Al gate is important to achieve channel conductance modulation by oxygen migration in the condition of ordinary device operation avoiding high gate leakage current. The reverse operation is achieved by application of $-V_{GS}$, which repels the oxygen ions back to the IZO channel; I_{DS} is thus reduced and V_T value is restored.

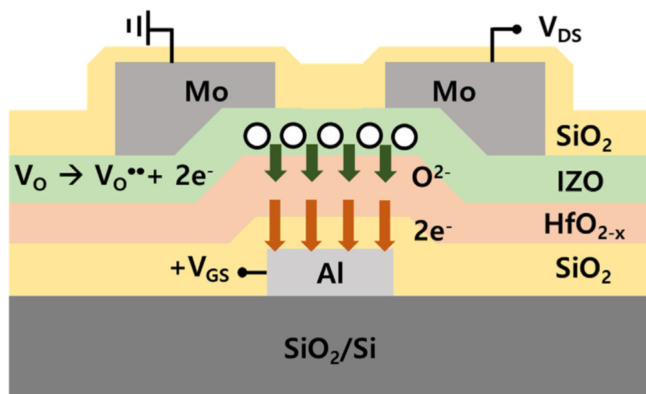

Fig. 4. Schematic illustration of oxygen ion migration from the IZO channel to the HfO_{2-x} gate oxide and simultaneous escape of the electrons through the SiO_2 blocking layer, which results in an increase in the dopant concentration in the IZO channel without electrical charging of the HfO_{2-x} gate oxide.

The conductance change and counterclockwise hysteresis in the transfer curves could be induced when the HfO_{2-x} gate insulator

was ferroelectric due to the presence of oxygen vacancies [20]. Although not presented here, the polarization-voltage (or electric field) analysis in the Al/SiO_2(40 nm)/HfO_{2-x}(100 nm)/Mo structure by sweeping the voltage 0 → +10 → 0 → −10 → 0 V, corresponding to maximum electric field of 0.71 MV/cm, revealed negligible hysteresis. Its remanent polarization values were ~0.05 μC/cm^2, which are much smaller than typical value > ~20 μC/cm^2 of ferroelectric HfO_2 [20,21]. The results of paraelectric characteristics in these structures are thought to be due to that the gate insulator consisted of HfO_{2-x} and SiO_2 bilayer stack, which reduced the electric field and consequent its ferroelectricity. Therefore, it is concluded that the ferroelectric effect is not significant in the present device.

The conductance change could be induced without ferroelectric effect, which was confirmed from our previous reports with IGZO TFTs using TaOx gate oxide [22,23]. In those studies, the conductance change occurred and it could be interpreted with oxygen ion exchange depending on the defective nature and binding energy in the gate insulator and channel layer. These results are thought to supportsupport the mechanism that the conductance change is induced mostly by oxygen migration and consequent channel conductance modulation.

In addition, the capacitance changes upon applying V_{GS} as a result of oxygen ion migration were examined by capacitance-voltage (C–V) measurements. Fig. 5(a) shows the C–V curve upon sweeping V_{GS} from −15 → +15 → −15 V, while source and drain were grounded. It shows the counterclockwise hysteresis with reduced V_T, implying that the carrier concentration in the IZO channel was increased upon applying $+V_{GS}$. It is consistent with the transfer curves of the device in Figs. 1 and 2. Fig. 5(b) shows the C–V curves as repeating $+V_{GS}$ sweeps from 0 → +15 V five times and then repeating $-V_{GS}$ sweeps from 0 → −15 V twice. It shows identical results of counterclockwise hysteresis of C–V curves with increased accumulation capacitance and reduced V_T as repeating $+V_{GS}$ sweeps, and then oppositely increased V_T as repeating $-V_{GS}$ sweeps. Because the device geometry is complex with a large area of gate electrode overlapped with source and drain electrodes, it is not simple to extract quantitative values from the curves. However, it is clear that the accumulation capacitance at $+V_{GS}$ region increased sequentially from ~200 to 260 pF with the repetition of $+V_{GS}$ sweep. The increased accumulation capacitance is explained with an increased HfO_{2-x} permittivity, which could come from the increase of oxygen content in HfO_{2-x}. For example, Pereira et al. reported that the permittivity of sputter-deposited HfO_{2-x} layer was proportional to the oxygen flow used in the sputtering conditions [24]. In their study, the permittivity varied from ~12 to 25 as the O_2/Ar ratio of flow rate was increased from 0 to 0.5, indicating the high sensitivity of HfOx permittivity to the oxygen content. We have also observed in Pt/HfOx/IGZO capacitor structure that the accumulation capacitance was increased after applying $+V_{GS}$, corresponding to an increase in permittivity from ~9.2 to 17 [7]. The results of increased accumulation capacitance after repeating $+V_{GS}$ sweep coincide also well with the increase in I_{DS} as a result of oxygen ion migration.

The migration rates of the oxygen ions from the IZO channel to the HfO_{2-x} and vice versa may differ from each other, depending on the binding energy of the oxygen ions with the cations or the density of the nearby vacant sites for the migration. The quantitative study on the activation energy for oxygen ion migration under electric field has not been performed yet, which is influenced by the atomic density, stoichiometry, microstructure, and defect density of the layers. It was previously demonstrated that the channel conductance modulation by oxygen ion migration was strongly dependent on the states of channel layer and gate oxide. For example, the TFT with atomic layer deposited-HfO_{2-x} gate oxide

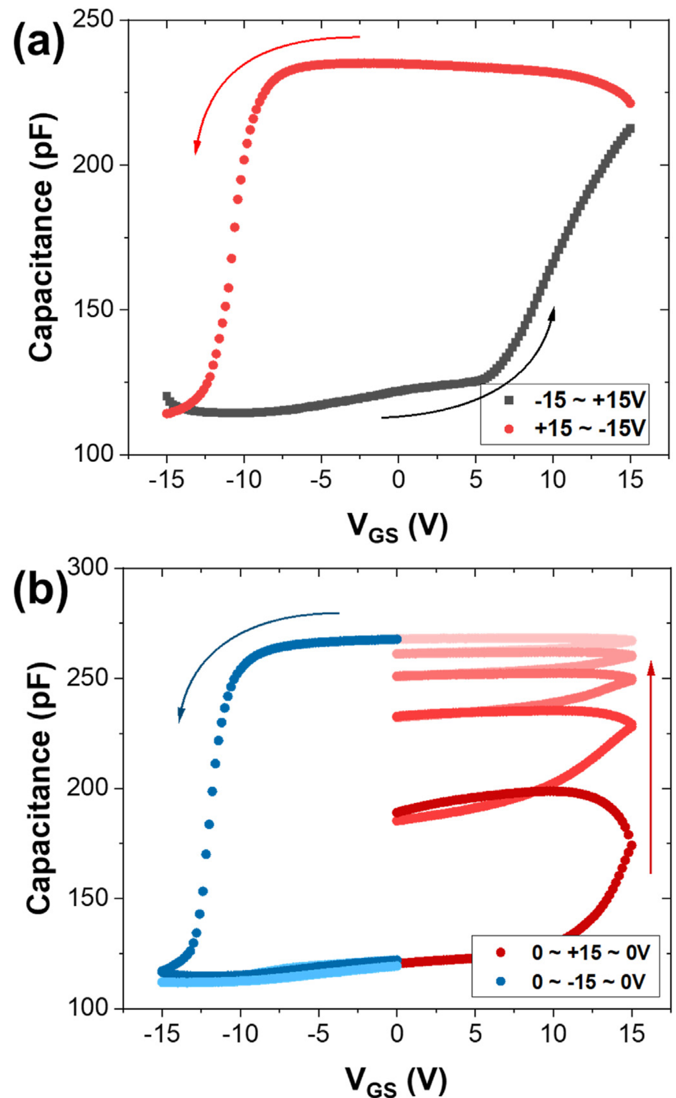

Fig. 5. C–V curves of HfO_{2-x}/IZO TFT upon V_{GS} sweeps of (a) −15 → +15 → −15 V and (b) 0 → +15 V five times and 0 → −15 V twice.

and ZnO channel layer that were processed at low temperature exhibited channel conductance modulation by oxygen exchange upon applying gate bias, whereas the device processed at high temperature did not show conductance change [8]. It was notable that despite the stoichiometry of HfO_{2-x} layers obtained by XPS analyses were found to be similar with O/Hf ~1.7 for both cases [8], the channel conductance change characteristics of these devices were clearly distinguishable. It means that not just the stoichiometry of the layers, but their microstructures are also important for oxygen ion migration. As discussed earlier, the study of the effect of nitrogen doping in the IGZO channel of TFT with TaO_x gate insulator on the conductance change characteristics disclosed also that nitrogen doping in the IGZO channel reduced the conductance change upon applying gate bias [23]. It could be interpreted by that the partial replacement of oxygen with nitrogen, having a higher binding energy with metal-cations, suppressed oxygen vacancy formation, then reduced the channel conductance change. These results supportedsupported that the states of the IZO channel and HfO_{2-x} gate oxide layers are important for oxygen migration and consequent channel conductance modulation. In addition, the consequent change in I_{DS} is complicate because the migration of the

oxygen ions alters several parameters at the same time such as V_T, μ, and interface states that determines the shape of transfer curves. Therefore, the programming and erasing operations may be asymmetric, as shown in Fig. 3.

The oxygen ion exchange between the IZO channel and the HfO_{2-x} gate oxide is expedited when the layers have sufficiently large numbers of vacant sites for oxygen ion migrations. To assess the defective natures of these layers, structural and compositional analyses of the layers were performed using transmission electron microscopy (TEM) with energy-dispersive spectroscopy (EDS). The bright-field TEM micrograph in Fig. 6(a) shows that the gate stack consists of the Al gate, the SiO_2 blocking layer, the HfO_{2-x} gate oxide, the IZO channel, and the SiO_2 capping layers. The HfO_{2-x} gate oxide and the IZO channel layers are found to show contrasts within their layers, which may come from the inhomogeneous atomic densities of these layers caused by the presence of large numbers of vacancies. The high-resolution TEM micrograph in Fig. 6(b) also shows that the HfO_{2-x} gate oxide and the IZO channel layers consist of small grains with a few tens of nanometers. The layers are not found to be grown with a typical columnar grain structure, but with a particulates structure having lots of boundaries with clear contrast within the layers stemming from unequal atomic density. Thus, it is believed that these structures of the HfO_{2-x} and the IZO layers ease the exchange of oxygen ions between the layers by providing abundant grain boundaries for oxygen ion migrations.

The selected area diffraction patterns shown in Fig. 6(c) match mostly with those of the crystalline monoclinic structure of HfO_2 (JCPDS 43−1017) and the body-centered cubic phase of In_2O_3 (JCPDS 06−0416). However, since the peaks for monoclinic phase of HfO_{2-x} are not clearly distinguished from the peaks for other phases, the HfO_{2-x} layer might be composed of mixed phases and further detailed analysis needs to be performed. Because the IZO layer has a In_2O_3/ZnO composition ratio of ~9, as shown in Fig. 6(d), the diffraction peaks coincide with those of In_2O_3 with a slightly reduced lattice size because the ionic radius of Zn^{2+} is smaller than that of In^{3+}. The compositions of the layers analyzed by EDS, as illustrated in Fig. 6(d), show that the HfO_{2-x} gate oxide is sub-stoichiometric with its O/Hf ratio ~1.5, showing it to be oxygen deficient. It is believed that the defective nature of the sub-stoichiometric HfO_{2-x} gate oxide with this oxygen deficiency agrees well with the TEM micrographs and eases the migration of oxygen ions under application of the gate bias by providing vacant oxygen sites.

In addition, XPS analysis was performed to analyze the change of oxygen content in the IZO channel and the HfO_{2-x} gate oxide layers before and after gate voltage application. The concentration of oxygen vacancies acting as n-type dopants in sputter-deposited IZO channel was reported to vary in the range of 10^{15}–10^{20} cm^{-3} depending on O_2/Ar flow ratio [25], thus I_{DS} change would correlate with the change of oxygen contents in the IZO channel. Fig. 7 shows the XPS spectra of the O 1s level in the IZO and the HfO_{2-x} layers

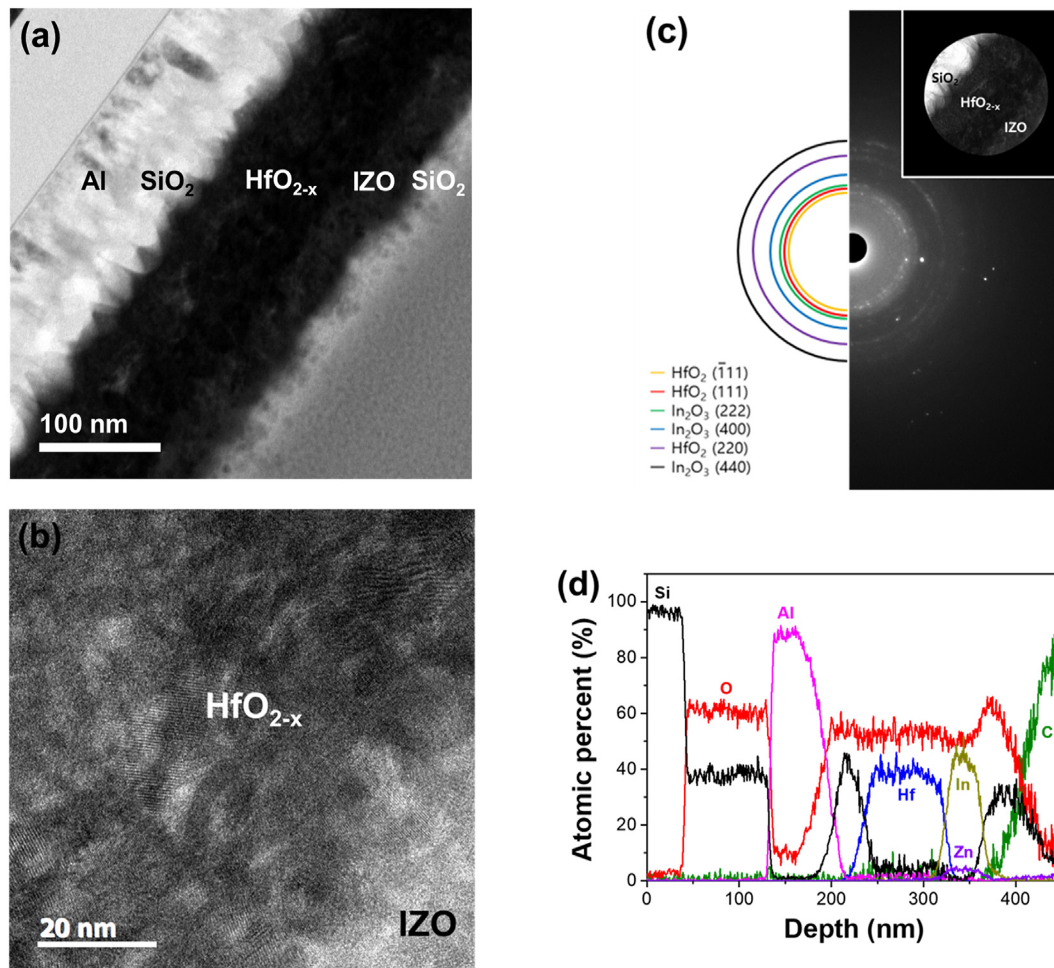

Fig. 6. (a) Cross-sectional bright-field TEM and (b) high-resolution TEM micrographs, (c) selected area diffraction patterns, and (d) depth profile of the composition of each layer measured via EDS compositional analyses in the scanning transmission electron microscopy (STEM) mode.

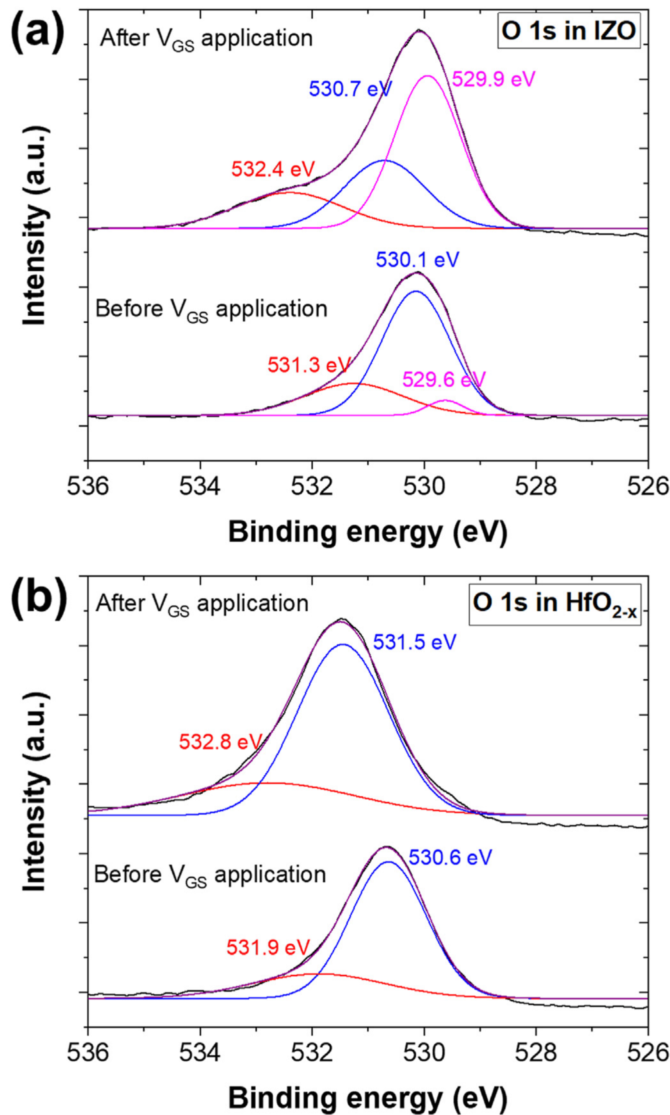

Fig. 7. XPS spectra of O 1s peaks in (a) IZO channel and (b) HfO_{2-x} gate oxide before and after gate voltage application.

before and after gate voltage application with $V_{GS} = +15$ V with a pulse width of 20 ms twenty times. The peaks were obtained at the middle positions of the layers in thickness, thus they could not be calibrated with C 1s peak. Therefore, the intensities and positions of the peaks were relatively compared. The O 1s peak in the IZO channel before gate voltage application is deconvoluted to 529.6 eV for lattice oxygen with an In—O bond, 530.1 eV for lattice oxygen with a Zn—O bond, and 531.3 eV for hydroxyl bonds or oxygen-deficient region [26]. After gate voltage application, the intensity of the peak for the In—O at 529.9 eV was increased while that of the Zn—O peak at 530.7 eV was decreased. Also, compared to lattice oxygen peaks, the peak at 532.4 eV for hydroxyl bonds or oxygen-deficient region was further shifted with a higher binding energy, which is typically observed when oxides become more oxygen-deficient [27,28]. It is noticeable that the bonding states of oxygen with In and Zn cations were changed and the oxygen deficient peak was also shifted after gate voltage application. Although it does not provide definite evidence, the results of the change in oxygen bonding states supportsupport that internal changes such as oxygen exchange occurred by applying gate voltage. The O 1s peak in the HfO_{2-x} gate oxide is deconvoluted to 530.6 eV for lattice oxygen and 531.9 eV for Hf—OH bonding before gate voltage application [29]. After gate voltage application, those peaks were shifted to higher energies of 531.5 and 532.8 eV, respectively. Because the calibration with C 1s reference peak was not performed, it is not clear whether the shift of peaks comes from the changes in bonding states. The peaks were obtained at the middle position in thickness, thus the change in the peaks by oxygen exchange could not be observed because the exchange should occur near the interface.

As discussed earlier, the I_{DS} modulation mechanism illustrated in Fig. 4 includes two requisite processes. The first process is that oxygen ions are exchanged between the IZO channel and the HfO_{2-x} gate oxide during gate biasing. The second process is that the electrons escape from the HfO_{2-x} gate oxide through the SiO_2 blocking oxide to sustain charge neutrality within the HfO_{2-x} gate oxide. To confirm these processes, two reference devices were prepared and their electrical properties were compared with those of the HfO_{2-x}/IZO TFT-memory. The first reference device contains a thin SiO_2 layer with a thickness of ~20 nm that is inserted between the IZO channel and the HfO_{2-x} gate oxide to prevent oxygen ion exchange, as illustrated in Fig. 8(a). The output curves in Fig. 8(b) indicate that I_{DS} is reduced slightly when measurements are repeated at the given V_{GS}. In addition, the transfer curves in Fig. 8(c) show clockwise hysteresis with a reduced I_{DS} and increased V_T during backward sweeps, which is typically observed when negative charges such as electrons are stored at the interface or inside the gate oxide. These characteristics are dissimilar to those of the HfO_{2-x}/IZO TFT-memory presented in Fig. 1, which show consecutive increases in I_{DS} upon repeated output measurements and counter-clockwise hysteresis in the transfer curves. The difference in this device structure from the HfO_{2-x}/IZO TFT-memory is that a thin SiO_2 layer has been inserted between the IZO channel and the HfO_{2-x} gate oxide that blocks the oxygen ion exchange between them. Only small numbers of electrons are allowed to be transported through the inserted SiO_2 layer under application of $+V_{GS}$, thus leading to the slight increase in V_T.

The second reference device has a thicker SiO_2 blocking layer inserted between the HfO_{2-x} gate oxide and the n^+-Si gate to prevent electrons from escaping through the SiO_2 blocking layer, as illustrated in Fig. 9(a). To achieve non-charge-storage-based operation through oxygen ion exchange, the gate oxide should not be electrically charged upon application of the gate voltage. In this device, the n^+-Si substrate was used as the bottom gate and a 100-nm-thick thermally-grown SiO_2 layer was used as a thick blocking layer. The output and transfer curves shown in Fig. 9(b) and **9(c)**, respectively, consistently show negative charging of the gate oxide, which results in reduction of I_{DS} upon repetition of the output measurements and clockwise hysteresis in the transfer curves. Because the IZO channel and the HfO_{2-x} gate oxide are in direct contact, exchange of oxygen ions between them may occur upon gate bias application, as shown schematically in Fig. 9(a). Although the oxygen ions could migrate from the IZO to the HfO_{2-x} gate oxide upon application of $+V_{GS}$, the electrons could not escape through the thicker SiO_2 blocking layer. As a result, negative charges are accumulated inside the HfO_{2-x} gate oxide that causes an electric field to build up and impede any further migration of the oxygen ions. Instead, the negative charging of the gate oxide reduces I_{DS} and causes a positive shift in V_T, similar to that observed in Fig. 8. Comparison of these results with those from the HfO_{2-x}/IZO TFT-memory clarifies that the changes in I_{DS} in the HfO_{2-x}/IZO TFT-memory come from the exchange of oxygen ions that occurs between the IZO channel and the HfO_{2-x} gate oxide and from the escape of the electrons to the gate. Besides oxygen ions, protons and moisture could be incorporated in the layers. Indeed, because protons are mobile and donor species in the IZO, their

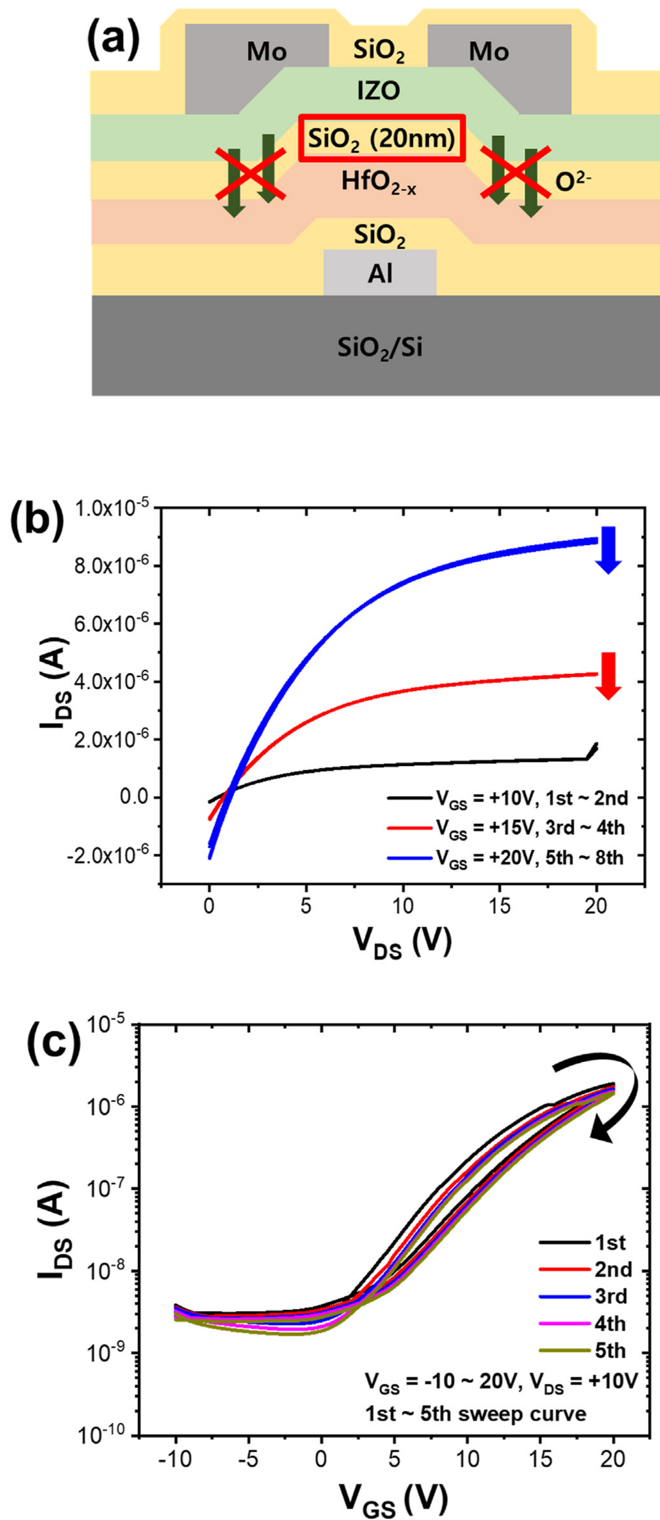

Fig. 8. (a) Schematic illustration of the reference device with a thin SiO_2 layer inserted between the HfO_{2-x} gate oxide and the IZO channel layer, (b) its output curves, and (c) its transfer curves.

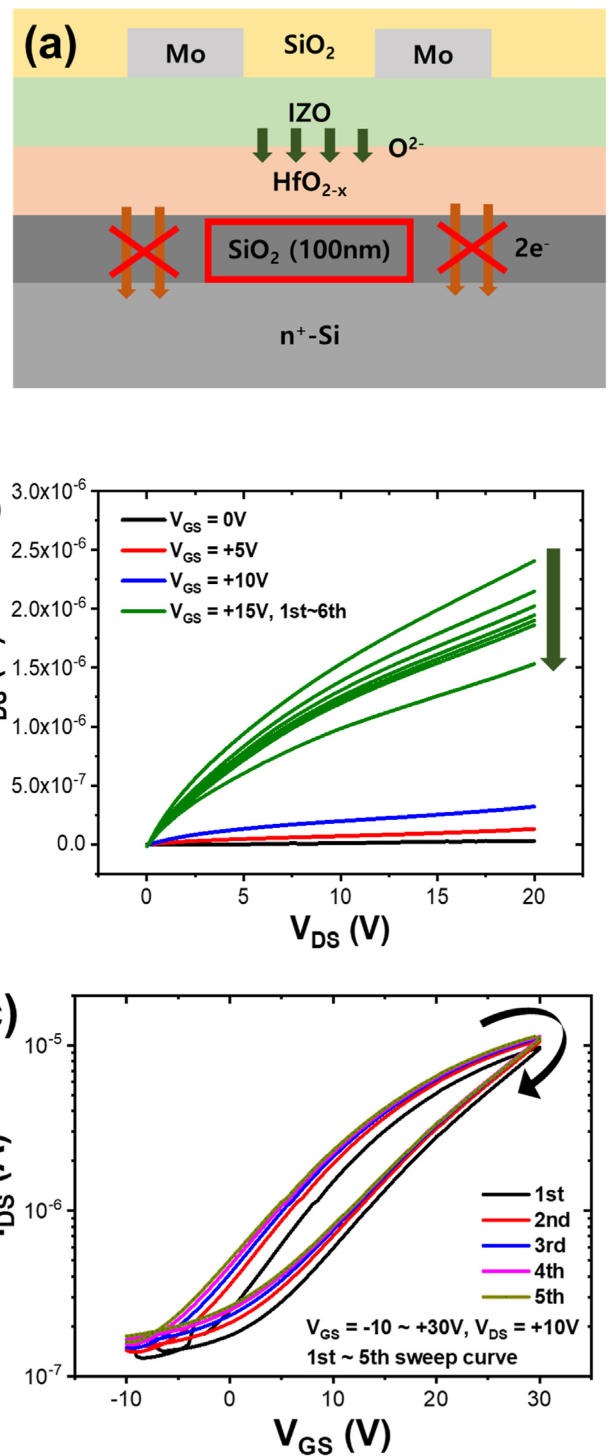

Fig. 9. (a) Schematic illustration of the reference device with the thicker SiO_2 blocking layer between the HfO_{2-x} gate oxide and the Al gate, (b) its output curves, and (c) its transfer curves.

redistribution may change the conductance. However, the reference device in Fig. 9 with a thick SiO_2 blocking layer did not show the same conductance change to that of main device although it has a direct contact between IZO and HfO_{2-x}. In addition, proton redistribution would not change the gate oxide capacitance shown in Fig. 5. These results indicate that the effect of proton and moisture incorporation on the device performance was not significant. The comparison also implies that the I_{DS} change is driven by oxygen ion exchange as a non-charge-storage-based operation, in contrast to the use of the V_T shift caused by electrical charging in conventional flash memory operation.

The conductance modulation by oxygen ion exchange is thought

to be applicable to the devices using various oxides systems if the oxide layers are prepared to enable oxygen ion exchange. For example, we have previously reported the conductance modulation in the devices using HfO_{2-x}/ZnO deposited by atomic layer deposition [8], TaOx/IGZO deposited by sputtering [22], and TaOx/nitrogen-doped IGZO systems [23]. These consistent results showing the conductance change in various defective oxides supportsupport the mechanism of the non-charge-storage-based memory operation with conductance change by oxygen ion exchange between defective gate insulator and oxide semiconductor channel layer.

4. Conclusion

The HfO_{2-x}/IZO TFT-memory proposed in this work exhibited nonvolatile and reversible changes in I_{DS} with respect to the polarity of the applied V_{GS}. In contrast to conventional flash memory operation, which the increase in V_T is caused by electron charging in the floating gate upon application of $+V_{GS}$, the device presented here showed an increase in I_{DS} with reduced V_T as a result of oxygen ion migration from the IZO channel to the HfO_{2-x} gate oxide, which led to an increase in the n-type doping concentration in the IZO channel. Application of $-V_{GS}$ caused the oxygen ions to migrate in the opposite direction, resulting in a reversible reduction in I_{DS}. The exchange of the oxygen ions can be eased by an oxygen deficiency in the sub-stoichiometric HfO_{2-x} gate oxide and the existence of large numbers of oxygen vacancies in the IZO channel that provide oxygen migration sites. A memory window with the changes in I_{DS} $> 10^3$ could be obtained and this window remained stable over time and upon repeated operations. Unlike the HfO_{2-x}/IZO TFT-memory, a reference device with a thin SiO_2 layer inserted between its IZO channel and the HfO_{2-x} gate oxide layers showed only the increase in V_T caused by electron charging because the inserted SiO_2 layer blocked the migration of the oxygen ions. Additionally, a second reference device with a thicker SiO_2 blocking layer between the HfO_{2-x} gate oxide and the gate electrode showed a similar increase in V_T caused by negative charging because the electrons could not escape from the HfO_{2-x} gate oxide to the gate electrode. These results clarified the mechanism for the proposed HfO_{2-x}/IZO TFT-memory characteristics associated with oxygen ion exchange between the gate oxide and the channel layer and confirmed the potential of the proposed device for non-charge-storage-based nonvolatile memory applications.

Credit author statement

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Declaration of competing interest

The authors declare no conflict of interest.

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