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Nonvolatile memory devices based on organic field-effect transistors

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Among the many possible device configurations for organic memory devices, organic field-effect transistor (OFET) memory is an emerging technology with the potential to realize lightweight, low-cost, flexible charge storage media. In this feature article, the recent progress in the classes of OFET-based memory, including floating gate OFET memory, polymer electret OFET memory, ferroelectric OFET memory and several other kinds of OFET memories with unique configurations, are introduced. Finally, the prospects and problems of OFETs memory are discussed.

organic nonvolatile memory, organic field-effect transistors, floating gate, ferroelectric, organic electret

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Organic electronics have been the subject of intense research during the last two decades because of their remarkable advantages such as the realization of low fabrication cost, large area, flexible devices that are not feasible to produce using standard inorganic electronics [1–4]. Organic devices such as organic filed effect transistors (OFETs) [5–7], organic light emitting diodes (OLEDs) [8], organic photovoltaic cells [9], chemical and photo sensors [10,11], are potential candidates for future flexible electronic-device applications. Organic nonvolatile memory is another emerging research field and a key area of application that exploits the advantages of organic materials [12–20], and great progress has been achieved in this field in the last few years. Recently, several types of memory devices based on organic and polymeric materials have been reported, including organic electrical bistable devices [12–16], organic-inorganic hybrid memory using a polymeric fuse [17], and a memory cell based on OFETs [18]. Among the many possible device configurations for organic memory, OFET-based memory is considered a promising candidate for realization of organic memory because of its nondestructive read-out, complementary integrated circuit architectural compatibility, and single transistor realization [19]. Recently, Sekitani et al. fabricated nonvolatile memory arrays containing 676 organic floating-gate transistors arranged in a 26×26 grid on a plastic film with a thickness of 125 μm that can withstand more than 1000 program/erase cycles [20]. Guo et al. reported OFET multibit storage devices based on pentacene or copper phthalocyaine (CuPc), which were fabricated using polystyrene (PS) or polymethylmethacrylate (PMMA) modified SiO_2 as dielectric layer through light-assisted programs [21]. The devices showed excellent multibit storage ability and the retention times were more than 250 h. Both of these were examples significantly progress the research of OFET memory. Although the performance of OFET memory is still not comparable with that of other types of organic memories or silicon counterparts, they show tremendous potential for future applications. In this feature article, we review the recent progress in classes of OFET-based memory including floating gate, polymer electret, ferroelectric and several other types of OFET memories with unique configurations.

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1 Parameters used to characterize OFET memory

There are several parameters used to characterize an OFET memory, such as the operating voltage, memory window, program/erase speed, retention time and endurance. The operating voltage of an OFET memory is expectative below about 10 V because of the desire of low-power IC designs; in addition, the reliability of the memory will decrease when the operating voltage is high. The memory window distinguishes the information storage level. For OFET memory, the memory window is defined as the threshold voltage (V_{th}) shift between the different charge storage states. The magnitude of the memory window will affect the accuracy of the data read. The program/erase speed is defined as the minimum time required to program/erase the device. At the present time, the program/erase speed is still in the order of micro to milliseconds. The retention time is another important parameter for memory. A retention time of more than 10 years at room temperature is desirable, but most organic non-volatile memory devices do not achieve this. The retention time can be improved by optimizing the circuits design. Endurance is the ability of the memory device to withstand repeated program/erase cycles. For non-volatile memory devices, the required endurance is about 10^6 cycles, but this is seldom achieved for organic devices at present.

2 Floating gate OFET memory

A floating gate transistor is a field-effect transistor with two gate electrodes. In addition to the control gate, similar to that in a regular transistor, it has a floating gate embedded in the gate dielectric. When the dielectric is thin enough, electronic charge can be moved onto the floating gate by quantum tunneling or thermal emission when a sufficient program voltage is applied between the control gate and the source contact. Charging the floating gate changes the V_{th} of the transistor because the charge on the floating gate partially screens the electric field between the control gate and the semiconductor. This V_{th} shift can be detected by measuring the drain current at a certain gate-source voltage. Because the floating gate is completely isolated by the dielectric, charge stored on the floating gate remains there without the need for any applied voltage (non-volatile memory). To erase the memory, a voltage of opposite polarity is applied, discharging the floating gate through the dielectric. Silicon-based floating gate transistors are excellent for high-density data storage and have been used for practical applications [22]. However, organic floating gate transistors are more attractive because of their potential applications in low-cost, large-area, and flexible devices. Figure 1 shows a schematic diagram of a typical floating gate OFET memory fabrication process and Figure 2 shows the main parameters

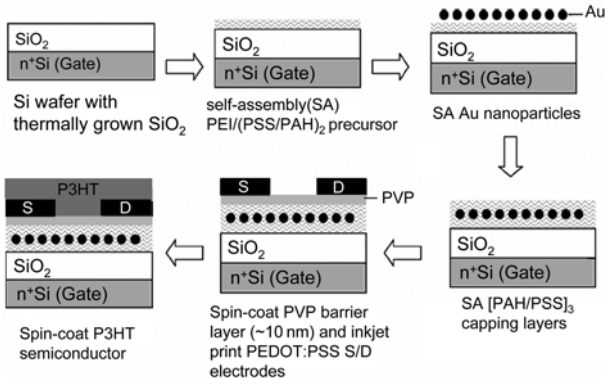

Figure 1 Schematic diagram of a typical floating gate OFET memory fabrication process flow [23].

of OFET memory. In 2006, Liu et al. proposed an OFET memory with self-assembled gold nanoparticles embedded in the gate dielectric [23]. The transistor was fabricated on a heavily doped n-type silicon (n+-Si) substrate containing a thermally grown oxide layer with a thickness of 100 nm. N^+-Si serves as the gate electrode while the oxide layer functions as the gate dielectric. The gold nanoparticles behave as the floating gate for charge storage, and were deposited on the gate oxide by electrostatic layer-by-layer self-assembly method. A self-assembled multilayer of polyelectrolytes, together with a thin spin-coated poly(4-vinyl phenol) (PVP) layer, covers the gold nanoparticles and separates them from the poly(3-hexylthiophene) (P3HT) channel. The memory transistor has an on/off ratio of over 1500 and a data retention time of about 200 s. Recently, Kim et al. used PMMA as a tunneling dielectric layer; the resulting memory devices exhibited a maximum memory window of 34 V with a programming voltage of 80 V [24]. The data retention measurements suggested that the memory properties could be maintained for more than 1 year. Both of these memories used an organic/inorganic hybrid structure. Our group reported an all-organic memory device based on CuPc thin-film transistors using a polyimide gate dielectric containing embedded gold nanocrystals that exhibited a memory window of 20 V [25]. Most examples of OFET memory require large program and erase voltages. Such high voltages are incompatible with low-power IC designs. A solution to lower the program and erase voltages is to use high-k dielectrics. Chang et al. fabricated an OFET memory device containing HfLaO (20 nm), HfON (20 nm), and HfO_2 (6 nm) as blocking, charge trapping, and tunneling gate insulator layers, respectively [26]. The devices showed a low program/erase voltage of 12 V, a speed of 1/100 ms, an initial memory window of 2.4 V, and a 0.78 V memory window after 48 hours. Recently, Sekitani et al. have developed flexible floating gate transistors with small program and erase voltages (–6 V to +3 V) and is one of the best results reported to date for floating gate OFET memory [20]. The control and floating gates

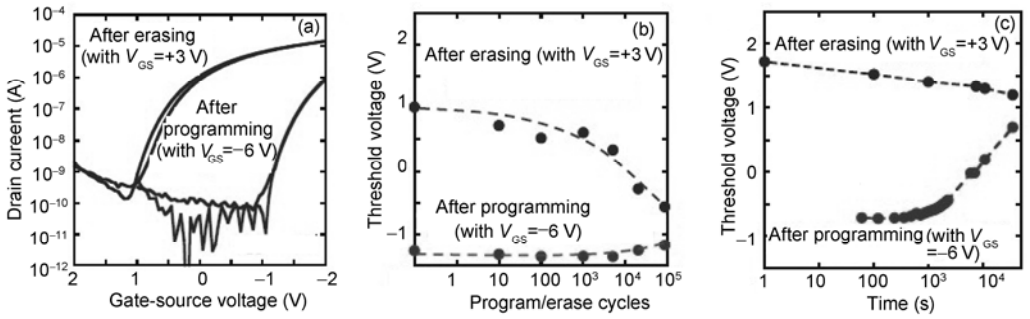

Figure 2 Main parameters of an OFET memory [20]. (a) Reversible shifts in the transfer curves of the memory devices after application of a gate bias; (b) endurance of the memory transistors; (c) retention characteristics of the memory transistors.

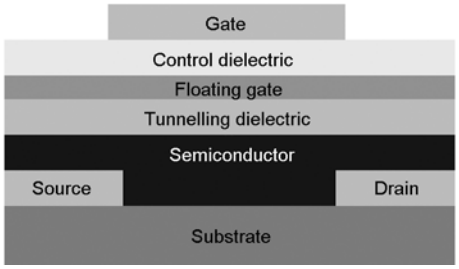

Figure 3 Schematic diagram of a device configuration for top-gate floating gate OFET memory.

were layers of evaporated aluminum with a thickness of 20 nm, the top and bottom dielectrics are both a combination of an aluminum oxide (AlO_x) layer (4 nm thick) grown in oxygen plasma at room temperature and an alkylphosphonic acid self-assembled monolayer (SAM) (2 nm thick) prepared from solution at room temperature. Top gate OFETs provides significant advantages over other device structures, such as autoencapsulation of relatively sensitive organic semiconductors by depositing the gate electrode and gate dielectric on top, and reduction of the contact resistance for charge injection from the source/drain electrodes into the semiconductor. A schematic diagram of a device configuration for top gate OFET memory is shown in Figure 3. Recently, Wang et al. realized a memory effect using a top gate configuration by inserting a layer of nanoparticles (such as Ag or CaF_2) as the floating gate between two Nylon 6 gate dielectrics [27]. Baeg et al. achieved a top gate OFET memory with good performance by embedding gold nanocrystals at the interface between a layer of PS and a layer of cross-linked PVP that were used as charge injection and current blocking gate dielectrics, respectively [18]. Therefore, top gate OFET memory is an alternative way to realize organic memory devices.

3 Polymer electret OFET memory

Hysteresis has been observed in the operation of OFETs upon cycling of OFETs containing nonferroelectric polymer gate dielectrics. In addition, highly ordered active semiconductor films can be obtained and high performance OFETs can be realized. Therefore, it is important to develop high performance OFET memory based on electrets. Figure 4(a) shows the basic device configuration of polymer electret OFET memory and the chemical structures of some common polymer electret materials are shown in Figure 4(b). In 2004, Singh et al. reported the first OFET memory elements containing an electret as the gate insulator [28]. Polyvinyl alcohol (PVA) was used as the gate insulator and fullerenes as molecular semiconductors. An amplification of the drain-source current (I_{ds}) in the order of 10^4 was observed upon application of a gate voltage, as well as a large shift of 14 V in V_{th} and a retention time of 15 h. They proposed that the observation of a switchable current originated from charge storage in the organic electret. More recently, some polymer electret OFET memory devices were realized using polymer modified SiO_2 as the gate insulator. A possible mechanism for the operation of the memory devices is shown schematically in Figure 5. When mobile carriers are field generated near the interface in the semiconductor, they are transferred to the polymer/SiO_2 interface by the transverse electric field. A reverse voltage sweep caused carriers to tunnel from the polymer/SiO_2 interface to the active semiconductor layer [19,29]. Consequently, reversible shifts in V_{th} can be observed. Baeg et al. developed a type of OFET memory containing a SiO_2 gate insulator that was modified with a thin layer of poly(α-methylstyrene) (PαMS), which acts as a polymeric gate dielectric [19]. This OFET memory device showed a large memory window of

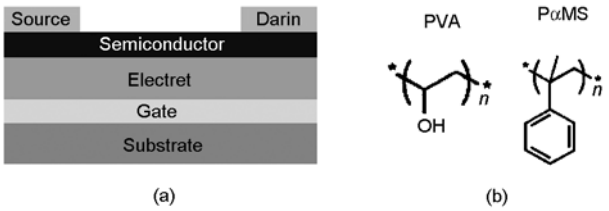

Figure 4 (a) Schematic diagram showing the device configuration of an electret OFET memory; (b) chemical structures of some common polymer electret materials.

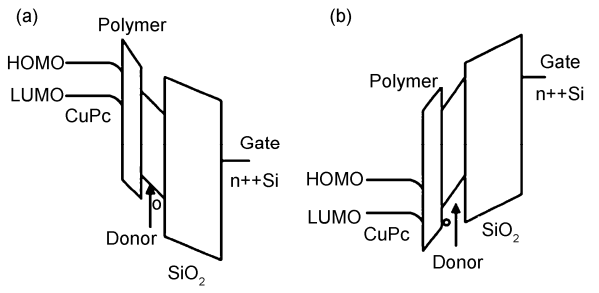

Figure 5 Schematic energy-band diagrams of memory structures under (a) program and (b) erase modes [29].

about 90 V, a high on/off ratio of 10^5, and a long retention time of more than 100 h. These memory characteristics were obtained only when an appropriate polymeric gate electret layer (e.g., PαMS) was inserted between the semiconductor and SiO_2 gate insulators in the OFET structure. Recently, Wu et al. reported high performance OFET memory elements with steep hysteresis loops using donor-polymer-blend buffer layers containing a donor-polymer blend on a SiO_2 gate insulator [29]. For comparison, the compounds tetrathiafulvalene (TTF), ferrocene (Fc) and 5, 10, 15, 20-tetra-phenyl-21H, 23H-porphine nickel (II) (NiTPP) were chosen as donors, while poly (ethylene oxide) (PEO), PS, polycarbonate (PC), and PMMA were used as the blend matrix (Figure 6(a) and (b)). These devices exhibited steep hysteresis loops with an on/off memory ratio of up to 2×10^4, and a retention time greater than 24 h. A low operational voltage is essential for practical applications. To achieve a low operating voltage, OFET devices were fabricated containing polymer dielectrics (cross-linked PMMA, with 1,6-bis(trichlorosilyl)hexane as a

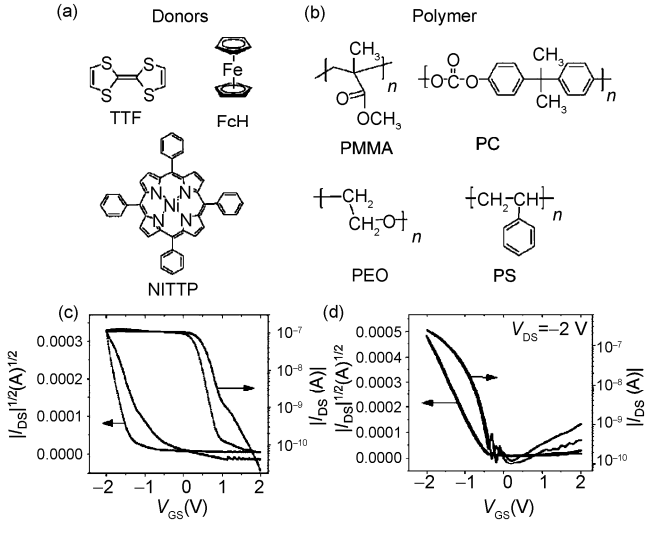

Figure 6 Chemical structures of (a) donor molecules and (b) polymers for blended organic memory transistors; (c) typical transfer characteristics of memory devices containing a cross-linked polymer as the dielectric; (d) transfer characteristics of a control device lacking a donor/polymer blend buffer layer [29].

cross-linking agent) and a donor/polymer blend buffer layer, which showed memory characteristics with a reduced operating voltage of less than 2 V (Figure 6(c)). This is one of the lowest operating voltages attained for OFET memory to date.

For memory cells, the traditional means of achieving a low cost per bit is by scaling down their size or having multilevel storage, and great developments have been achieved in these areas [30,31]. Multibit storage is attracting an increasing amount of attention because scaling is limited by photolithography. Recently, Guo et al. developed OFET memories with multibit storage ability [21]. The multibit storage OFETs based on pentacene or CuPc were fabricated using a SiO_2 modified with PS or PMMA dielectric layer through light-assisted programs. Figure 7(a) shows transfer curves for the pentacene-based OFETs containing a PS modified SiO_2 dielectric layer under irradiation with 1 mW cm^{-2} of visible light. V_{th} and the magnitude of the field-effect onset voltage are strongly related to the starting value of the sweeping gate voltage. When a positive gate voltage increases from 20 to 80 V, V_{th} and the onset voltage changed by more than 55 V. Meanwhile, the stored holes can still be erased by the light-assisted program. Shown in Figure 7(b) are the retention characteristics of the four states. The retention time was greater than 250 h, which is one of the best achieved for OFET memories. After further investigation and optimization, multibit storage OFETs can potentially be applied in low-cost, lightweight systems.

4 Ferroelectric OFET memory

Most of the organic memory transistors reported to date exploit the electric field induced remnant polarization in ferroelectric polymer films [32–45]. Inorganic ferroelectric FET memories have been studied for decades; a memory performance of practical value has been achieved in recent years [46,47]. Its functionality arises from the attenuation of the charge carrier concentration in the semiconductor by ferroelectric polarization of the gate insulator; even when the applied electric field or voltage is removed, there are still residual polarization charges in the ferroelectric film. As shown in Figure 8, typical hysteresis loops can be obtained for a ferroelectric film capacitor at several voltages. Figure 9(a) shows a schematic diagram of the device configuration for ferroelectric OFET memory; shown in Figure 9(b) are the chemical structures of some common organic ferroelectric materials. In 2001, Velu et al. reported an OFET memory device comprised of an active layer of sexithiophene and a ferroelectric gate insulator of Pb (Zr, Ti) O_3 or PZT [32]. Although the performance of this device was not good, since then, ferroelectric OFET memories have attracted extensive attention. In 2004, Schroeder et al. developed OFET memories using gate insulators containing the amorphous, ferroelectric-like material poly(*m*-xylylene adipamide) (MXD6). These devices have an on/off ratio of

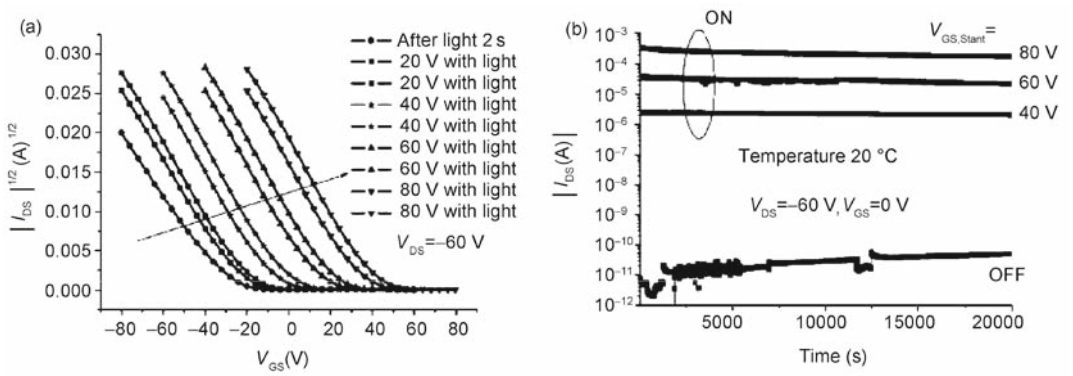

Figure 7 (a) Transfer curves of different light-assisted programs ($V_{GS, Start}$=20, 40, 60, and 80 V, V_{DS}=–60 V under visible light emission); (b) current based on V_{DS} =–60 V and V_{GS} =0 V with light-assisted start scanning of $V_{GS,Start}$=40, 60, and 80 V and V_{DS} =–60 V (on state), and $V_{GS,Pro}$=–150 V, V_{DS} =0 V, and t=1 μs (off state) without light at room temperature [21].

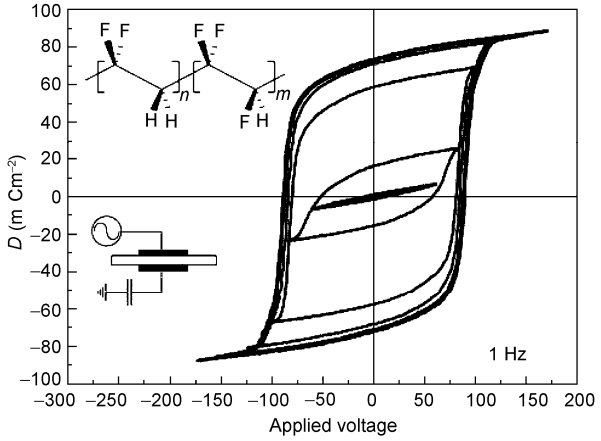

Figure 8 Ferroelectric hysteresis loops of a P(VDF/TrFE) polymer capacitor device [34].

200 at a gate bias of 2.5 V, one of 30 at zero gate bias and a retention time of three hours [33]. In 2005, Naber et al. fabricated ferroelectric OFET memory devices containing the ferroelectric copolymer poly(vinylidene fluoride/trifluoro- ethylene) (P(VDF/TrFE)) as a gate insulator and poly[2-methoxy, 5-(2′-ethyl-hexyloxy)-p-phenylene-vinylene] as a semiconductor [34,35]. The devices had an on/off ratio of 10^4, with a programming time of 0.3 ms and a memory stability of more than 1 week. Most of the recent ferroelectric OFET memories have used MXD6 or (P(VDF/TrFE)) as ferroelectric dielectrics [36–45]. Nonetheless, critical problems remain to be overcome prior to any practical application of this ferroelectric polymer for nonvolatile OFET memory on flexible plastic or glass substrates. These include its low field mobility (less than ~10^{-2} cm^2 V^{-1} s^{-1}) and the high current leakage from thin ferroelectric films. Fortunately, Lee et al. reported ferroelectric OFET memories based on pentacene with P(VDF-TrFE) films as dielectric layer, which were cured at 160°C for 2 hours in a vacuum oven and then subsequently cooled to room temperature under a stream of N_2 gas [39]. The devices demonstrated a maximum mobility

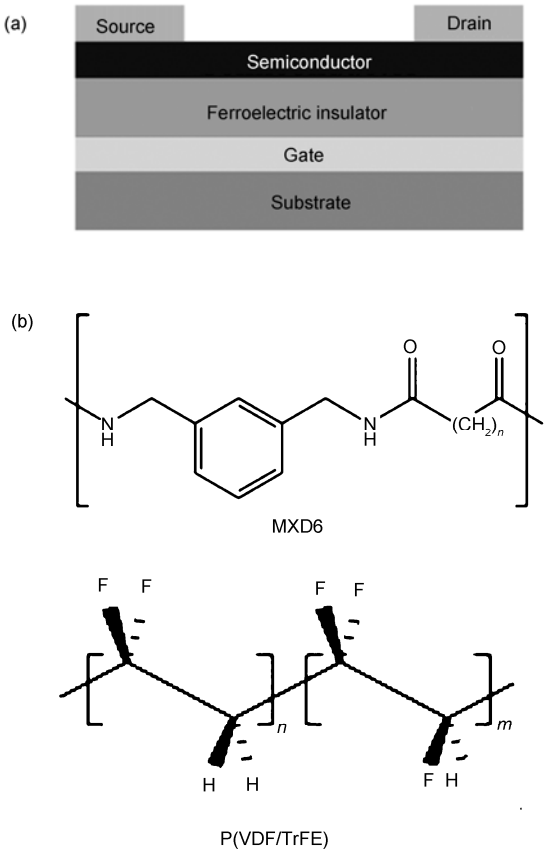

Figure 9 (a) Schematic diagram shows the device configuration of a ferroelectric OFET memory; (b) chemical structures of some common ferroelectric materials.

of 0.18 cm^2 V^{-1} s^{-1} and a large memory window of 2.5–8 V under a minimum write-erase switching voltage of ±13 V, and also exhibited good retention properties. Tremendous progress has been made in the field of ferroelectric OFET memories in recent years, but there is still a lot of work to do towards the practical application of nonvolatile ferroelectric OFET memories.

5 Several other types of OFET memories with unique configurations

In addition to the above kinds of OFET-based memory, several other configurations have been used for memory devices. In 2007, Scharnberg et al. proposed a technique to adjust V_{th} of an OFET using a design similar to a dual-gate structure with an insulating Teflon based electret layer as a second gate, as shown in Figure 10(a). The Teflon film was formed by thermal evaporation and charged using corona discharge to form an electret. The electret layer was used as a second gate and can be used to shift the V_{th} of the transistor. The V_{th} of a pentacene bottom gate OFET was shifted from +13.1 to −2.3 V by deposition of a Teflon encapsulating layer. An additional advantage of this technique is that after the electret has been charged there is no further need for an active power supply because the electret is charged permanently. Furthermore, because the charges are trapped permanently in the electret, there is no leakage of current through the top gate dielectric, which is a problem for conventional top gates [48]. Guo et al. reported an OFET based on CuPc with an inserted layer of molybdenum oxide (MoO_3), as shown in Figure 10(b) [49]. The OFETs containing the MoO_3 layer exhibited a memory effect, with large reversible shifts in V_{th} of about 40 V, an on/off ratio exceeding 10^3, and a long retention time. It was suggested that the inserted MoO_3 layer does not affect the charge injection and transport in the devices. When a large positive gate voltage is applied, the thin MoO_3 layer can generate holes and electrons. Thus, the interface between the CuPc and MoO_3 layers helped to store electrons because of the poor electron transporting ability of CuPc and the traps formed on the MoO_3 surface. When V_G is removed, the electrons are stored at the MoO_3 surface, behaving as a "floating gate" that can induce a large number of holes. Therefore, the operating model changes from an enhancement model into a depletion one, and a large V_{th} shift is generated. In 2008, Novembre et al. developed an organic memory device based on a pentacene-gold nanoparticles active layer. Gold nanoparticles were immobilized on the silicon dioxide of pentacene transistor using an amino-terminated SAM [50]. Under appropriate writing and erasing pulses on the gate, a large V_{th} shift of 22 V and an on/off drain current ratio of 3×10^4 were obtained. Recently, Mabrook et al. fabricated devices containing PMMA as gate insulator (Figure 10(c)) that exhibited good charge retention properties [51]. The operating mechanism of the devices is as follows: when a negative gate bias is applied, holes are injected from the pentacene layer into the nanoparticle layer, charging the nanoparticles and programming the memory device. In contrast, when a positive gate voltage is applied, holes are ejected from the nanoparticle layer through the pentacene layer resulting in an erase process. These special configuration OFET memories provide more options for memory applications.

6 Applications and prospects of OFET memory

OFET memory devices have great potential for memory applications such as in radio-frequency identification (RFID) devices, smart cards and disposable circuitry. Organic memory tags are the backbone of RFID systems since they contain data that allow the items to be identified. An organic memory tag is made of a nonvolatile memory associated with a radio frequency communication block, performing RF-signal modulation antenna. Promising OFET-based RFID tags that operate at 13.56 MHz were developed in 2007. In 2009, Sekitani et al. developed OFET memory arrays for flexible sensor arrays [20]. The sensor was fabricated by laminating three sheets: a polyethylene naphthalate (PEN) sheet containing 676 two-transistor memory cells arranged in a 26×26 array (Figure 11(a)), a pressure sensitive rubber sheet, and a PEN sheet with a copper electrode. Shown in Figure 11(b) is a photograph of the three individual sheets before lamination. By applying a program voltage to the copper electrode and an access voltage to all of the memory cells, the copper electrode supplies the program voltage to the floating-gate transistors in the positions where pressure is applied, and the pressure distribution is stored in the memory array. Figure 11(c) shows a demonstration of the sensor. Pressure was applied using two different objects: a roll of tape and two fingers. The stored information was read out after 20 min and again after 12 hours using a multichannel drive system.

Tremendous progress has been made in the field of

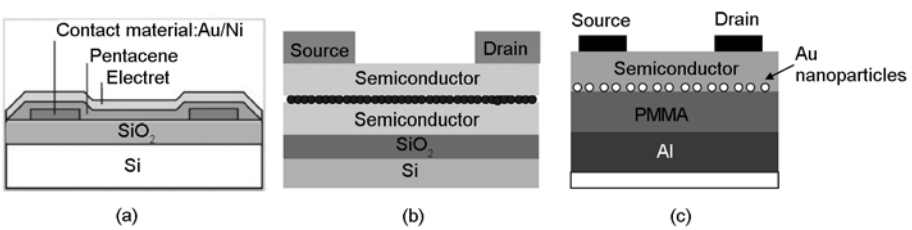

Figure 10 (a) Schematic diagram of an OFET containing an electret encapsulating layer; (b) cross-section of an OFET with a MoO_3 inserted layer; (c) schematic diagram of gold nanoparticle-pentacene memory transistors.

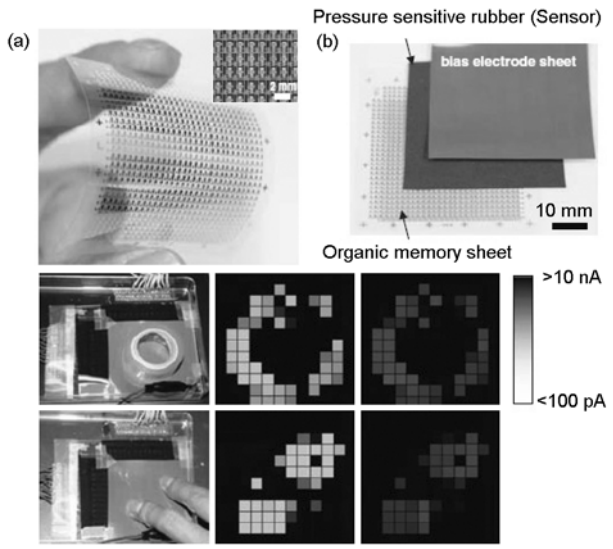

Figure 11 (a) Photograph of an organic floating-gate transistor sheet comprising 26×26 memory cells; (b) photograph of the three individual sheets before lamination, bottom, 125 μm-thick PEN sheet with 676 two-transistor memory cells; center, 500 μm-thick pressure sensitive rubber sheet; top, 125 μm-thick PEN sheet with copper electrodes; (c) demonstration of the sensor array [20].

OFET memories since it was first described. Currently, OFET memories exhibiting operating voltages of about 2 V, more than 10^3 program/erase cycles, and retention times of a few hundred hours have been achieved. In addition, OFET memories integrated with other electronic elements have been reported. OFET memories have great potential for application in low cost, large areas, plastic systems, but many challenges still remain. These include: program/read/erase voltages are still large; data retention times are too short to satisfy the requirements of practical applications; operating mechanisms of OFET memories are not clearly understood. All of these issues need to be addressed in the future to aid the design of high performance devices. OFET memories have received extensive attention and promise attractive application prospects. It is hoped that further research will successfully resolve the problems that OFET memories are currently encountering, allowing their wide use in organic electronics.

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