Normally-off logic based on resistive switches – Part II: Logic circuits

S. Balatti, *Student Member, IEEE*, S. Ambrogio, *Student Member, IEEE*, D. Ielmini, *Senior Member, IEEE*

***Abstract*—Logic gates based on the resistive switching memory (RRAM) allows for normally-off digital computing thanks to the nonvolatile nature of the RRAM switch [1]. An extremely small area consumption can be achieved thanks to the 2−terminal structure of the RRAM switch and its capability of 3D stacking. However, the RRAM organization details within the array must be thoroughly investigated. This work discusses the array organization and the select/unselect schemes of RRAM logic circuits. We demonstrate a 1-bit adder to support the high functionality of RRAM logic. These results support RRAM as a promising technology for nonvolatile logic circuits beyond CMOS.**

Keywords: Resistive switching memory (RRAM), logic gates, logic circuits, logic computing

I. Introduction

Resistive switching memory (RRAM) is raising an increasing interest for high-density nonvolatile memories [2]–[5] and logic circuits [1], [6]–[8]. The crossbar latch was first proposed to allow inversion and restoration within diode logic circuits [9]. Material implication (IMP) gates were then introduced using a network of parallel RRAM switches [6] or a complementary resistive switch [8]. In the companion paper, we showed that two serially-connected RRAM switches are capable of AND, NOT or IMP operations [1]. Other logic functions, such as OR and XOR, can be achieved with more RRAM switches and multiple steps. In RRAM logic, the input state is contained as the initial state of the RRAM switch, while the output is the final state of one or both switches [1], [6]. The network of passive RRAM switches is driven by a peripheral circuit of CMOS devices allowing for selection/deselection and application of voltage pulses needed to accomplish each operation [1].

To validate and further explore this CMOS/RRAM hybrid approach to logic computing, however, the details of the circuit implementation must be addressed. The circuit architecture of choice for RRAM switches is the crossbar array, where each RRAM device is located between a row and a column [10]. The minimum device size in this configuration is only $4F^2$, where F is the minimum feature size which can be achieved by optical lithography. Crossbar stacking was also demonstrated in the literature, which translates in an even smaller device size of $4F^2/n$, where n is the number of stacked layers [10], [11]. Thanks to the small size of the individual switch in the crossbar array, the RRAM logic circuits can achieve extremely high density, *e.g.*, only $2F^2$ for an AND gate, which is more than 100 times smaller than a typical logic gate in CMOS technology [1], [12]. To assess the actual size and performance of RRAM logic circuits, however, the array organization and disturb must be studied.

S. Balatti, S. Ambrogio and D. Ielmini are with the Dipartimento di Elettronica e Informazione and Italian Universities Nanoelectronics Team (IU.NET), Politecnico di Milano, piazza L. da Vinci 32, 20133 Milano, Italy. E-mail daniele.ielmini@polimi.it

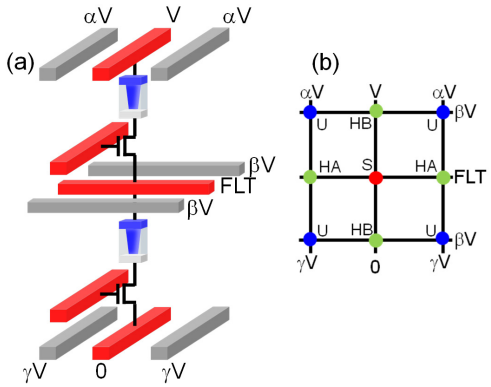

Fig. 1. Schematic view of 2 stacked arrays with 1T1R architecture (a) and corresponding plan view (b). The selected columns are biased at V and 0, while the unselected at αV and γV. The selected row is floating and the unselected rows are biased at βV. Depending on its position in the array a cell can be selected (S), unselected (U) or half selected (HA and HB).

This work demonstrates logic computation in RRAM crossbar circuits through simulations and experiments. First, the select/unselect scheme for disturb-free logic operation in 2 stacked crossbar arrays will be discussed. Two architectures will be considered, where transistors and/or resistances are used as select elements in the array. The wordline/bitline bias for select/unselect will be discussed for both architectures. Finally, 1-bit addition in an 11-RRAM circuit with 7 clock pulses will be demonstrated by experiments and simulations.

II. 1T1R crossbar implementation

Our general implementation consists of 2 stacked crossbar arrays, each array being a periodic sequence of rows and columns with a RRAM switch located between each row and column. The intermediate rows are shared between the top and the bottom crossbar arrays [10]. The stacked structure allows to naturally implement the serial-RRAM structure of the logic gate [1]. Here it is possible to either independently access individual cells within each crossbar array, *e.g.*, for the write operation, or access any given logic gate by applying a voltage V to the top column with grounded bottom column and floating intermediate row, to perform any given logic operations [1].

Fig. 1a illustrates one possible array implementation of RRAM logic, where RRAMs in both the top and bottom crossbars are accompanied by a select transistor in the so-called

one-transistor/one-resistor (1T1R) structure. Only the selected RRAM gate is shown in all schemes, where a simple logic operation, *e.g.*, AND, is carried out. While the scheme in Fig. 1a is totally agnostic with respect to the specific integration approach, the select transistor might be thought as a vertical gate-all-around (GAA) transistor, similar to the upper select gate and bottom select gate in 3D Flash architectures [13], the one-transistor/one-capacitor DRAM [14] and the 1T1R structure proposed for phase change memories [15]. With respect to the conventional crossbar approach with passive selector elements (*e.g.*, diodes), the 1T1R with a vertical GAA transistor would require a row/column pitch of 3F instead of 2F, to accommodate the channel width (1F), the gate line space surrounding the channel (1F) and the spacer (1F). Therefore, the estimated single device area is $9F^2$, instead of $4F^2$ of an ideal passive crossbar. Note that, although the use of select transistors increases the occupied area, the area consumption is still much smaller than the corresponding CMOS logic gate. For instance, the 2T2R structure in Fig. 1 allows for AND operation, whereas 4 transistors are needed for the same function in CMOS logic. Also, CMOS logic gates cannot be arranged with an array architecture as shown in Fig. 1, which is at the origin of the small circuit area of RRAM logic.

Fig. 1a also shows a generic bias scheme for logic operation in the selected gate, where a voltage V is applied to the top column, while the bottom column is grounded and the intermediate row remains floating. The voltage V is positive for AND (or transfer) operations, while V is negative for IMP (and NOT) operations. For the sake of simplicity, we assumed that the top and bottom RRAM in the logic gate are located at the same coordinates on the array, although they also might be located at different positions, provided that they share the same intermediate floating row. The input states (set state 0 or reset state 1) are initially stored in the two switches at the selected position in the array. In the following, we will assume that IMP operation takes place by different reset voltages in the top and bottom RRAM switches, namely the bottom RRAM switch (P) has a relatively large reset voltage V_{reset}, while the top RRAM switch (Q) has a small reset voltage V^*_{reset} < V_{reset} [1]. The small value of V^*_{reset} causes Q to reset first in the IMP gate, thus allowing to achieve IMP functionality. As discussed in [1], different reset voltages can be obtained by different materials in the RRAM device, *e.g.*, using an electrochemical-type RRAM with Ag or Cu electrode to achieve asymmetric switching with relatively small reset voltage [16].

The logic operation takes place in the selected RRAM switches by applying positive/negative V with appropriate voltages V_{G1} and V_{G2} to the gate of the select transistors to activate the current path across the selected RRAMs. Note that the transistor gate lines are parallel to the columns, and unselected gate lines are left at low voltage to avoid any disturb to the unselected RRAM elements during either write or logic computation. To unselect all other RRAMs in the crossbar arrays, the unselected top columns, intermediate rows and bottom columns must be biased to an appropriate voltage. As shown in Fig. 1a, voltage values αV, βV and γV, with α, β and γ being positive and less than 1, are used to bias the unselected top columns, intermediate rows and bottom columns, respectively. To study the disturb conditions for α, β and γ, four cases can be considered depending on the position of the logic gate as shown in the top-view of the crossbar circuit in Fig. 1b. Each of these cases will be considered in the following subsections.

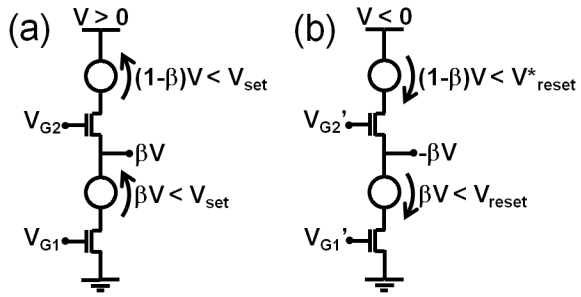

Fig. 2. Generic half-selected gates HB during AND (a) and IMP (b) operation. Note the different gate voltages in (a) and (b), where V_{G1} and V_{G2} are smaller than V'_{G1} and V'_{G2} to properly control the current during the set transition.

A. Selected gate

The selected gate (S in Fig. 1b) is located at the crossing between the top column biased at V and the floated row. The grounded column is assumed exactly below the top column biased at V. Logic switching occurs in S according to the AND and IMP operations [1]. To induce the logic operation the applied voltage must satisfy the following conditions:

$$V_{set} < V < 2V_{set}, \tag{1}$$

for AND operation, and:

$$V > 2V^*_{reset} + 2V_{MOS}, \tag{2}$$

for IMP operation, where the voltage V_{MOS} across the transistor depends on the current I through the equivalent transistor resistance R_{MOS}, namely V_{MOS} = $R_{MOS}I^*_{reset}$. Note that there is no maximum limit for V in Eq. (2): in fact, as soon as reset transition of Q occurs at I^*_{reset}, almost the entire applied voltage drops across Q due to its high resistance, thus protecting P against any disturb. A practical maximum limit of V in Eq. (2) is therefore the breakdown voltage for Q. On the other hand V_{MOS} can be neglected for AND operation in Eq. (1) because I is approximately zero.

B. Unselected gates

The unselected gates (U in Fig. 1b) do not share any row or column with the selected gate. The transistors of these logic gates are non-conducting since the gate voltage is low on all unselected gate lines. Therefore, no disturb can take place on these logic gates.

C. Half-selected gate of type A

The half-selected gate of type A (HA in Fig. 1b) is located at the crossing between a generic unselected column and the selected row. These are not affected by any disturb, since the select transistors are switched off.

TABLE I
PARAMETER VALUES USED TO EVALUATE THE ALLOWED RANGE OF α, β AND γ IN FIG. 3 AND FIG. 6.

Parameter	Value
V_{set}	1.2 V
V^*_{reset}	0.2 V
V_{reset}	0.4 V
V_C	0.4 V
I_C	10 μA
R_{MOS}	20 kΩ
R_S	20 kΩ

D. Half-selected gate of type B

The half selected gate of type B (HB in Fig. 1b) is located at the crossing between the selected column and a generic unselected row. The transistors of these logic gates are conducting since they share the high voltage of the selected logic gates in the top and bottom arrays, respectively. Fig. 2 shows a generic HB gate during AND operation (a) and IMP operation (b), differing by the polarity of the voltage applied to the top column. The gate voltages are also different to ensure proper biasing of the transistors for set (a) and reset (b) operations during AND and IMP, respectively. In the case of AND, disturb should be avoided by ensuring that the voltages across the RRAM switches are both below the set voltage V_{set}. Based on Fig. 2a, this condition reads:

$$1 - \frac{V_{set}}{V} < \beta < \frac{V_{set}}{V}, \tag{3}$$

for AND operation. The condition in Eq. (3) is represented in Fig. 3a as the range of suitable values of β as a function of the applied voltage V during AND operation. In these calculations, the values of V_{set} and V_C shown in Tab. I were assumed. The figure also includes the conditions expressed by Eq. (1) about the minimum and maximum voltages necessary to operate the AND logic gate [1]. Clearly, a large difference between V_C and V_{set} is beneficial to broaden the window of β. The other parameters α and γ, which do not impact the disturb analysis, can be conveniently chosen to be around 0.5.

For IMP operation, both βV and (1-β)V must be smaller than the reset voltage to avoid reset transition in either the top or bottom device of HB. The acceptable β must thus comply with the condition:

$$1 - \frac{V^*_{reset}}{V}\left(1 + \frac{R_{MOS}}{R}\right) < \beta < \frac{V_{reset}}{|V|}\left(1 + \frac{R_{MOS}}{R}\right), \tag{4}$$

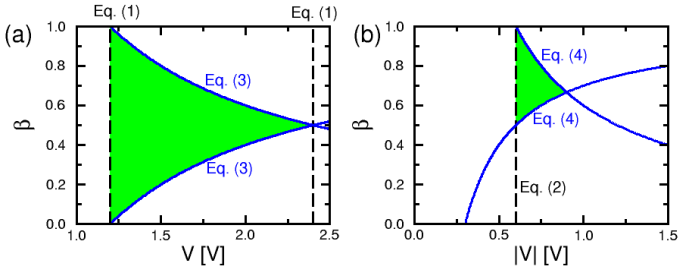

Fig. 3. Range of allowed values of parameter β as function of applied voltage for AND (a) and IMP (b) operations in the 1T1R architecture of Fig. 1. The range is limited by conditions described in Eqs. (1-4).

which is shown in Fig. 3b as the allowed range of parameter β as a function of the absolute value of the voltage V applied in the IMP operation. Also the minimum voltage in Eq. (2) to operate the IMP logic gate is shown in the figure. Assuming the values of V_{set}, V^*_{reset} and V_{reset} in Tab. I, β can be conveniently chosen within the range from 0 to 1 during AND operation and from 0.5 to 1 during IMP operations, depending on the applied voltage. On the other hand, coefficients α and γ are not relevant for disturb, thus a convenient value of α = γ = 0.5 can be assumed.

III. HYBRID 1T1R/1R1R ARCHITECTURE

A simple alternative to the 1T1R structure is the hybrid structure schematically shown in Fig. 4, where RRAM switches are accompanied by a select transistor in the bottom layer, while a passive resistance R_S is used in the top layer for the purpose of current limitation. The transistors in the bottom layer can thus be fabricated as front-end transistors with either horizontal (conventional) or vertical geometry. No transistors in the top layer are needed, thus alleviating the complexity of the crossbar fabrication. The gate lines are parallel to the intermediate rows for convenience of the biasing scheme. As in the full 1T1R architecture, the selected top and bottom columns are biased at V and 0, respectively, while the intermediate row is left floating to allow for conditional switching during AND or IMP operations. Write and read operations in the top crossbar array are achieved by selecting the respective switch through the 1T1R architecture. On the other hand, reading a cell in the top crossbar is possible by first transferring the bit value to the bottom crossbar through a modified AND operation [1], then reading the corresponding bottom RRAM switch. A similar procedure can be used for writing input states in the top crossbar. This allows to avoid direct read/write in the top crossbar array which may be affected by excessive leakage current due to the inefficient selection in the 1R1R architecture.

To study the disturb effect during logic operation in the crossbar array, we considered all cases of unselected and half-selected logic gates as indicated in Fig. 1b.

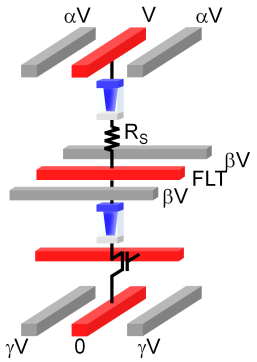

Fig. 4. Schematic view of the alternative structure 1T1R/1R1R. With respect to the 1T1R structure in Fig. 1a, the transistor of the top RRAM is replaced by a resistor R_S for selection and current limitation.

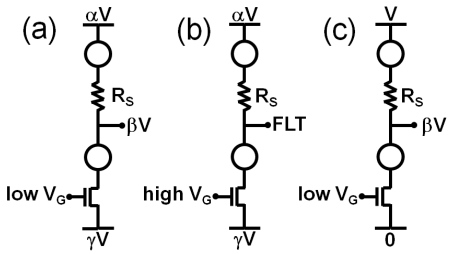

Fig. 5. Bias configuration during logic operation for unselected cell U (a), half-selected cell HA (b) and half-selected HB defined according to Fig. 1b.

A. Selected gate (S)

To induce the logic operation the applied voltage must satisfy the conditions:

$$V_{set} < V < 2V_{set}, \tag{5}$$

for AND operation, and

$$V > 2V^*_{reset} + V_{R_S} + V_{MOS}, \tag{6}$$

where V_{R_S} is the voltage across the series resistance, namely $V_{R_S} = R_S I_{*reset}$, similarly to Eq. (2).

B. Unselected gate (U)

First, we consider the U gates, sharing neither the row nor the column with the selected gate. The bias of the U gate is shown in Fig. 5a: the low gate voltage protects the bottom RRAM from any possible disturb, while the top RRAM case must be studied in detail. To rule out any disturb, the voltage drop across the top cell must be lower than V_{set} and higher than $-V^*_{reset}$, where V^*_{reset} is assumed positive. This condition can be generally expressed as:

$$-V^*_{reset} < (\alpha - \beta)V - R_S I < V_{set}, \tag{7}$$

for IMP operation where V is positive for AND operation and negative for IMP operation, or the current I is assumed positive if it flows from top to bottom. In cases $\alpha > \beta$ for AND operation (V > 0) and $\alpha < \beta$ for IMP operation (V < 0), the voltage across the cell is positive, which may induce a set transition. Since set transition can only take place in state 1, the current I can be neglected, thus Eq. (7) becomes (α - β)V < V_{set}, which considering positive and negative V becomes:

$$\alpha - \beta < \frac{V_{set}}{V} \tag{8}$$

for AND operation, and

$$\beta - \alpha < \frac{V_{set}}{|V|} \tag{9}$$

for IMP operation. On the other hand, assuming $\alpha < \beta$ for AND operation (V > 0) and $\alpha > \beta$ for IMP operation (V < 0), the disturbing voltage is negative, thus may possibly induce reset transition in state 0, where the current is not negligible anymore. Therefore, Eq. (7) becomes (β - α)V < V^*_{reset} - R_SI, which, by noting I = (α-β)V/(R + R_S) and distinguishing between positive and negative V, becomes:

$$\beta - \alpha < \frac{V^*_{reset}}{V}(1 + \frac{R_S}{R}) \tag{10}$$

for AND operation, and:

$$\alpha - \beta < \frac{V^*_{reset}}{|V|}(1 + \frac{R_S}{R})\ (IMP\ operation) \tag{11}$$

for IMP operation.

C. Half-selected gate of type A (HA)

Cells sharing the same row and the same gate voltage as the selected device are biased according to the scheme in Fig. 5b. Disturb might take place in both the top and bottom RRAM, and all possible values of the floating node potential (FLT) should be considered. As worst cases, we consider FLT = 0 and FLT = V in the following, namely the minimum and maximum potential for the floating node. In the case FLT = 0, the voltage across the top RRAM switch should not exceed the set voltage during AND operation or the reset voltage during the IMP operation, which reads:

$$-V^*_{reset} < \alpha V - R_S I < V_{set} \tag{12}$$

which, after considering the different values of the current for set and reset disturbs, becomes:

$$\alpha < \frac{V_{set}}{V} \tag{13}$$

for AND operation, and:

$$\alpha < \frac{V^*_{reset}}{|V|}(1 + \frac{R_S}{R}) \tag{14}$$

for IMP operation. For the bottom RRAM switch, similar conditions apply to prevent disturb, namely:

$$-V_{set} < \gamma V - R_{MOS} I < V_{reset} \tag{15}$$

which, after considering the different operations can be rewritten as:

$$\gamma < \frac{V_{reset}}{V}(1 + \frac{R_{MOS}}{R}) \tag{16}$$

for AND operation, and:

$$\gamma < \frac{V_{set}}{|V|} \tag{17}$$

for IMP operation.

Similar equations are obtained for the case FLT = V. First, the top-RRAM voltage should not exceed either the set or reset voltages according to:

$$-V_{set} < (1 - \alpha)V - R_S I < V^*_{reset} \tag{18}$$

where the set and reset disturb conditions apply to IMP (V < 0) or AND (V > 0) operations, respectively. Eq. (18) can be thus restated as:

$$\alpha > 1 - \frac{V^*_{reset}}{V}(1 + \frac{R_S}{R}) \tag{19}$$

for AND operation, and:

$$\alpha > 1 - \frac{V_{set}}{|V|} \tag{20}$$

for IMP operation. For the bottom RRAM switch, similar conditions apply to prevent disturb, namely:

$$-V_{reset} < (1 - \gamma)V - R_{MOS} I < V_{set} \tag{21}$$

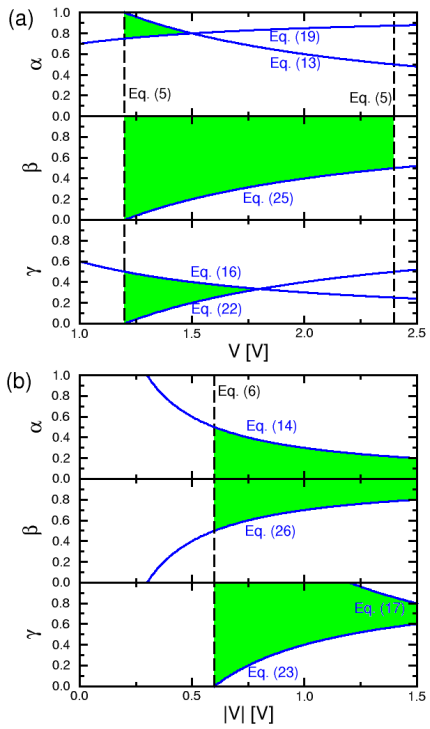

Fig. 6. Range of allowed values of parameters α, β and γ for AND (a) and IMP (b) operations in the 1T1R/1R1R architecture of Fig. 4.

where the set and reset disturb conditions apply to AND (V > 0) or IMP (V < 0) operations, respectively. Eq. (21) can be thus rewritten as:

$$\gamma > 1 - \frac{V_{set}}{V} \tag{22}$$

for AND operation, and:

$$\gamma > 1 - \frac{V_{reset}}{|V|} * (1 + \frac{R_{MOS}}{R}) \tag{23}$$

for IMP operation. Conditions on α and γ in Eqs. (13-23) are included in Fig. 6 for AND operation (a) and for IMP operation (b).

D. Half-selected gate HB

Cells sharing the same column as S are biased according to the scheme in Fig. 5c. The select transistor in the bottom RRAM is in an off state, thus disturb can only take place in the top cell. For this RRAM switch, the voltage should not exceed either the set or reset voltages according to:

$$-V^*_{reset} < (1-\beta)V - R_S I < V_{set} \tag{24}$$

where the set and reset conditions apply to the AND and IMP operation, respectively. These two conditions can be distinguished as follows:

$$\beta > 1 - \frac{V_{set}}{V} \ (AND\ operation) \tag{25}$$

$$\beta > 1 - \frac{V^*_{reset}}{|V|}(1 + \frac{R_S}{R}) \ (IMP\ operation) \tag{26}$$

which are represented in Fig. 6 for AND operation (a) and IMP operation (b).

E. Operating window of α, β and γ

Fig. 6 shows the allowed range of parameters α, β and γ as function of V for AND (a) and IMP (b) operations. Using the values reported in Tab. I, the conditions expressed by Eqs. (8-11) are satisfied irrespective of the applied voltage.

From Fig. 6, the most strict condition is on α during AND operation, where the parameter is limited by V_{set}, V_{reset} and R_S. The window can be increased using a larger value for R_S. This causes also an increase of the other parameters β and γ, although V shift to high voltage for IMP operation due to Eq. (6).

IV. 1-BIT ADDER

To fully support RRAM logic, complex functions such as the 1-bit full adder must be demonstrated [12], [17], [18]. Fig. 7 schematically shows the input/output flow diagram of a 1-bit adder, where input bits A and B are summed with carry-in C_{in}, to yield the output S given by:

$$S = A \oplus B \oplus C_{in}, \tag{27}$$

where $\oplus$ indicates the XOR function. The carry-out bit C_{out} is given by:

$$C_{out} = (A \cdot B) + C_{in} \cdot (A \oplus B), \tag{28}$$

where the AND and OR operations can be replaced by IMP functions, thus leading to:

$$C_{out} = ((A \oplus B) \rightarrow C_{in}) \rightarrow (A \cdot B). \tag{29}$$

Eqs. (27) and (29) can be implemented with RRAM logic relying on the AND, IMP, OR and XOR functions already described in [1]. Tab. II and Fig. 8 report the sequence of operations in the proposed RRAM adder at each clock signal. In this implementation, we adopted a general RRAM-logic approach [1], where IMP is operated by the use of three states, namely 0, 0^* and 1. This allowed us to experimentally demonstrate the scheme of Tab. II, since the RRAM devices with different reset currents I_{reset} and I^*_{reset}, which were assumed in the approach of Sec. 2 and 3, were not available.

Addition in Tab. II is completed in 7 clock pulses with 11 RRAM switches. Input states A and B are initially stored in switches P1 and P2, respectively, while the C_{in} is stored in P7. Other auxiliary switches are initially prepared in either state 0^* or state 1, depending on their use. The output S finally appears in switch P6 at clock 7, while the C_{out} is located in P10. In the first 4 clock pulses, the XOR operation A $\oplus$ B is completed through AND and IMP operations according to the algorithm:

$$A \oplus B = (A \rightarrow B') \cdot (B' \rightarrow A), \tag{30}$$

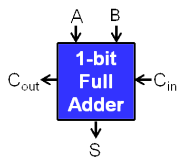

Fig. 7. Flow diagram of a 1-bit adder with input A and B, output S, carry-in C_{in} and carry-out C_{out}.

TABLE II

SEQUENCE OF OPERATIONS IN THE 1-BIT ADDITION WITH 7 CLOCK PULSES AND 11 SWITCHES. IMP AND REGENERATION (*e.g.*, P3 = P3) ARE REPORTED IN THE OUTPUT SWITCH ONLY, WHILE AND IS REPORTED FOR BOTH SWITCHES. INPUT STATES ARE LOCATED IN P1 = A, P2 = B, OUTPUT STATE IN P6 = P11 = S, CARRY-IN IN P7 = C_{in} AND CARRY-OUT IN P10 = C_{out}.

Clock=	**1**	**2**	**3**	**4**	**5**	**6**	**7**
P1 = A	P1·P5			P1·P2			
P2 = B				P1·P2	P2·P10		
P3 = 0*	P2→P3	P3=P3					
P4 = 0*		P2→P4	P1→P4	P4·P5			
P5 = 1	P1·P5		P3→P5	P4·P5	P5·P6		
P6 = 1					P5·P6	P8→P6	S=P6·P11
P7 = C_{in}							
P8 = 0*	P7→P8	P8=P8					
P9 = 0*		P7→P9			P4→P9	P9=P9	
P10 = 1					P2·P10		C_{out}=P9→P10
P11 = 0*			P7→P11			P5→P11	S=P6·P11

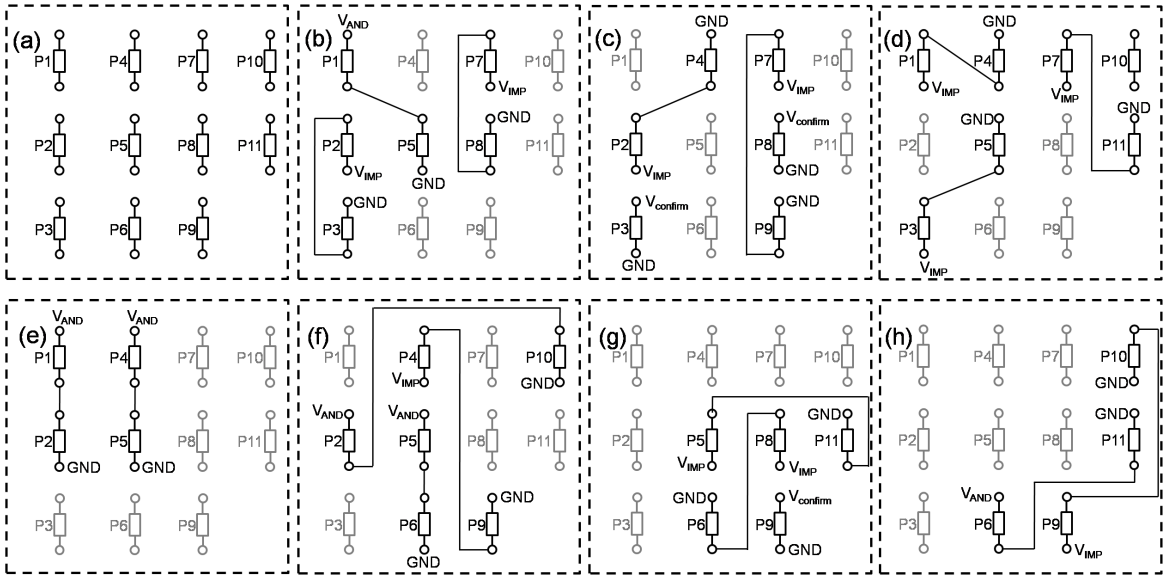

Fig. 8. Schematic of the connections for the 1-bit adder demonstrated through reconfigurable wiring. Note that 1T1R devices were used to demonstrate the functionality of the adder. All switches without connections (a), switches and connections for each clock pulses from 1 to 7 (b-h). V_{AND}, V_{IMP} and $V_{confirm}$ are the voltages applied to compute AND, IMP and confirm operations, while GND is the ground (*i.e.*, 0 V). All the applied voltages are positive, IMP operation is obtained applying a positive pulse at the bottom switch, instead a negative pulse at the top switch.

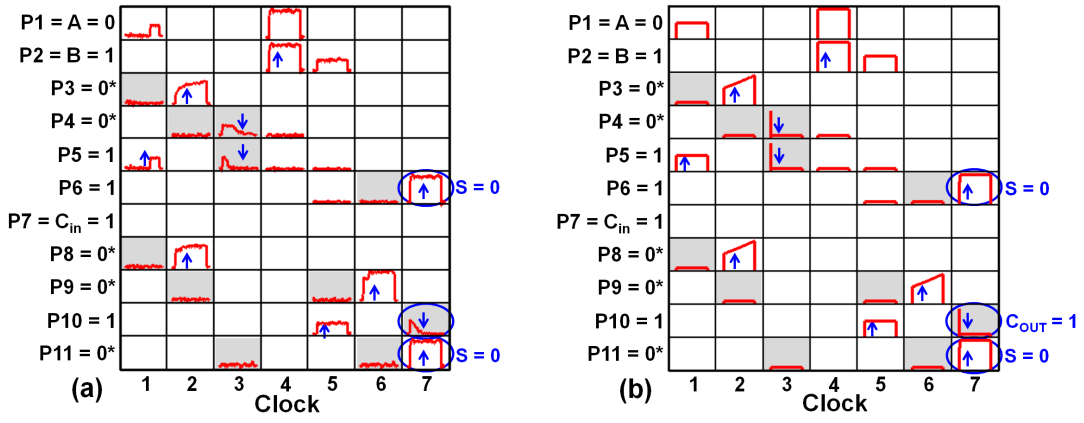

Fig. 9. Experimental (a) and simulated (b) current in RRAM gates for demonstrating the 1-bit adder according to the scheme in Tab. II. The current is shown only in the output RRAM for IMP (highlighted in gray), and in both RRAMs for AND operations. The blue arrows indicate set (1 to 0) or reset (0 to 1) transitions in the logic switch. The operation current was I_C = 80 μA, pulse time = 100 ms.

in agreement with Tab. IV in the companion paper [1]. The result of the XOR operation is found in P4 and P5 at clock #4, and is further replicated in P6 at clock #5. During this initial phase, the negated C_{in} is replicated in three auxiliary switches, namely P8 (clock #1 and #2), P9 (clock #2) and P11 (clock #3). At clock #6, the operations $C'_{in} \rightarrow A \oplus B$ and $A \oplus B \rightarrow C'_{in}$ which are needed to complete the second XOR operation in Eq. (27), are completed in P6 and P11, respectively, then their respective outputs are used as inputs for the final AND operation providing the output S at clock #7. To compute the carry out, the operations $(A \oplus B) \rightarrow C'_{in}$ and $A \cdot B$ are performed at clock #5 in P9 and P10, respectively, then their outputs are combined through the final IMP operation at clock #7 in P10, according to Eq. (29).

The RRAM adder requires a relatively small area consumption of only 11 switches, which would correspond to areas of $44F^2$ or $22F^2$, in the case of an ideal crossbar with one or 2 layers, respectively. Assuming the 1T1R architecture in Sec. 2 with a vertical transistor and $9F^2$ area of the individual switch, the ideal area consumption would rise to about $100F^2$ or $50F^2$, in the case of one or 2 layers. These results suggest a huge area saving consumption with respect to the 28-transistor adder in CMOS logic requiring few-thousands of F^2 in CMOS technology [12], [17]. The switch count and area consumption of the RRAM adder are also advantageous compared to adder circuits based on alternative technologies, such as magnetic or domain wall logic [19].

A. Experimental demonstration

The RRAM adder in Tab. II was experimentally demonstrated by wire-bonded RRAM devices with 1T1R architecture [20]. The integrated select transistor was used to control the operation current to values I_C = 80 μA and I_C^* = 30 μA for states 0 and 0^*, respectively. As a representative case, Fig. 9a shows the measured current in the serially connected RRAM switches during a 1-bit addition according to Tab. II, for initial input states A = 0 and B = 1 with carry-in C_{in} = 0. Each clock pulse lasted 0.1 s. Grey boxes indicate IMP operation (V < 0), while all other boxes contain AND operations (V > 0). The current is shown for both RRAM switches for AND operations. For instance, the current shown in P1 and P5 at clock #1, representing the operation P1·P5, shows a steep increase at about 2/3 of the pulse-width, due to the transition of P5 from state 1 to state 0, indicated as a blue arrow in P5. A reduced compliance current I_C^* was used during this operation since P5 must serve as second operand in the IMP operation P3 $\rightarrow$ P5 at clock #3. Similar set transitions during AND operations take place in P1·P2 at clock #4, P2·P10 at clock #5 and P6·P11 at clock #11. Confirm transitions from 0^* to 0 were carried out in P3 and P8 at clock #2 and P9 at clock #6. The current during a generic IMP operation P $\rightarrow$ Q is shown for the second operand (Q) only. For instance, the current during the operation P2 $\rightarrow$ P3 with P2 = B = 1 at clock #1 is shown for P3 only. Since P2 remains in the off state, only a low, off-state current can be seen with no switching. Reset transitions $0^* \rightarrow 1$ during IMP operations are seen in P4 and P5 at clock #3 and P10 = C_{out} at clock #7.

Fig. 9b shows the calculated current response for the same addition as in Fig. 9a. Simulations were achieved with an analytical model for RRAM based on filament growth/dissolution activated by the local field and temperature [21]. Set and reset transitions well agree with the experimental switching behavior in Fig. 9a.

Tab. II shows that the 1-bit adder requires 11 cells and 7 clock pulses. Generalizing, for a N-bit full adder, 12+N cells (11 for computation and N+1 to store the results) and 27N clock pulses (*i.e.* for each bit, 7 pulses for computation, 19 pulses to initialize the switches and one pulse to store the sum in a memory switch) are needed. Assuming a crossbar implementation, similar to the one described in section III.E in the companion paper [1], the switch number is again 11, while the number of clock pulses becomes equal to 39N. These experimental results can be compared to other theoretical RRAM adders reported in the literature. For instance, a simulated N-bit IMP-based adder that requires 89N clock pulses and 3N+5 switches was reported [22]. This approach can be further optimized by series/parallel schemes: for instance, the number of cycles is reduced to 29N in a serial approach [23]. The number of cycles/switches was shown to be reduced with the use of complementary resistive switch (CRS) [24], although direct cascading is not possible in this approach, due to the different nature of the input (a voltage driving CRS switching) and the output (the CRS resistance state). Note finally that previous works only reported the adder operation by simulations, whereas the present work provides both simulations and experimental demonstration with practical RRAM devices.

B. Energy consumption

The energy consumption in Fig. 9 can be estimated by the formula:

$$\begin{aligned} E_{add} =& N_{1\rightarrow 0} V_+ I_C \frac{t_P}{2} + N_{1\rightarrow 0^*} V_+ I_C^* \frac{t_P}{2} + N_0 V_+ I_C t_P \\ &+ N_{0^*\rightarrow 0} V_+ (I_C + I_C^*) \frac{t_P}{2} + N_{0^*\rightarrow 1} V_- I_C^* \frac{t_P}{2}, \end{aligned} \tag{31}$$

where $N_{1\rightarrow 0}$, $N_{1\rightarrow 0^*}$, N_0, $N_{0^*\rightarrow 0}$ and $N_{0^*\rightarrow 1}$ are the number of transitions $1 \rightarrow 0$ (full set), $1 \rightarrow 0^*$ (partial set), $0 \rightarrow 0$ (no transition during AND operation), $0^* \rightarrow 0$ (confirm) and $0^* \rightarrow 1$ (reset), respectively. The voltages V_+ and V_- are those appearing across the 2 serially-connected RRAM switches during AND and IMP operations, respectively, while t_P is the clock pulse-width. Each transition was assumed to take place in correspondence of $t_P/2$ for simplicity in Eq. (31). Fig. 10 shows the number of transitions in Eq. (31) as a function of the input states A, B and C_{in}, and the estimated energy consumption for a practical case, assuming t_P = 10 ns, $I_C = 2I_C^*$ = 10 μA, V_+ = 1.3 V and $|V_-|$ = 0.6 V. This is the 'dynamic' energy consumption of the RRAM adder, while there is no static power component given the nonvolatile nature of RRAM switches. On the other hand, the static power consumption in a CMOS microprocessor might be even larger than the dynamic contribution [25]. These results suggest that, besides a smaller circuit area, RRAM logic may allow reducing the normally-off operation of non-volatile switches.

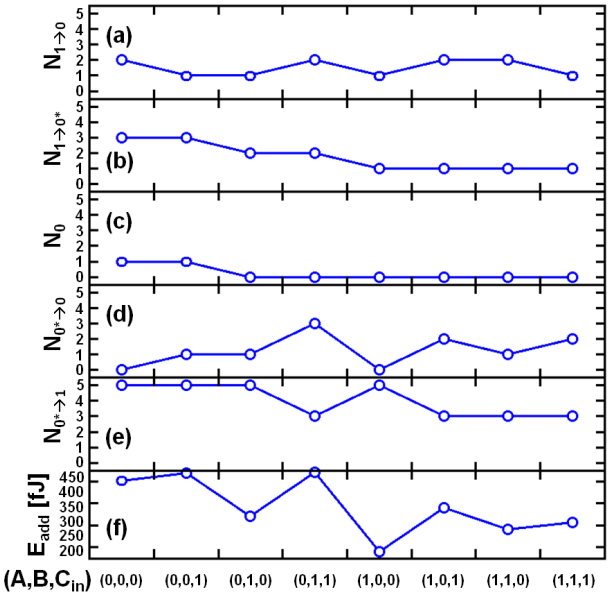

Fig. 10. Number of transitions from 1 to 0 (a), from 1 to 0* (b), from 0* to 0 (c), from 0* to 1 (d), number of no-transitions in the set state (e) and energy dissipation as a function of the input configuration (A,B,C_{in}). The total dissipated energy (f) is evaluated by Eq. (31).

V. Conclusions

This work addresses RRAM logic from the circuit viewpoint. We show that both 1T1R and 1T1R-1R1R architectures show a window of operating voltages for AND and IMP operations which form the basis for all logic operations. Finally, a 1-bit adder is designed and demonstrated by experiments and simulations, allowing for a prediction of energy consumption. RRAM logic appears as a promising alternative to CMOS technology for area and energy scaling thanks to the reduced area and nonvolatile behavior of RRAM devices.

VI. Acknowledgments

The authors acknowledge Adesto Technologies for providing experimental RRAM samples for this work.

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