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Norton TLM based stub-link conversion technique

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Abstract

This paper presents a fast and efficient way of simulating multistage power electronic circuits with stages operating at widely separated frequencies, using the Norton transmission line modelling (TLM) technique. A multistage circuit can be decoupled into several sub-circuits which can then be simulated individually with different time steps according to their circuit time constants. Energy exchange between linked sub-circuits are made possible via the use of a stub-link conversion technique. Simulation is carried out using a forward voltage converter circuit. Results are compared with those from PSpice.

1 Introduction

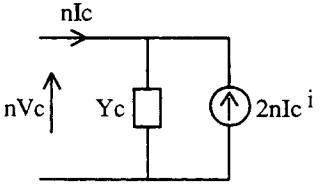
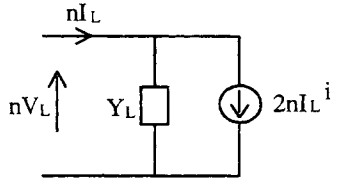
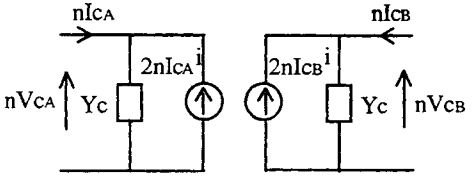
Many power electronic circuits consist of several power stages which operate at widely different frequencies, such as switched mode power supply systems and converter/inverter driven power and machine systems. Traditional time-domain simulation approach usually models the entire system as a single network and execute the model algorithms sequentially. The size of the time step used for the simulation of such single system is, however, limited by the smallest time constant, ie. the highest switching frequency, in the multi-stage system. Consequently, the model formulation process for large multistage system becomes complicated and the corresponding computing time is large. Recently, a decoupling technique based on the transmission line (TL) link model has been proposed and successfully implemented in simulating a multistage power electronic system (Hui[1]). Since links are two-port models, they serve to decouple a complex circuit into simpler sub-circuits. This results in simpler system equation formulation, as well as significantly faster simulation process, since smaller system matrices are involved.

Use of the Norton TL models instead of the traditional Thevenin models allow nodal analysis techniques to be employed (Fung[2]). This further simplifies the system equation formulation process, since in any circuit, there are many ways to define the meshes but only one way to define the nodes. Further computing time reduction can be achieved if different time steps are used for the simulation of different sub-circuits, provided energy exchange between the decoupled sub-circuits can take place regularly.

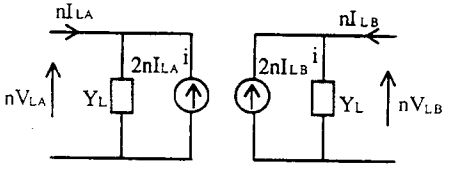
2 Norton transmission line models

Norton TL models for reactive components were recently proposed (Fung[2]). For reference, these models are summarised in table 1 below.

Table 1 Norton TL stub and link models for reactive components

Norton TL Model	Model Equations
Capacitor stub: 	$Yc = 2C/T$ $nIc = nVc*Yc - 2nIc^i$ $n+1Ic^i = nIc + nIc^i$
Inductor stub: 	$Y_L = T/2L$ $nI_L = nV_L*Y_L + 2nI_L^i$ $n+1I_L^i = nI_L - nI_L^i$
Capacitor link: 	$Yc = C/T$ $nIc_A = nVc_A*Yc - 2nIc_A^i$ $nIc_B = nIc_B*Yc - 2nIc_B^i$ $n+1Ic_A^i = nIc_B + nIc_B^i$ $n+1Ic_B^i = nIc_A + nIc_A^i$

Inductor link:



$$Y_L = T/L$$
$$nI_{LA} = nV_{LA} \cdot Yc - 2nI_{LA}^{i}$$
$$nI_{LB} = nI_{LB} \cdot Yc - 2nI_{LB}^{i}$$
$$n+1I_{LA}^{i} = nI_{LB} + nI_{LB}^{i}$$
$$n+1I_{LB}^{i} = nI_{LA} + nI_{LA}^{i}$$

3 Multiple Time Steps in Norton models

Since a link model is two ported, it decouples an electric circuit into two sub-circuits, which may be switching in different frequencies. A simple case is shown in Figures 1 to 3, where sub-circuit A switches at 50 Hz and sub-circuit B at say 20 KHz.

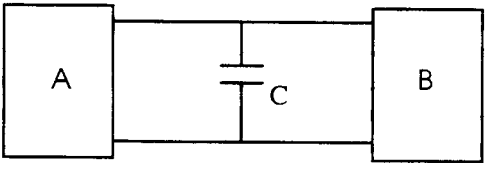


Figure 1 Capacitor link C

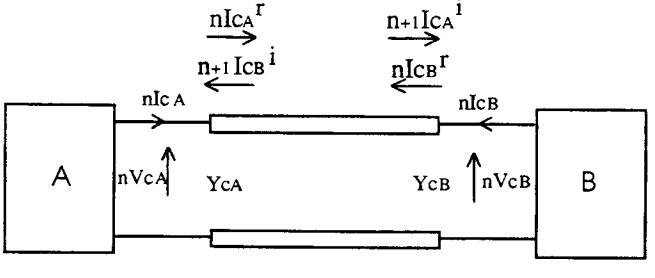


Figure 2 Capacitor modelled by TL link

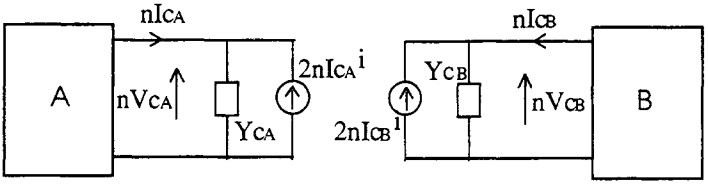


Figure 3 Capacitor modelled by Norton TL link

For a link model to operate in two different time steps say t_1 for sub-circuit A and t_2 for sub-circuit B, modifications are needed to the link model shown in table 1. Firstly the admittances on the two sides of the model, which depend on the time step, are now different.

$$Y_{cA} = C/t_1 \quad (1)$$

$$Y_{cB} = C/t_2 \quad (2)$$

Secondly, the exchange equations for the incident current at the next time step, $_{n+1}Ic_A^i$ and $_{n+1}Ic_B^i$ have to be modified. In a link model shown in Figure 2, it takes one time step for a voltage or current pulse to travel the length of the transmission line to become the incident pulse for the next time step. Hence normally,

$$_{n+1}Ic_A^i = nIc_B^r$$

$$_{n+1}Ic_B^i = nIc_A^r$$

However, this is true only if a single time step is used. Two different time steps require two different characteristic admittances on the two ends of the transmission line. Hence the equations just shown are no longer valid. Equating the incident and reflected voltages,

$$_{n+1}Ic_A^i / Y_{cA} = nIc_B^r / Y_{cB}$$

$$_{n+1}Ic_B^i / Y_{cB} = nIc_A^r / Y_{cA}$$

Substitute (1) and (2) into these two equations,

$$_{n+1}Ic_A^i = nIc_B^r * (t_2/t_1)$$

$$_{n+1}Ic_B^i = nIc_A^r * (t_1/t_2)$$

Thus the two exchange equations for next incident currents shown in Table 1 can be modified to,

$$_{n+1}Ic_A^i = (nIc_B + nIc_B^i) * (t_2/t_1) \quad (3)$$

$$_{n+1}Ic_B^i = (nIc_A + nIc_A^i) * (t_1/t_2) \quad (4)$$

Thirdly, in a homogeneous link model using only one time step, simulation proceeds by finding all the nodal voltages, then the reflected currents in a given time step, and then the incident currents for the next time step by the exchange

equations shown in table 1. This process is then repeated for successive time steps. With different time steps the two sides of the model are out of synchronisation. For example, assume t_1 is greater than t_2, each time sub-circuit A completes one time step, sub-circuit B has to go through (t_1/t_2) time steps before both sub-circuits are in synchronisation again. Until then it will be wrong to allow the two sides to exchange any current pulse. There is no problem stopping sub-circuit A for sub-circuit B to catch up, but for B to take several small time steps, it needs a new incident current each time, which is not available from A. To overcome this problem, the Norton link model must first be changed to a Norton equivalent stub model. Since stub model is one-ported, it just reflects the incident current. Sub-circuit B is able to proceed until it catches up with A. The stub model is then converted back to the link model before equations 3 and 4 are applied for current exchange.

Consider sub-circuit B in Figure 3, it is connected initially to a link model as shown in Figure 4a. At other instances, sub-circuit B can be considered as connected to a stub shown in Figure 4b. Since sub-circuit B is operating all the time on time step t_2, the admittances for the stub model Y_{CB}_sb and for the link model Y_{CB}_lk as given in table 1 are,

$$Y_{CB}\_sb = 2*C / t_2 \tag{5}$$

$$Y_{CB}\_lk = C / t_2 \tag{6}$$

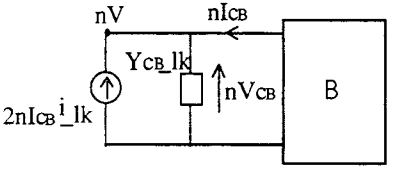


Figure 4a Norton link

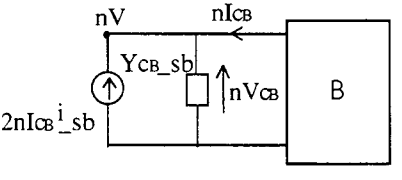


Figure 4b Norton stub

For the two models to be equivalent, the model voltage nV_{CB}, model current nI_{CB} and node voltage nV must be identical. This is the basis upon which the conversion equations are derived. To convert from link to stub, the model current is obtained from Figure 4a and 4b respectively and then equated, assuming the node voltage nV is known.

$$nV*Y_{CB}\_lk - 2*nI_{CB}{}^{i}\_lk = nV*Y_{CB}\_sb - 2*nI_{CB}{}^{i}\_sb$$

With equations (5) and (6), the above expression gives the following link-to-stub conversion equation,

$$nI_{CB}{}^{i}\_sb = nI_{CB}{}^{i}\_lk + nV*Y_{CB}\_lk/2 \tag{7}$$

Conversely the stub-to-link conversion equation can be expressed as

$$nI_{CB}{}^{i}\_lk = nI_{CB}{}^{i}\_sb - nV*Y_{CB}\_lk/2 \tag{8}$$

4 Circuit Simulation

A forward voltage converter circuit shown in Figure 5 was chosen for simulation. Figure 6 shows one case where capacitor C1 is simulated using Norton TL link and all other reactive components are handled by Norton TL stubs. All rectifiers, diode and switch are simulated as switched resistances. Nine nodes are identified in the equivalent circuit and are numbered 0 to 8 in Figure 6.

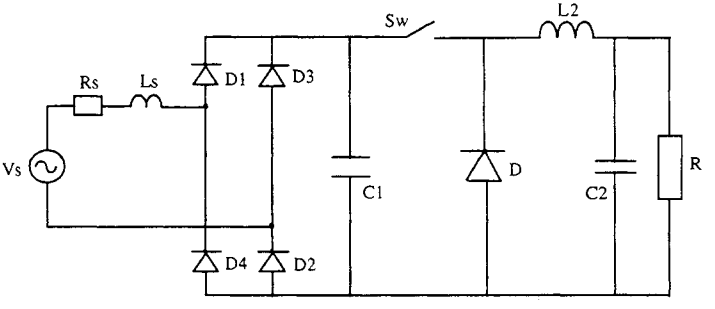


Figure 5 Forward Voltage Converter circuit

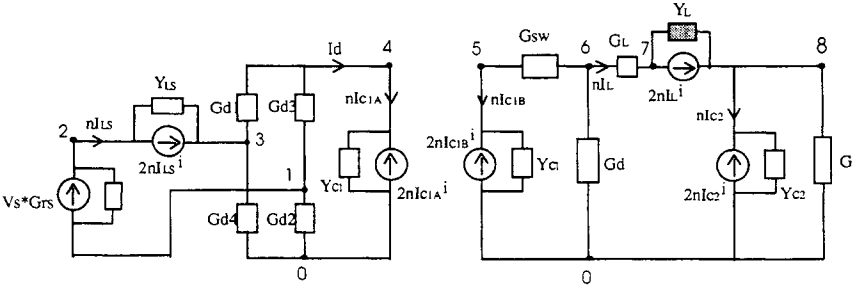


Figure 6 Norton TL equivalent circuit

The Norton TL link model for capacitor C1 decouples the converter circuit into two sub-circuits A and B. Simulation was carried out by finding all nodal voltages, then all TL model currents and finally all TL model incident currents for the next time step, in a manner described in reference 2. Since sub-circuit A switches at 50 Hz and sub-circuit B switches at 25 KHz, two different time steps can be used to model the decoupled circuit, using the stub-link conversion technique.

5 Results and discussion

The forward converter circuit shown in Figure 5 and 6 were first simulated with PSpice for 10 mains cycles (PSpice user guide[3]). Steady state results were taken starting from the 10^{th} mains cycle. Figure 7 shows the voltage across capacitor C1, and the current output from the rectifiers Id, plotted every 100 micro seconds over the 10^{th} mains cycle. Figure 8 shows the output voltage across C2 and the inductor current, plotted every 1 micro second over a duration of 500 micro seconds. This is purposely chosen so that the low frequency circuit response as well as high frequency ripples can be analysed.

Parameters used for simulation are:
AC mains 50 volts at 50 Hz
Switching frequency at 25 KHz and duty cycle 0.175

Diode on resistance = 1.2Ω	Diode off resistance = 10 KΩ
Switch on resistance = 1Ω	Switch off resistance = 10 KΩ
Source resistance Rs = 1Ω	Load resistance R = 7.2Ω
Inductor L2 resistance = 1Ω	
Source inductance Ls = 1 μH	Inductor L2 = 500 μH
Capacitor C1=500 μF	Capacitor C2 = 10 μF

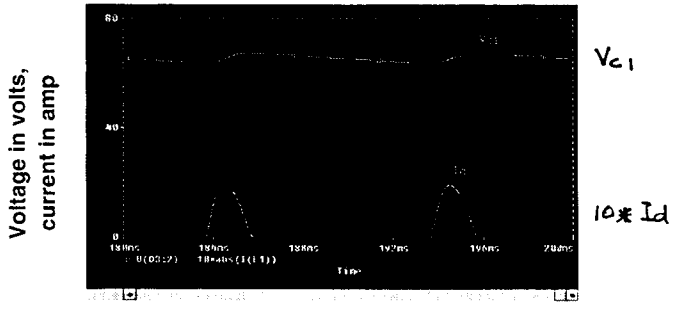


Figure 7 PSpice simulated voltage of C1 and output current of rectifiers Id

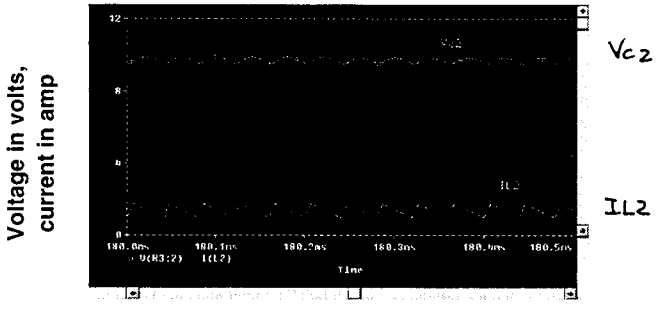


Figure 8 PSpice simulated voltage of C2 and current of inductor IL2

TLM simulation was also carried out using Norton TL stub and link models based on one time step of 1 μsec. Results are shown in Figures 9 and 10.

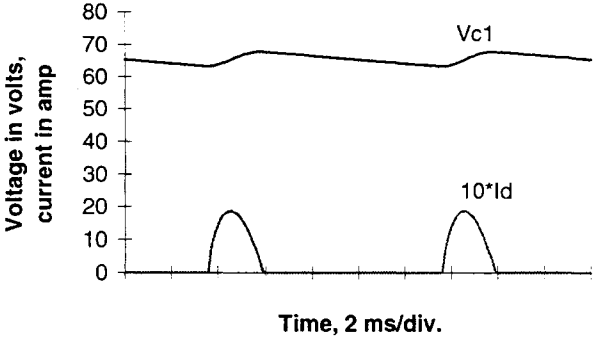


Figure 9 Link simulated voltage of C1 and output current of rectifiers Id (one time step only)

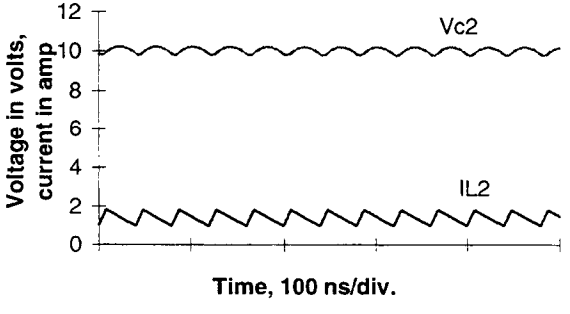


Figure 10 Link simulated voltage of C2 and current of inductor IL2 (one time step only)

Next, the stub-link conversion technique is added to allow two separate time steps to be used, to cater for the fact that the two sub-circuits operate at different frequencies. Results are shown in Figures 11 and 12.

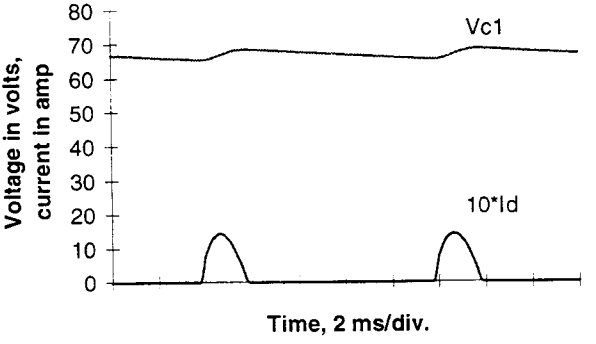


Figure 11 Dual time step simulated voltage of C1 and output current of rectifiers Id (t_1=4 μsec, t_2=1μsec)

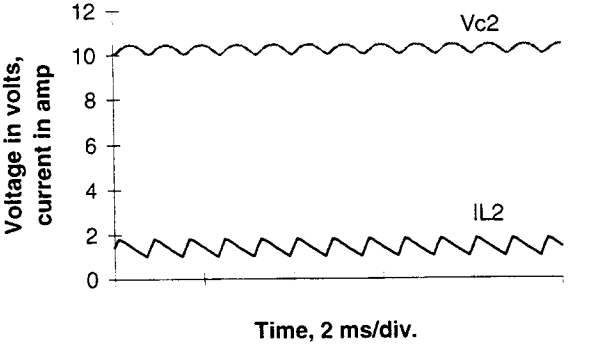


Figure 12 Dual time step simulated voltage of C2 and current of inductor IL2 (t_1=4 μsec, t_2=1μsec)

Comparing the results obtained through simulation by PSpice, conventional Norton TL models and multiple time step technique as shown in Figures 7 to 12 showed that they are reasonably close to one another.

Using a 66 MHz 468 PC, program execution time required to perform the circuit simulation for 10 mains cycles were taken. They are listed in table 2 below for comparison.

Table 2 Execution time comparison

PSpice	1533 seconds
Norton TL stub only (time step 1μsec)	34 seconds
Norton TL link (time step 1μsec)	21 seconds
Norton TL link (two time steps 2 and 1 μsec)	20 seconds
Norton TL link (two time steps 3 and 1 μsec)	18 seconds
Norton TL link (two time steps 4 and 1 μsec)	17 seconds

6 Conclusion

It has been found that the use of the Norton TL link model can lead to considerable reduction in computing time in circuit simulation, with good accuracy. In this case, 38% reduction is obtained. Use of multiple time steps further improves the efficiency in computer simulation without significantly compromising the accuracy of the result. In this case, a total reduction of 50% is achieved, compared to the stub only method. The results obtained has confirmed the validity of the proposed stub-link conversion technique.

Reference

1. S.Y.R Hui, K.K. Fung and C. Christopoulos, Decoupled Simulation of DC-Linked Power Electronic Systems Using Transmission-Line Links, *IEEE Transactions on Power Electronics*, January 1994, Vol. 9, No.1

2. K.K. Fung and S.Y.R Hui, Duality of Transmission Line models for Circuit Simulation, *Proceedings of ElectroSoft 1996*

3. *The design center circuit analysis user's guide*, MicroSim Corp., July 1992