Novel Code Converter Employing Reversible logic

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ABSTRACT

Quantum computing is one of the emerging fields of technology that has been a guiding light for low power VLSI, low power CMOS design, optical information computing, DNAcomputing, Bio-informatics and Nano-technology .A quantum circuit is a model for quantum computation in which a computation is performed by a sequence of quantum gates, which are reversible transformation on a quantum mechanical analog of an n bit register, referred to as an n- qubit. Code converters are required day in and day out. In this paper, a reversible 5421 to binary code converter is implemented.

Keywords:

Quantum computation, Reversible Logic, Code Converters, New MCL Gate, Garbage Values, Nano-technology, advanced computing

1. INTRODUCTION AND LITERATURE SURVEY:

The primitive combinational logic circuits dissipate heat energy for every bit of information that is lost during the operation. This is because according to second law of thermodynamics, information once lost cannot be recovered by any methods. In late 1960's great scientists and physicists like R.Landauer[1] demonstrated that even highly sophisticated circuits which are constructed using conventional irreversible gates dissipate heat due to loss of information. It was further shown that one bit of information lost, will dissipate kT*ln (2) joules of energy where, k is the Boltzmann's constant and k=1.38x10 $^{-23}$ J/K, T is the absolute temperature in Kelvin. At room temperature i.e. at 300 K, the amount of energy lost will be $2.9x10^{-21}$J which is small but not negligible .According to Moore's law the number of transistors will double every 18 months. Thus energy conservative devices are the need of the day.

This paper is organized into six sections. Section 1 is Introduction. In the section 2 we discuss the various definitions regarding the reversible logic gates. In the section 3 the study of previously existing reversible logic gates mainly used in this paper is performed. The section 4 shows the truth table and the conventional irreversible logic implementation of the 5421 to decimal code converter. It also throws light on the designed reversible code converter. The

section 5 proposes a new reversible logic gate that further simplifies the design. The simulation results are also shown here. The paper then concludes with the scope for future work and acknowledgements.

2. BASIC DEFINITIONS PERTAINING TO REVERSIBLE LOGIC:

2.1 Reversible Function:

A Boolean Function $f(x_1,x_2,x_3,....x_n)$ is said to be reversible if it satisfies the following criteria : (i)The number of inputs is equal to the number of the number of outputs.(ii)Every output vector has an unique pre-image.

2.2 Reversible logic gate:

A reversible logic gate is an N-input N-output logic device that provides one to one mapping between the input and the output. It not only helps us to determine the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs.

2.3 Garbage:

Additional inputs or outputs can be added so as to make the number of inputs and outputs equal whenever necessary. This also refers to the number of outputs which are not used in the synthesis of a given function. In certain cases these become mandatory to achieve reversibility.

2.4 Quantum cost [9]:

This refers to the cost of the circuit in terms of the cost of a primitive gate. It is computed knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit.

2.5 Gate levels or Logic Depth:

This refers to the number of levels in the circuit which are required to realize the given logic functions.

2.6 Flexibility [9]:

This refers to the universality of a reversible logic gate in realizing more functions.

2.7 Gate count:

The number of reversible gates used to realize the function.

The following are the important design constraints for reversible logic circuits.

1. Reversible logic gates do not allow fan-outs.
2. Reversible logic circuits should have minimum quantum cost.
3. The design can be optimized so as to produce minimum number of garbage outputs.
4. The reversible logic circuits must use minimum number of constant inputs.
5. The reversible logic circuits must use a minimum logic depth or gate levels.

3. PRE-EXISTING REVERSIBLE LOGIC GATES:

3.1 Feynman Gate(FEY):

It is a 2x2 gate and its logic circuit and its quantum implementation is as shown in the figure. It is also known as Controlled Not Gate. It has quantum cost one and is generally used for Fan Out purposes.
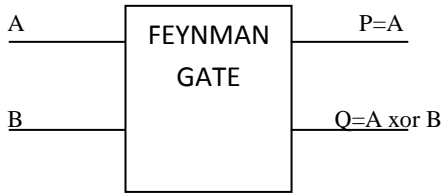
Figure 3.1a
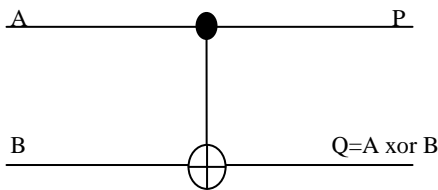
Figure 3.1b

3.2 Peres Gate (PRG):

It is a 3x3 gate and its logic circuit and its quantum implementation is as shown in the figure. It has quantum cost four.
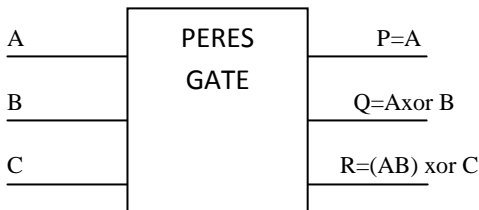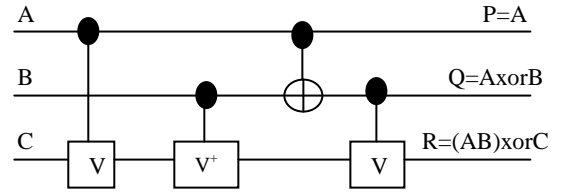

Figure 3.2a

Figure 3.2b

3.3 SCL Gate:

It is a 4x4 gate and its logic circuit is as shown .Its quantum cost is not specified by [9].
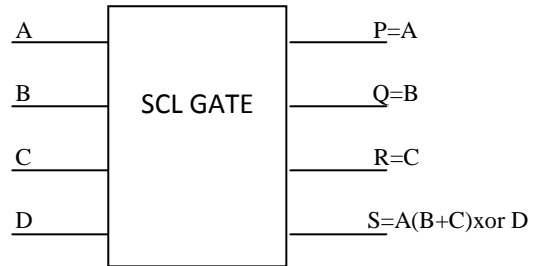

Figure 3.3

3.4 Fredkin Gate (FRED):

It is a 3x3 gate and its logic circuit and its quantum implementation is as shown in the figure. It has quantum cost five.
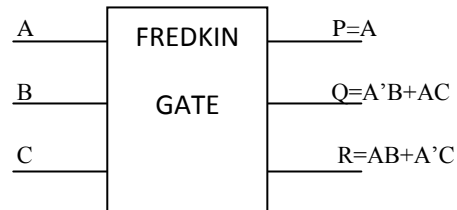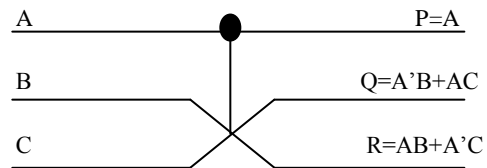

Figure 3.4a

Figure 3.4b

3.5 BJN Gate:

It is a 3x3 gate and its logic circuit and its quantum implementation is as shown in the figure. It has quantum cost five.
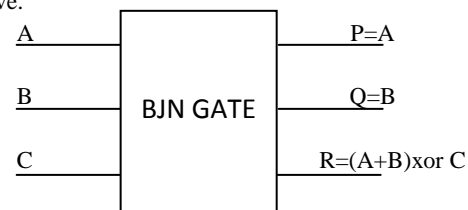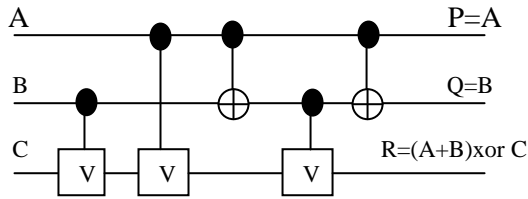

Figure 1.5a

Figure 3.5b

3.6 TR Gate:

It is a 3x3 gate and its logic circuit and its quantum implementation is as shown in the figure. It has quantum cost six.
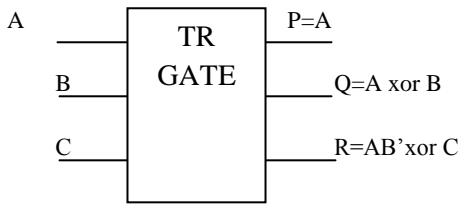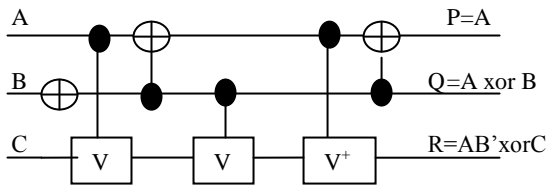

Figure 3.6a

Figure 3.6b

3.7 NFT Gate:

It is a 3x3 gate and its logic circuit and its quantum implementation is as shown in the figure. It has quantum cost five.
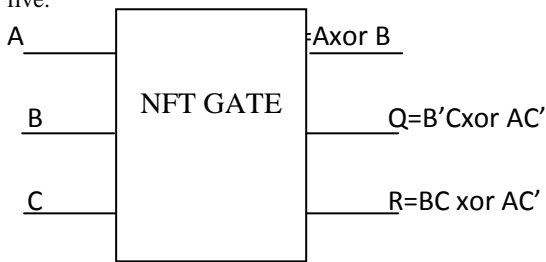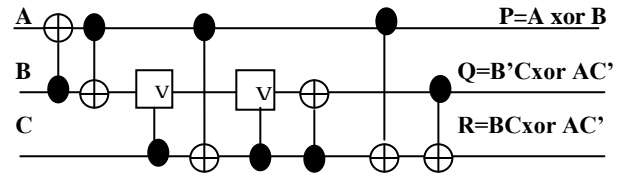

Figure 3.7a

Figure 3.7b

4. DESIGN OF 5421 TO BINARY CODE CONVERTER:

5421 is a weighted code i.e. the corresponding decimal digits are easily determined by adding the weights associated with the 1's in the code groups. The weights are given by the code name .The code word group for each decimal digit consists of 4 bits. 5421 code has an upper hand in variety of factors such as simplicity in circuit construction, operating speed and ease of decoding for read out purposes. The proposed paper involves conversion from 5421 code to Binary. The truth table of 5421 to binary code converter is as shown. The inputs are various combinations possible for 5421 code and the outputs are the corresponding binary values. Since the maximum value that can be represented in the 5421 code is 5+4+2+1=12 there is repetition of certain outputs.

Table 1: Truth Table of 5421 To Binary Code Converter

Inputs 5 4 2 1	Outputs 8 4 2 1
0 0 0 0	0 0 0 0
0 0 0 1	0 0 0 1
0 0 1 0	0 0 1 0
0 0 1 1	0 0 1 1
0 1 0 0	0 1 0 0
0 1 0 1	0 1 0 1
0 1 1 0	0 1 1 0
0 1 1 1	0 1 1 1
1 0 0 0	0 1 0 1
1 0 0 1	0 1 1 0
1 0 1 0	0 1 1 1
1 0 1 1	1 0 0 0
1 1 0 0	1 0 0 1
1 1 0 1	1 0 1 0
1 1 1 0	1 0 1 1
1 1 1 1	1 1 0 0

The irreversible implementation is as shown in figure 4.1. The reversible logic implementation is a shown in figure 4.2 4.3and 4.4. In general, the Fredkin Gate is used as a multiplier to form the product of two input variables; Feynman Gate is used for complementing. The BJN Gate [7], has been used as an adder to realize the sum of products (SOP).
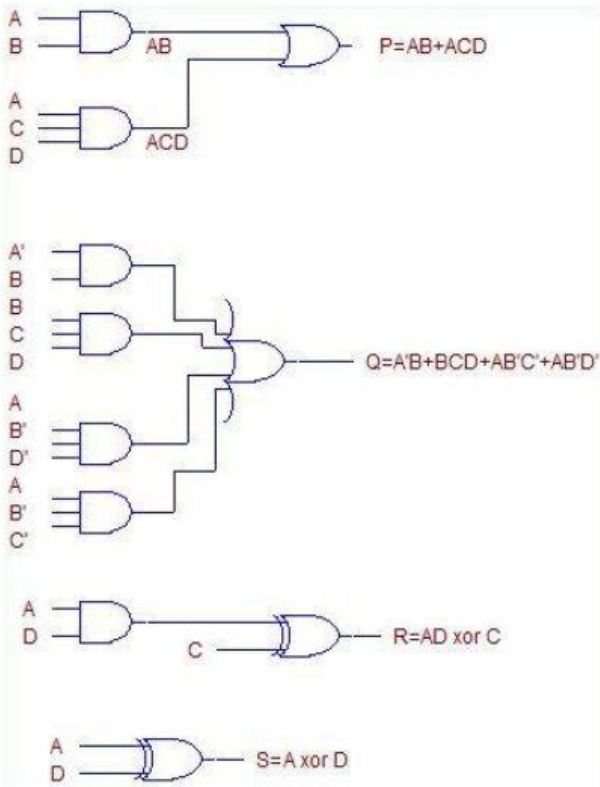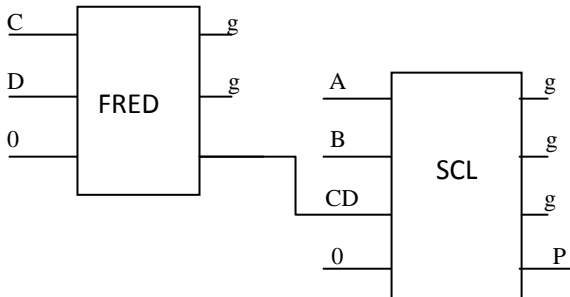
Figure 4.1 Irreversible Implementation

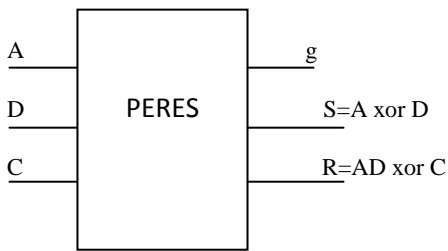**Figure 4.2 Reversible Implementation for P**

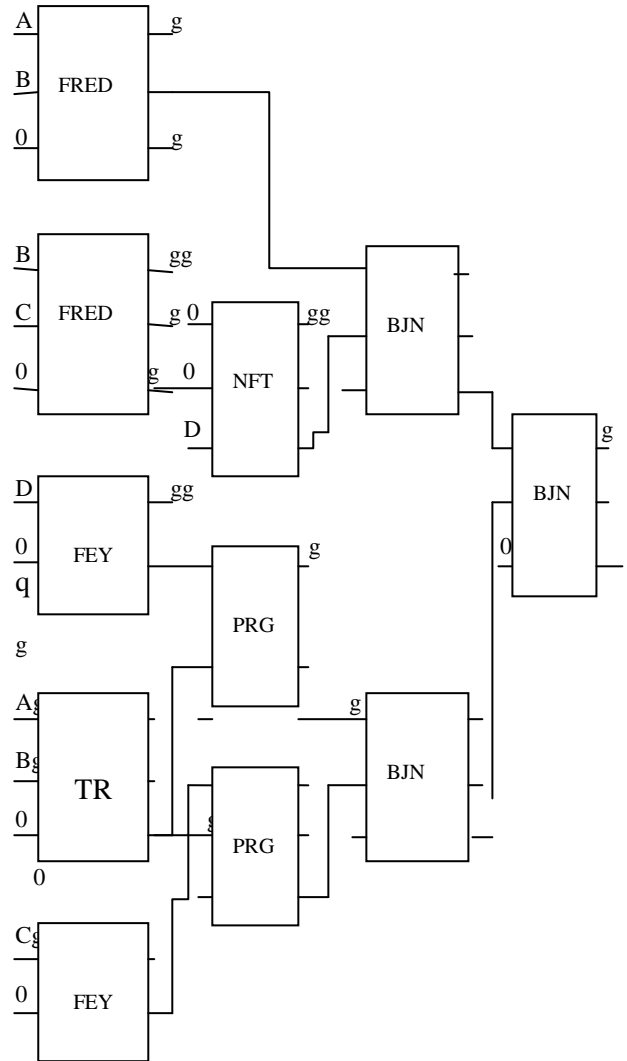**Figure 4.3 Reversible Implementation for R and S**

Figure 4.4 Reversible Implementation for Q

5. PROPOSED REVERSIBLE NEW MCL GATE:

The previous design using the already existing reversible logic gates can be further optimized by incorporating the New MCL (Multiply Complements Logic) Gate. The MCL gate is a 3x3 gate which maps the inputs A, B, C to P= (B+C)', Q= (A+B)',R=A. The truth table of this gate is as shown. The block diagram of this gate is as depicted.

Table 2: Truth Table of New MCL Gate

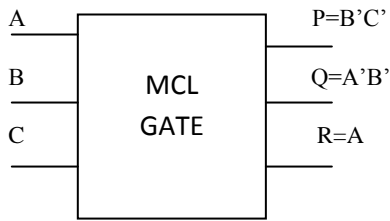| A	B	C	P=B'C'	Q=A'B'	R=A
0	0	0	1	1	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	0	0	1
1	1	0	0	1	1
1	1	1	1	1	1

Figure 5.1 New MCL Gate

5.1 Design using New MCL gate:

The design of the 5421 to binary code converter using the new reversible MCL logic gate is as shown in the figure. This design reduces the number of gates used; thus there is a cut down in the number of garbage values and constant inputs.
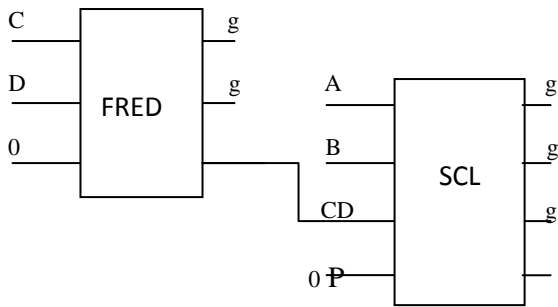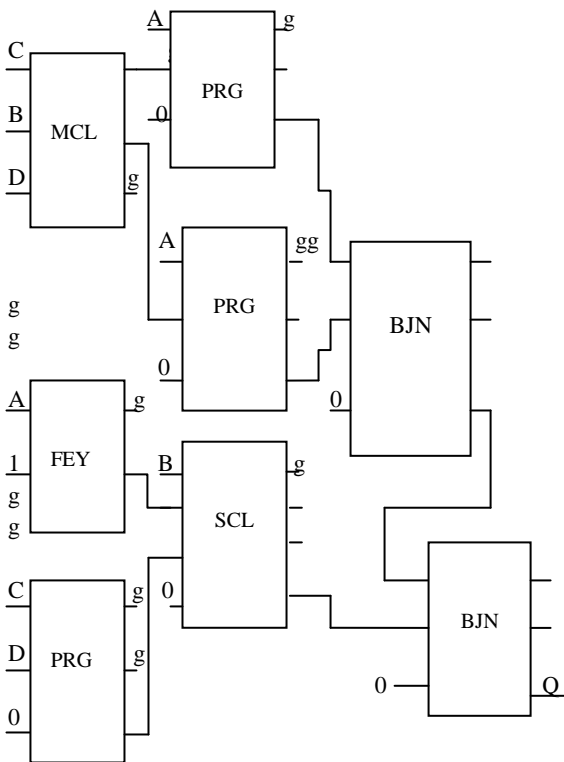

Figure 5.2 Reversible Implementation for P

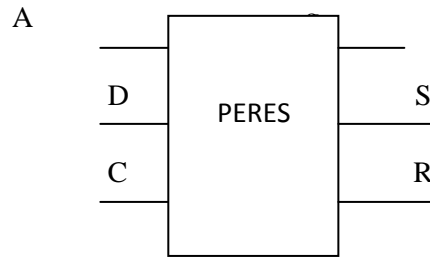**Figure 5.3 Realization of Expression for Q using MCL gate**

Figure 5.4 Reversible Implementation for R and S

5.2 Simulation Results:

The reversible implementation of the 5421 to binary code converter is simulated using XILINX in Verilog and MODELSIM.The Simulation results are shown in figure 5.4.
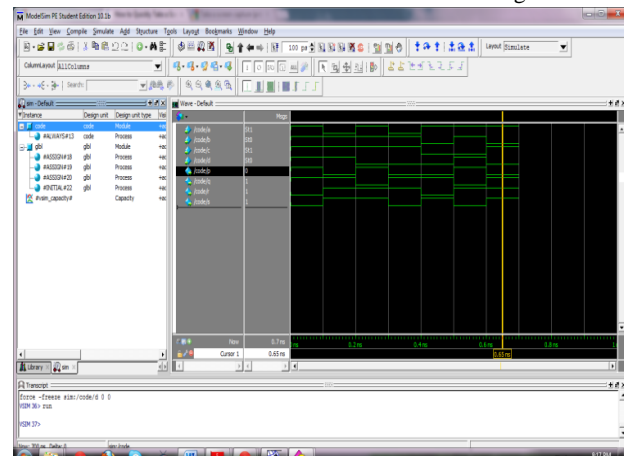

Figure 5.5 :Simulation Results using XILINX and Modelsim

6. CONCLUSIONS AND SCOPE FOR FUTURE WORK:

The proposed design 1 makes use of 1 Fredkin and 1 SCL Gate for expression of P; 2 Fredkin , 2 Feynman, 1 TR , 2 Peres , 1 NFT and 3 BJN Gates for the expression of Q; a single Peres Gate for the expressions of R and S. The proposed design 2 makes use of 1 Feynman, 3 Peres, 1 SCL, 1 MCL and 2 BJN Gates for the expression of Q with the other three designs unchanged. This reducesthe number of gates by **three,** the number of garbage outputs by **five**and number of constant inputs by **four.** The comparison of the two designs is tabulated and the same is graphically represented in figure 6.1.

In this paper a Novel 5421 to Binary Code Converter is presented. Firstly study of the common definitions pertaining to reversible logic gates is done in order to gain some clarity regarding the subject. Then a design is proposed using the existing gates. Working in the direction of optimization of the design, the paper presents a new reversible MCL gate, where the design is optimized in terms of number of garbage outputs, number of gates and number of constant inputs. Alternate optimization parameters such as quantum cost reduction, area upon fabrication etc., are under investigation as a future work.

Table 3: Comparison of the Two Designs

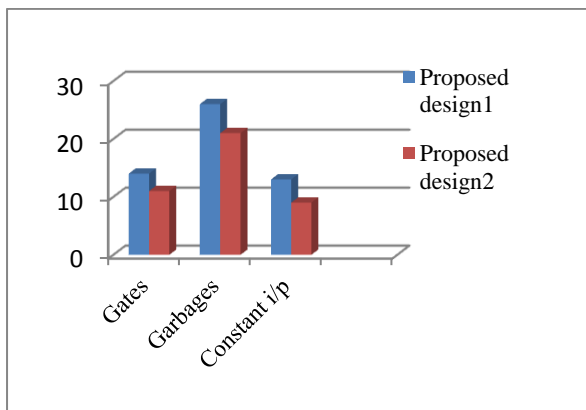| Parameter	No. of Gates	No. of Garbage Outputs	No. of Constant Inputs
Design 1 (using pre existing reversible gates)	14	26	13
Design 2 (using New MCL gate along with other gates)	11	21	9
Percentage Reduction	21.4%	19.2%	30.8%

Figure 6.1 Graphical Representation of Comparison of the two designs

7. ACKNOWLEDGEMENTS:

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