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Novel Design and Implementation Of 8 X 8 SRAM Cell Array for Low Power Applications

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***Abstract*—SRAM cells are widely used as cache memory in most of the devices now a days. Design of SRAM with low power and high efficiency has been a difficult task which is continuously being upgraded. In this paper we came out with a novel method to reduce the power consumption of SRAM cell by combining most advanced technologies in the SRAM cell design. This paper involves the integration of column decoder and multiplexer into a power efficient column select and use of twisted bitlines instead of normal bitlines and replacing linear sense amplifier with latch based sense amplifier. In this project, standard 6T (6 transistors) are used by which the leakage current is drastically reduced and low power is achieved. The full custom layout of the SRAM was realized using Electric VLSI CAD tool, the DRC and LVS was verified using Electric VLSI CAD tool and the Simulation was verified using LTSpice tool. The final tapeout (GDS II) was done using Electric VLSI CAD tool.**

*Keyword-**CMOS, SRAM, VLSI, Twisted Bitlines, LSA***

I. INTRODUCTION

The quest for larger data storage capacity lead the fabrication technology and memory development process to drive them to a more compact design rules. The maximum realizable data storage capacity for a single chip semiconductor is approximately doubling every couple of years. Many VLSI circuits are using on chip memories for their subsystems,the capacity of single chip read/write memory commercially available today is 1GigaByte.

But with the increasing memory size increases the number of transistors which in turn increases the power dissipation.Modern digital systems require the capability of storing and retrieving large amounts of information at high speeds without dissipating too much power. Number of stored data bits per unit area is a key design issue which determine storage capacity and so, the memory cost per bit. The time required to store 0r retrieve the data in the memory array is called the memory access time. The access time determines the memory speed, which is an important performance criterion of the memory array. Memories are of two types dynamic and static.

In Dynamic random access memory a capacitor is used to store the information and a transistor to access it. The cell information is degraded becauseof the junction leakage current. So it cannot store the data and read or write has to be done periodically even when cell is not accessed. But in Static Random Access Memory a latch is used, so the cell data is stored until the power is turned on. Due to low cost

and high density, dram is widely used for main memory in personal and mainframe computers. SRAM is mainly used for cache memory in microprocessors, main frames and engineering workstations.

In our paper we have discussed the low power SRAM cell design using different peripheral circuits for cache memory and concentrating on the low power stable read and write operations. As the technology decreases the power consumption becomes an important factor due to high transistor density, increased leakage currents and increase in interconnect parasitic. The power usage can be decreased by means of implementing appropriate methods.

In the first section we have discussed about the traditional 6T SRAM cell architecture which consists of hierarchical bitlines. Then the proposed architecture is discussed which is designed by replacing the hierarchical bitlines with twisted bitlines and the linear sense amplifier with the latch based sense amplifier. In our paper we also made a modification to the column decoder and multiplexer inorder to reduce the number of transistors. We designed a column select instead of column decoder and multiplexer which does the operation of both.

II. SIGNIFICANCE

Twisted bitlines and LSA is being used for long time, but research shows that nobody has combined these techniques together to build a power efficient circuit. Column Select gives extra edge for our design to make the design more power efficient.

III. TRADITIONAL ARCHITECTURE

The hierarchical bitlines random access memory is shown in figure 1. The architecture shown is an asynchronous design and is called Random access architecture because the memory location or addresses can be accessed randomly for reading or writing using the row or column decoder.

The storage array, or *cor*e, is made up of simple cell circuits arranged to share connections in horizontal rows and vertical columns. The horizontal lines, which are driven only from outside the storage array, are called word lines, while the vertical lines, along which data flow into and out of cells, are called bitlines. A cell is accessed for reading or writing by selecting its row and column[1].

Each cell is capable of storing 0 or 1. The row and column to be selected are determined by decoding information from the row and column decoders respectively.

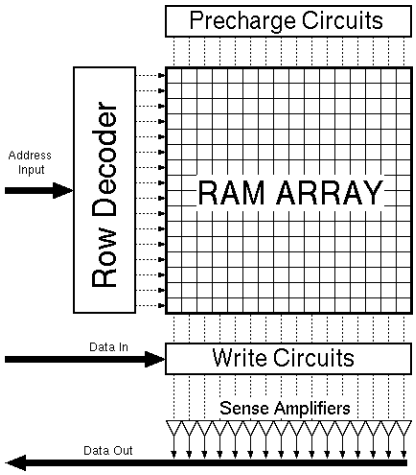

Figure 1: Traditional Architecture of SRAM cell Array[2]

IV. PROPOSED ARCHITECTURE

A. *Twisted Bit Lines*

In designing high performance circuits signal integrity is a critical factor. In the proposed architecture the parallel bit lines will introduce the cross coupling noise and in turn dissipates more power. This is the reason we used twisted bitlines to avoid the cross coupling effect.

Twisting can be defined as the local reordering of parallel running interconnect lines. It can be used for the bitline and/or wordline schemes of memories, or for busses in general[3].

The twisted bitline format for 4 bitlines is shown in the figure below.

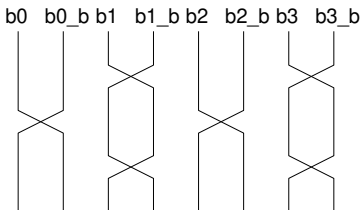

Figure 2: Twisted Bitline Architecture[3]

B. *Latch based Sense Amplifier*

The sense amplifiers need to amplify the data which is present on the bitlines during the read operation. The memory cells are weak due to their small size, and hence cannot the discharge the bitlines fast enough. Also, the bitlines continue to slew till a large differential voltage is formed between them[4]. This causes significant power dissipation since the bitlines have large capacitances[4]. Hence, by limiting the word line pulse width we can control the amount of charge pulled down by the bitlines and hence limit power dissipation[4].

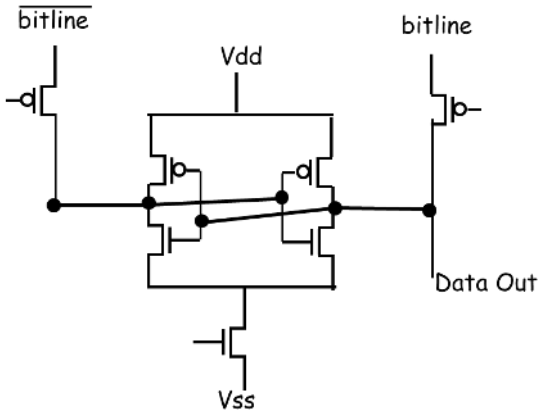

Figure 3: Latch Based Sense Amplifier[2]

The proposed architecture is shown in the below figure.

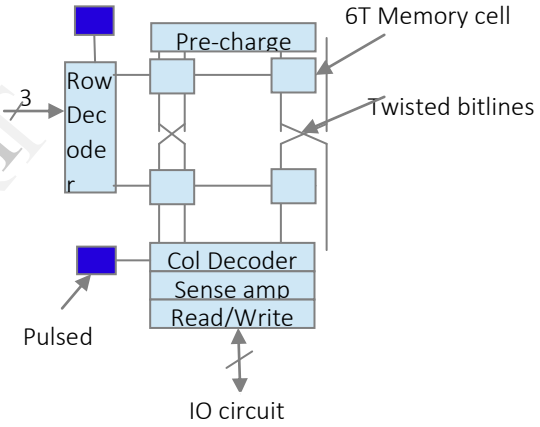

Figure 4: Proposed Architecture

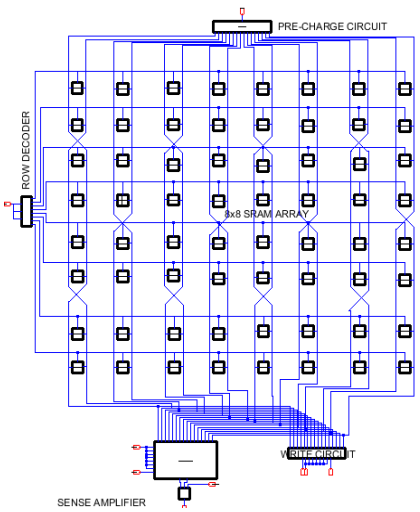

Figure 5: Schematic of Proposed Architecture in Electric

V. COMPARISON OF TRADITIONAL AND PROPOSED ARCHITECTURE

The Number of transistors can be drastically reduced in the proposed architecture, Table 1 shows comparison of number of transistors.

In the proposed architecture the column decoder is integrated with multiplexer and designed as a column select component which is for low power operation. Similarly the latch based sense amplifier which was 8 in the traditional architecture comes down to just 1 in the proposed architecture. So based on the above reasons we reduced a significant 129 transistors.

COMPONENT	TRADITIONAL ARCHITECTURE	PROPOSED ARCHITECTURE
SRAM	48	48
Column Decoder	96	16
LSA	56	7
Pre charge Circuit	16	16
Row decoder	70	70
Write driver	32	32
Total Transistors	318	189 less by 129

Table 1: Comparison of number of Transistors

VI. MEMORY WRITE AND READ:

In the simulation we have selected 1st row 8th column element for us to store the value which we read into it and then we read the stored value from the same cell using read operation.

A. Read and write '1':

To the operation first we select all the column decoders inputs to 1 and row decoder inputs to '0'.Then the phi signal is activated which is used to precharge the bit and bit_b to the required voltage levels.

When the Vwe is enabled the value of '1' is stored into the designated cell of the sram. Then to perform the read operation we enable Vsae i.e. the sense amplifier signal which is used to read '1' which we have written when Vwe is enabled. From the simulation results we can see that the voltage is 1.10v which is aproximately 1v.

Hence the read and write operation is performed accurately for '1'.

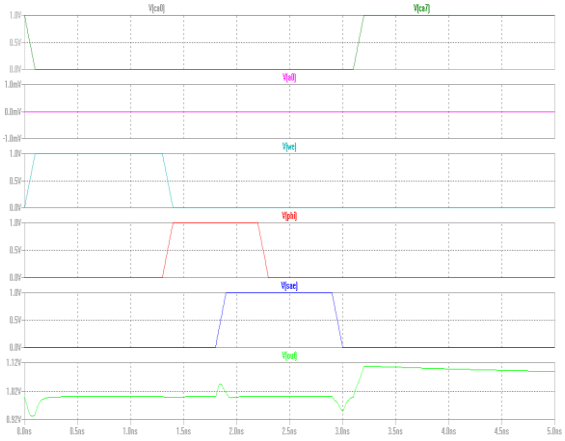

Figure 6: Read and write operation for 1

The same process is followed for Read and Write '0'.

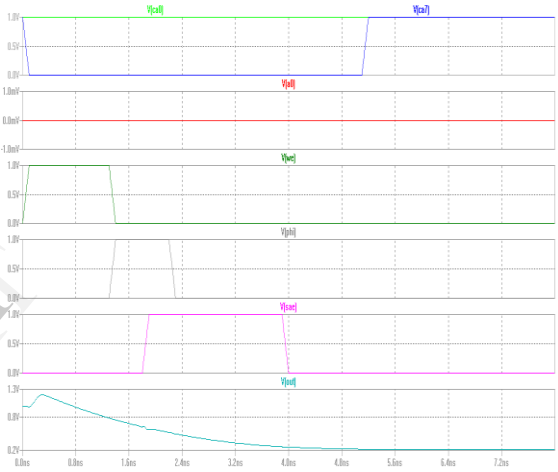

Figure 7: Read and write operation for 0

VII. SIGNAL TO NOISE MARGIN

Static noise margin (SNM) is an important parameter of SRAM cell. Static noise margin is defined as the maximum amplitude of circuit's direct current noise which the storage unit can endure with, and it is the measure of storage unit's ability against interference. If the current noise exceeds the max amplitude, error flipping will occur at the storage nodes of the cell. With the development of integrated circuit, supply voltage becomes lower, and the external noise becomes relatively larger[5]. Static noise margin will be decreased with the low supply voltage [6]. Static Noise Margin determines and checks whether the cell is written '0' or '1'. The SNM is estimated 0.4V when compared to 0.6V[7]. The low the value of SNM SRAM cell is more stable.

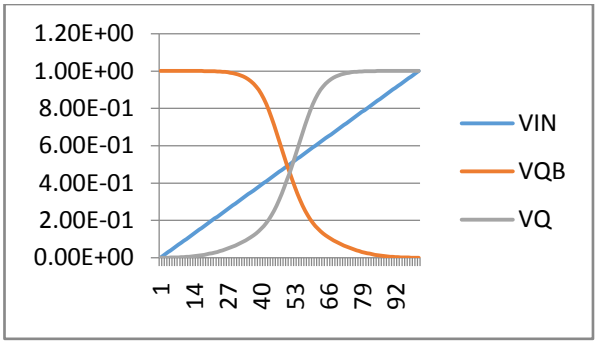

Figure 8: Signal to Noise Margin graph

VIII. POWER DISSIPATION

The two main power components that constitute the CMOS integrated circuit power are: static power and dynamic power. Static power essentially consists of the power used when the transistor is not in the process of switching and is essentially determined by the formula

$$P_{static} = I_{static} V_{dd}$$

where Vdd is the supply voltage and Istatic is the total current flowing through the device [8]Typically, CMOS technology has been praised for its low static power. However, as devices are scaled, gate oxide thicknesses decrease and there is increased probability of tunneling, resulting in larger and larger leakage currents. This subthreshold leakage current is governed by thermodynamics, more specifically the Boltzmann distribution[9].

Static Power Dissipation for conventional architecture: 702.652 uW. Static Power Dissipation for Twisted architecture: 122.578 uW.

IX. DESIGN VERIFICATION

Electric VLSI CAD tool enables us to verify the design in a systematic manner. Layout vs Schematic check (LVS) to ensure whether the layout has been designed according to schematic or not. Design Rule Check (DRC) checks whether the schematic and layout design rules are followed or not.

After the LVS and DRC check the final layout was fitted in to a pad frame and I/O's are connected.

A. GDS II

GDS II- Graphic Database System was founded by Calma Company. GDS II consists of the photo mask format of the IC.

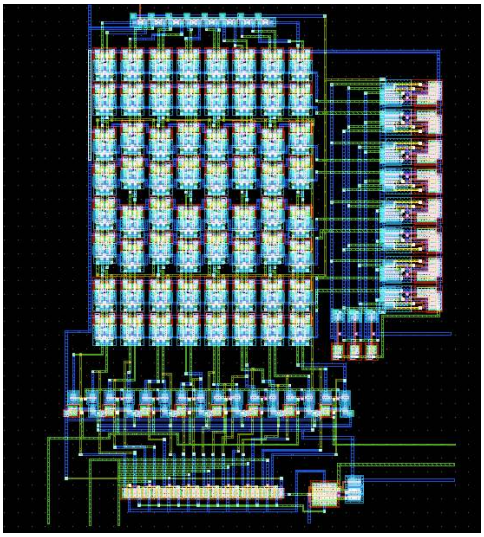

Figure 9: GDS II of the twisted 8 x8 architecture

X. CONCLUSION AND FUTURE WORK

The above discussed project is a remarkable one in the VLSI industry, it follows the current trends and produced a considerably better results than the traditional architecture. The only constraint in using the Electric VLSI CAD tool was, it's an open source tool so the resource was very less and technology was 200nm because the latest technology available is expensive.

In future we are planning to implement this design in the latest nanometer technologies, Incorporating Multi Threshold CMOS (MTCMOS) technique to reduce the leakage power and improve the efficiency.

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