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Novel Design Methodology for Short-Channel MOSFET Analog Circuits

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Abstract

This paper presents a methodology that addresses short-channel effects to design MOSFET circuits. The circuit design is based on a combination of parameter extraction and simple analytical models that allows precise results. The extraction mainly depends on the inversion level, which is independent of geometry, therefore providing points that are applicable to a wide variety of circuits. Trade-offs and design space of the device are clearly brought to the circuit design. Hand calculations and simulations of a common-source amplifier illustrate the methodology.

1. Introduction

The market trend towards mixed-signal chips demands equal design pace for both digital and analog sections. The tools for digital circuits are well developed [1,2]. The analog section, though, lacks consistent design methods [2].

The methodology introduced in this paper takes into account second order effects by referring them to the Early voltage. Extraction for this parameter is based on the inversion level, voltage supply limitations, and practical range of channel length, therefore, showing the design space for the device. Thermal noise and thermal noise coefficient are direct function of the inversion level, with their short channel effects linked to the Early voltage. The result is a simple yet accurate set of equations. The influence of second order effects in the relationship between inversion level and gate-to-source voltage is also analyzed. Trade-offs of an amplifier and their relationship with the device are addressed in the procedure. Design and simulations of a common-source amplifier demonstrate the methodology. The design approach proposed here can also be applied to more complex circuits.

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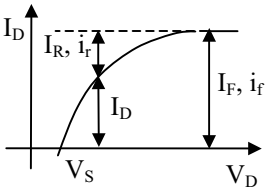
2. The MOSFET Model

An analytical MOSFET model valid in all regions of operation and suitable for hand design is presented in [3]. In this model the main parameter is the inversion level i_f alongside the normalization current I_S. i_f is the forward current I_F normalized by I_S, where I_F comes form the drain current I_D, which is decomposed into the forward and reverse I_R currents, equations (1) and (2). I_S contains information about technology, mobility μ and oxide capacitance per unit area *C'ox*, as well as geometry, width W and length L, equation (3). ϕ_t is the thermal voltage and *n* is the slope factor, typically 1.3 [3]. The region of inversion will depend on the value of i_f as seen in Figure 1. For the device in saturation i_r, I_R normalized by I_S, can be disregarded as Figure 1 shows. Also, because several properties of the device are attached to i_f as equations (1) to (9) show, the circuit trade-offs are naturally stated.



	Triode	Saturation
Strong Inversion	$i_f >> 1$	$i_f >> 1$ $i_f >> i_r$
Weak Inversion	$i_f \approx 1$	$i_f \approx 1$ $i_f >> i_r$

Figure 1. Drain Current and Inversion Level.

$$I_D = I_F - I_R \quad (1) \qquad i_{f(r)} = \frac{I_{F(R)}}{I_S} \quad (2) \qquad I_S = \mu n C'_{ox} \frac{\phi_t^2}{2} \frac{W}{L} \quad (3)$$

Equation (4) relates the normalized currents to the drain and source voltages, where V_P is the pinch-off voltage. i_p is the normalized current related to the pinch off condition and can be an arbitrary small value to define the transition between strong and weak inversion. For instance, i_p equal 3 [3]. Equation (5) shows the relationship between the gate voltage V_G and V_P. The drain-to-source saturation voltage VDSsat, equation (6), comes from (4) for a small i_r.

$$\frac{V_P - V_{S(D)}}{\phi_t} = \sqrt{1+i_{f(r)}} - \sqrt{1+i_p} + \ln\left[\frac{\sqrt{1+i_{f(r)}}-1}{\sqrt{1+i_p}-1}\right] \quad (4)$$

$$V_P \cong \frac{V_G - V_{TO}}{n} \quad (5) \qquad \frac{V_{DSsat}}{\phi_t} = \left(\sqrt{1+i_f}-1\right)+4 \quad (6)$$

The source and drain transconductances are given by equation (7) and the gate transconductance by (8).

$$\frac{\phi_t g_{ms(d)}}{I_{F(R)}} = \frac{2}{1+\sqrt{1+i_{f(r)}}} \quad (7) \qquad g_m = \frac{g_{ms} - g_{md}}{n} \quad (8)$$

Equation (9) relates intrinsic cutoff frequency f_T to i_f.

$$f_T \cong \frac{\mu\phi_t}{2\pi L^2} 2\left(\sqrt{1+i_f} - 1\right) \quad (9)$$

This set of equations, (1) to (9), addresses some of the main aspects of the MOSFET circuits.

3. Short-Channel Effects

3.1 The Influence in the Early Voltage

Short channel effects are usually addressed either by the effective mobility μ_{eff} and effective channel length L_{eff}, in models for simulators [4,5], or by the Early voltage VA, in models for hand calculation [5], yet, we can establish a relationship between both models. Carrier velocity saturation, the channel length modulation (CLM), drain induced barrier lowering (DIBL), and substrate current induced body effect (SCBE) are responsible for the behavior of the drain current [6]. All those effects are normally embedded in μ_{eff} and L_{eff}. On the other hand, VA is usually considered a constant value, see Figure 2(a) and equation (10). This is an erroneous approach because VA also has the same effects of μ_{eff} and L_{eff} [6], and therefore, also dependent on bias and geometry, as Figure 2(b) shows. Equation (12), coming from (10) and (11), relates μ_{eff} and L_{eff} to VA in a very simple expression. The mobility μ and channel length L are μ_{eff} and L_{eff} in the exact point of saturation, assuming that there is no short channel effect on the saturation point, and also assuming that i_f is the same in saturation and deep saturation.

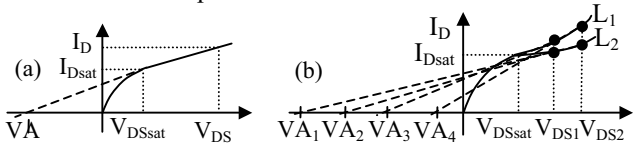


Figure 2. VA and I_D: (a) Ideal (b) Real

$$I_D = I_{Dsat}\left(\frac{V_{DS} - VA}{V_{DSsat} - VA}\right) \cong I_{Dsat}\left(1 - \frac{V_{DS}}{VA}\right) \quad (10)$$

$$\frac{I_D}{I_{Dsat}} = \frac{i_f \mu_{eff} n C'_{ox} \frac{\phi_t^2}{2}\frac{W}{L_{eff}}}{i_f \mu n C'_{ox} \frac{\phi_t^2}{2}\frac{W}{L}} = \frac{\mu_{eff}}{L_{eff}}\frac{L}{\mu} \quad (11)$$

$$\frac{\mu_{eff}}{L_{eff}} = \frac{\mu}{L}\left(1 - \frac{V_{DS}}{VA}\right) \quad (12)$$

Equation (12) shows that it is possible to refer all short channel effects to the Early voltage. The major advantage of this approach lies in the fact that the extraction of VA is easy to make either form simulations or from measurements. The designer can, therefore, work directly with points of VA for circuit design, and bypass models that are more adequate for simulators. A procedure used in the case of lack of appropriate models [7,8].

The problem now is how to determine a space of extraction for VA that is applicable to as many designs as possible. The Early voltage depends on the inversion level, channel length, drain-to-source voltage and temperature [6]. It is easy to set up a realistic range of values for these parameters according to practical limitations of the device, for instance: i_f between 1 and 1000, V_{DS} between 0 and the maximum voltage supply, and L normalized by the minimum length L_{min} between 1 and 9. The temperature, here, is a fixed value. Because i_f is independent of geometry, one set of extraction can be used for any design.

Figure 3 shows the Early voltage extracted from simulations for TSMC25 technology, L_{min}=0.3µm, run T21Q (MM_NON-EPI), using BSIM 3v3. Views of VA according to V_{DS} and i_f for each channel are provided.

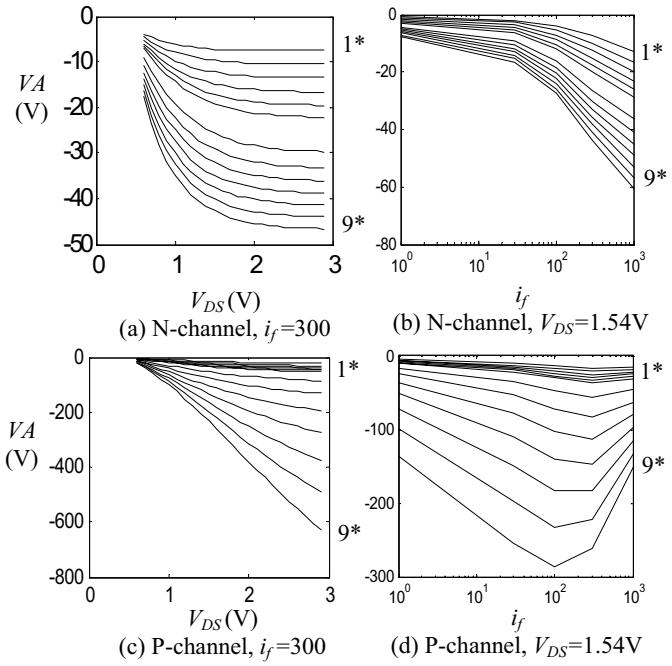


Figure 3. *VA=f(V_{DS}, i_f, L)*, at T=300K, *:L/L_{min}=1.0, 1.2, 1.4, 1.6, 1.8, 2.0, 3.0, 4.0, 5.0, 6.0, 7.0, 8.0, 9.0

In fact, the designer can extract more samples of i_f sweeping in V_{DS} and of V_{DS} sweeping in i_f. This kind of extraction provides not only a good view of the design space, but also actual values of VA for design purposes. Moreover, it is easy to conclude that a constant value of VA would work for few designs if compared with the universe of available values.

About the computational cost: Here 31 points of V_{DS}, 5 of i_f, 13 channel lengths, for each channel type, compose

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Figure 3. These are few points for today's computers, yet the points for VA are extensive.

3.2 The Influence in i_f X V_{GS}

It is easy to infer that the short channel effects for the device in saturation should also affect the relationship between i_f and V_{GS}, as seen in equations (4) and (5), for V_{GS} equal to V_{DS}. Figure 4 shows this case for the N and P channels of the TSMC 25 technology. The difference in i_f for one specific V_{GS}, considering the device with the longest channel as reference, can be around 50%. For instance: for V_{GS}=0.65V and N-channel, the i_f for L/L_{min}=8 is around 100, while for L/L_{min}=1 it is close to 50. A design based on the long channel model using the minimum length, in this case, would result in a drain current with half of the expected value.

The plots of Figure 4 provide all the information needed to correct any distortion in current due to short channel effects for any design. i_f guarantees geometry independence. In order to consider the body effect, some extra graphics with other values of V_{BS} may be made.

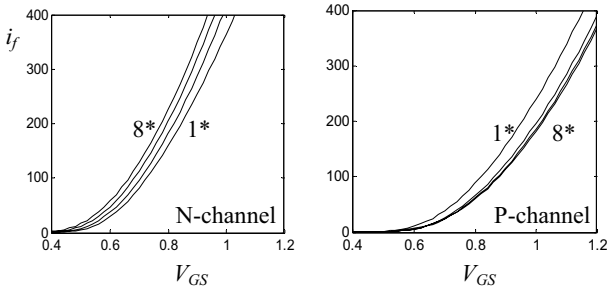

Figure 4. i_f for N, P MOS function of V_{GS}, at T=300K V_{BS}=0V, *:L/L_{min}=1.0, 2.0, 4.0, 8.0

4. Thermal Noise

The Early voltage can also models the short channel effects in the thermal noise. μ_{eff} and L_{eff} added to the noise for simulators [4,9], are regarded only as constants [5] in the design equations. Equation (12), here, also allows us to add second order effects in a long channel model for the thermal noise.

Equation (13) is first order model of the thermal noise. It is an approximation of (14) with the thermal noise coefficient γ equal to 2/(3n), by using (8), or $\gamma \cong 0.51$.

$$i_d^2 = 4KT(2/3)g_m\Delta f \quad (13) \qquad i_d^2 = 4KT\gamma g_{ms}\Delta f \quad (14)$$

The thermal noise in terms of normalized current can be found by developing (14) using (3) and (7), and knowing that ϕ_t=KT/q. The result is (15).

$$\frac{i_d^2}{8qI_S\Delta f} = \gamma\left(\sqrt{1+i_f}-1\right) \quad (15) \qquad \gamma = \frac{\mu_{eff}}{L_{eff}^2}\frac{Q_I}{g_{ms}} \quad (16)$$

Equation (16), for γ, takes into account the short channel effects and the total inversion layer charge Q_I, (17) [9].

$$|Q_I| = WL_{eff}C'_{ox}\,n\phi_t\left[\frac{2}{3}\left(\sqrt{1+i_f}+\sqrt{1+i_r}-\frac{\sqrt{1+i_f}\sqrt{1+i_r}}{\sqrt{1+i_f}+\sqrt{1+i_r}}\right)-1\right] \quad (17)$$

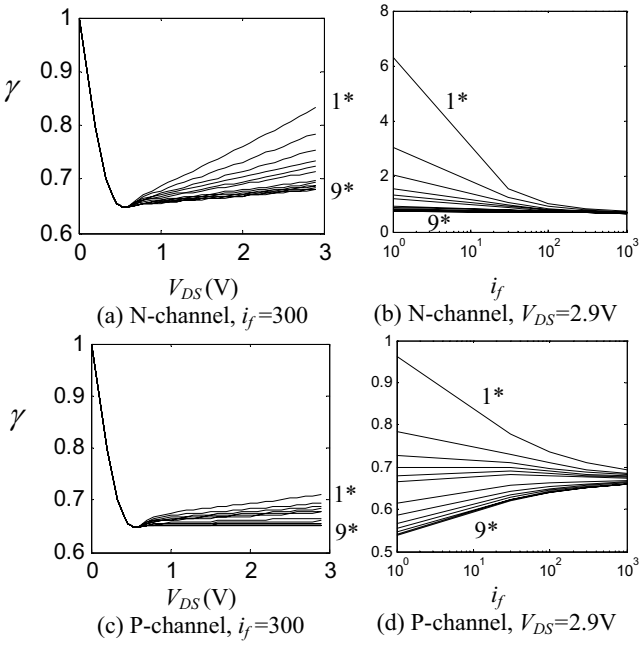

Figure 5. γ=f(V_{DS}, i_f, L), at T=300K, *:L/L_{min}=1.0, 1.2, 1.4, 1.6, 1.8, 2.0, 3.0, 4.0, 5.0, 6.0, 7.0, 8.0, 9.0

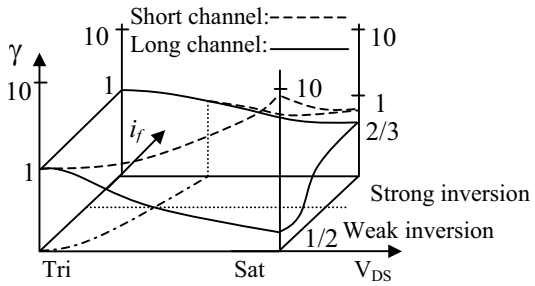

Figure 6. - Profile of γ for all regions of operation for long and short channel devices.

Equation (18) is a model for γ addressing secondary effects in terms of VA. It comes from (3), (7), (16) and (17), based on the assumption that, because g_{ms} operates with zero drain-to-source voltage, there is no short channel effect, in other words, g_{ms} is function of μ and L, thus resulting in the ratio $(\mu_{eff}L)/(L_{eff}\mu)$ in the expression of γ, which is related to VA according to equation (12). In saturation γ is given by (19).

$$\gamma = \left[\frac{2}{3}\left(\sqrt{1+i_f}+\sqrt{1+i_r}-\frac{\sqrt{1+i_f}\sqrt{1+i_r}}{\sqrt{1+i_f}+\sqrt{1+i_r}}\right)-1\right]\frac{1}{\left(\sqrt{1+i_f}-1\right)}\left(1-\frac{V_{DS}}{VA}\right) \quad (18)$$

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$$\gamma_{sat} = \frac{1}{3}\left(2 + \frac{1}{i_f} - \frac{\sqrt{1+i_f}}{i_f}\right)\left(1 - \frac{V_{DS}}{VA}\right) \quad (19)$$

Figure 5 comes from the combination of the expression (18) and the points of VA from Figure 3. The only difference is that V_{DS} is now equal to 2.9 for the profile of i_f. Figure 6 shows the expected behavior of γ for all regions of operation [9,10,11]. Figure 5 shows how both N and P channels match this profile accordingly.

5. The Common-Source Amplifier

The common-source (CS) amplifier, shown in Figure 7, is the base to explain the design methodology.

Transconductances and output conductances, the small signal parameters, as well as drain current and V_{GS}-V_T, the DC parameters, classically describes the MOSFET circuits. The use of the inversion level allows an equivalent formulation, except that the circuit is now described for all regions of operation, from weak to strong inversion. Circuit trade-offs are naturally stated because several MOSFET parameters are direct function of i_f. Also, the design space of i_f is well defined as explained in section 3. In the classical formulation, the designer searches for currents and geometries with no boundary values.

Equation (20) is the DC gain A_{VO} for the CS amplifier and equation (21) is the equivalent in terms of i_f. The practical range of VA in equation (21), set up according to section 3, can be easily found to show the limits of A_{VO} for this circuit for a certain technology. The designer defines limits for i_f and a maximum channel length. The voltages supply V_{DD} and V_{SS} determine the maximum V_{DS}. Equation (20) does not allow this kind of design space exploration. We may say that equation (21) is close to the device while equation (20) is close to the circuit specifications. Device tells the limitations of the technology and not circuit specifications.

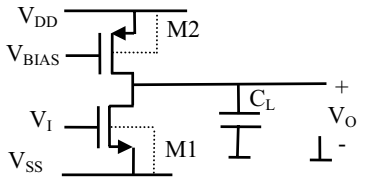

Figure 7. Common-Source (CS) Amplifier

$$A_{VO} = \frac{g_{m1}}{g_{O1} + g_{O2}} \quad (20) \qquad A_{VO} = \frac{1}{\phi_t n}\left(\frac{2}{\sqrt{1+i_{f1}}+1}\right)\left(\frac{1}{1/VA_1 + 1/VA_2}\right) \quad (21)$$

A real design scenario, though, presents more circuit requirements. For the sake of understanding of the design method, we are going to add voltage swing V_{SWING}, gain bandwidth product GBW, noise and power to our discussion. Though, more specs might be added. The voltage swing depends on the V_{DSsat}, which is a direct function of i_f, equation (6). For this circuit we have GBW=gm/(2πC_L). Power depends on the voltage supply and drain current, this last one function of i_f and geometry. Equation (22) is the input referred thermal noise $V^2_{N,in}$ for the CS amplifier. Equation (23) is $V^2_{N,in}$ now addressing the second order effects, where $[i^2_d/8qI_S]_1$ and $[i^2_d/8qI_S]_2$ are points from equation (15) using γ from the graphics for M1 and M2. I_{S1} and I_{S2} determine the value of the noise. This particular model for the thermal noise to work correctly needs to take into account the effect of the Early voltage from the drain current in the transconductance.

$$V^2_{N,in} = \left(i^2_{d1} + i^2_{d2}\right)\frac{1}{\left(g_{m1}\right)^2} \quad (22)$$

$$V^2_{N,in} = \left(8qI_{S1}\left[\frac{i^2_d}{8qI_S}\right]_1 + 8qI_{S2}\left[\frac{i^2_d}{8qI_S}\right]_2\right)\frac{1}{\left(\frac{1}{n}\frac{2I_{S1}}{\phi_t}\left(\sqrt{1+i_{f1}}-1\right)\left(1-\frac{V_{DS1}}{VA_1}\right)\right)^2} \quad (23)$$

Table 1. Variables: Device X Circuit.

Device				Circuit
V_{GS}, L, (V_{BS}) → i_f	i_f → V_{DSsat}	i_f, L, V_{DS} → VA, γ, f_t	i_f, L, V_{DS}, W → g_m, I_D, g_o, $i^2_d/\Delta f$	A_{VO}
				V_{SWING}
		[A_{VO},	[GBW,	GBW
	[V_{SWING}]	GBW_{MAX}]	Power, Noise]	Power
				Noise

Table 1 summarizes the relationship between device and circuit variables for the CS amplifier. Nevertheless, this table is valid for more complex structures. Variables on the right side of the brace are function of the ones on the left side. The trade-offs of the circuit are represented by the variables in the square brackets in the 'Device' side of the table. GBW_{MAX} is some fraction of f_T, here function of V_{DS} because of the influence of VA, see appendix.

One can notice that V_{DS} now becomes part of the design modeling. Section 3 showed that VA is function of V_{DS}. From equation (24) for the drain current of M1 and M2 with I_{Dsat1} equal to I_{Dsat2} comes equation (25), which presents the condition for the convergence of the circuit. For a given drain-to-source voltage for each transistor, the pair i_f and L should provide VA that satisfies equation (25).

$$I_{Dsat1}\left(1+\frac{V_{DS1}}{VA_1}\right) = I_{Dsat2}\left(1+\frac{V_{DS2}}{VA_2}\right) \quad (24) \qquad \frac{V_{DS1}}{VA_1} = \frac{V_{DS2}}{VA_2} \quad (25)$$

Equation (25) provides a relationship between DC bias and DC gain. Also, expressions similar to equation (25) can be developed for larger structures. The graphics presented in section 3 and equation (25) provided the device design space and the mathematical condition to solve the tuning during the hand calculation stage and not in front of a simulator. The tuning process of a circuit is somehow the search of VA to solve (25).

6. Design Methodology

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The methodology proposed here combines parameter extraction with analytical modeling. The extraction goes further than the range of inversion level for design purposes [7,8,12], it also covers a range of drain-to-source voltage, and the relationship i_f and V_{GS}. The steps to do the design are based on the influence of the device variables in the circuit as shown in Table 1, and it attempts to solve constraints prior to the simulations. The procedure suggested is:

1-Extract VA=f(i_f, L, V_{DS}) and i_f=f(L, V_{GS}, V_{BS});
2-Assign an expected V_{DS} for each transistor as well as an initial channel length;
3-Depending on the circuit, some transistors may have V_{GS} determined because of the V_{DS} chosen in step 2. In this case find i_f and VA based on their respective plots from step 1. Check the V_{DS} assigned in step 2 using equation (25), and requirements of V_{SWING}, A_{VO}, and GBW_{MAX}. If some V_{DS} or specs are not met, return to step 2;
4-For the transistors with V_{GS} not defined, search the pair (VA, i_f), in the plot VA=f(i_f, L, V_{DS}), that satisfies the V_{DS} of step 2, as well as the requirements of V_{SWING}, A_{VO}, and GBW_{MAX}. Get the V_{GS} in i_f=f(L, V_{GS}, V_{BS}) once i_f is found. If specs are not met, return to step 2;
5-Determine the widths that complies with GBW, noise and power, or provides the best trade-off among them.

7. Examples

7.1. Bias Point, DC Gain and Voltage Swing

Simulation results for the CS amplifier using BSIM3v3 illustrate the methodology. For TSMC25 technology the sheet normalization current I_{SQ}, I_S for W equal to L, for the NMOS and PMOS are I_{SQN}=62.20nA and I_{SQP}=22.26nA at 300K. Table 2 presents a design for V_{DS}=0.75V, L/L_{min}=4, and i_f=300 for each transistor. Figures 3 (a) and (c) provide VA_1 and VA_2 for these V_{DS} and L/L_{min}. With equations (7) and (8) we can determine g_m, and with equation (25) the maximum V_{Omax} and minimum V_{Omin} output voltages. The output swing is found according to the voltage gain, and V_{Omax} and V_{Omin} are determined by proportion of VA_1 and VA_2. Table 3 shows the results for a 10mVp input.

Table 2. Amp. Design1 for A_{VO}, V_{DD}=-V_{SS}=0.75V.

i_{f1}=i_{f2}	L/L_{min}	W_1(μm)	W_2(μm)	L_1=L_2(μm)	I_{BIAS}(μA)
300	4	50	140	1.2	777

Table 3. Design1: Theoretical X Simulation.

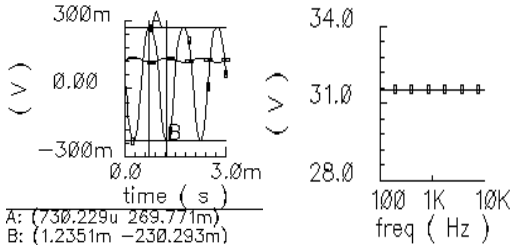
	I_D (μA)	VA_1 (V)	VA_2 (V)	g_{m1} (mS)	Vo_{max} (mV)	Vo_{min} (mV)	A_{VO}
Th.	777	-16.3	-27.1	2.75	270	-449	36
Sim.	769	-14.7	-15.9	3.17	269	-230	32

Table 4. V_{GS} and V_{DS}: Theoretical X Simulation.

	V_{GS1}(mV)	V_{GS2}(mV)	V_{DS1}(mV)	V_{DS2}(mV)
Th.	880.0	1120.0	563.4	936.6
Sim.	876.6	1123.8	686.5	813.5

From Figures 3 (a) and (c), for the same V_{DS}, the result is two distinct VA's, therefore, not satisfying equation (25) and explaining the errors in the VA's simulated. On the other hand, V_{Omax} and V_{Omin} simulated follow the proportion of VA_2 and VA_1 also simulated. The differences in g_m can be attributed to second order effects disregarded in the hand design. Figure 8 shows simulations for voltage swing and DC gain whose results are in Table 3.

Table 4 shows the results for the voltages of each transistor. V_{GS} for M1 and M2 come from Figure 4 for the specified i_f, and confirm the efficiency of the graphical solution once the errors are insignificant. The ratios V_{DS1}/VA_1 and V_{DS2}/VA_2 from the simulations are 46.7e-3 and 51.2e-3, respectively, hence validating equation (25).



(a) V_O Transient (10mVp input) (b) Frequency response, A_{VO}

Figure 8. Simulations for the CS amplifier.

7.2. VA and Gain Enhancement

Knowledge of the profile of the Early voltage is important before attempt to increase the DC gain by reducing the current [5]. For the CS amplifier with V_{DS}=1.54V, L/L_{min}=9, and i_f=300 for both transistors, we can take VA_1 and VA_2 from Figures 3 (b) and (d). If the current is reduced 3 times, meaning i_f from 300 to 100, the gain should increase 1.73 times according to (21) assuming VA_1 and VA_2 constant. However, carefully checking the characteristic of VA in this range of i_f, we see that VA for the NMOS reduces from 43.6V to 27.6V, a factor of 1.58. VA for the PMOS goes from to 261 to 288, here disregarded if compared to the one of the NMOS. The result is a DC gain that increases only 1.096 times. Table 5 is the design for this case.

Table 5. Amp. Design 2 for A_{VO}, V_{DD}=-V_{SS}=1.54V.

i_{f1}=i_{f2}	L/L_{min}	W_1(μm)	W_2(μm)	L_1=L_2(μm)	I_{BIAS}(μA)
300	9	13.5	37.7	2.7	93.3

Final Gain

Initial Gain

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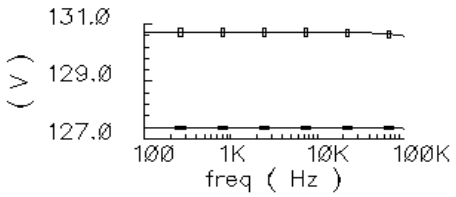

Figure 9. A_{VO} and the reduction of I_{BIAS}.

Figure 9 shows the simulations with almost no gain enhancement, as expected, whose results are summarized in Table 6. The VA_2 equal to 62 in the simulations can be explained by the convergence properties of equation (25).

Table 6. Design 2: Theoretical X Simulation.

	$I_D(\mu A)$	$VA_1(V)$	$VA_2(V)$	$g_{m1}(\mu S)$	Avo
Th. Initial	93.3	43.6	261	300	120
Sim. Initial	93.6	33.3	312	395	127
Th. Final	31.1	27.6	288	166	134
Sim. Final	31.0	23.8	62	234	130

7.3. Thermal Noise

To verify the noise model, equation (23), we tested several values of voltage supply in the CS amplifier of the first example now with minimum length and width reduced proportionally. The thermal noise using the regular model, equation (13), is 2.865nV/√Hz. The actual values, however, are higher as Table 7 and Figure 10 show. The agreement between calculations and simulations validates this modeling for the thermal noise.

Table 7. Noise: Calculations X Simulations.

V_{DD} (V)	$\left[\frac{i_d^2}{8qI_S\Delta f}\right]_1$	$\left[\frac{i_d^2}{8qI_S\Delta f}\right]_2$	VA_1 (V)	$\sqrt{V_{N,in}}^2{}_{CALC}$ (nV/√Hz)	$\sqrt{V_{N,in}}^2{}_{SIM}$ (nV/√Hz)
0.9	11.1	11.0	-5.86	3.220	3.193
1.2	11.4	11.1	-6.85	3.158	3.172
1.5	11.8	11.2	-7.15	3.108	3.137
1.8	12.2	11.3	-7.35	3.052	3.115
2.1	12.5	11.4	-7.51	2.980	3.099
2.4	12.9	11.4	-7.68	2.913	3.089

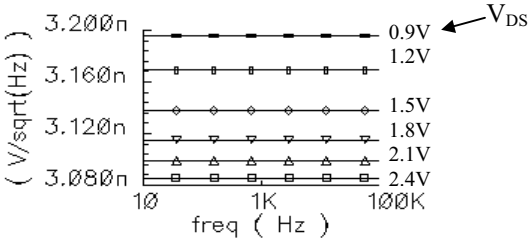

Figure 10. Noise for several values of V_{DS}.

8. Conclusions

This paper has presented a novel approach to take into account short-channel effects to design MOSFET circuits. Examples based on normalized curves were presented showing that it is possible to precisely design a circuit for gain and noise with few points of extraction and simple models. Moreover, few plots based on the inversion level can solve a wide variety of designs. The trade-offs of the circuit were related to the limitations of the device. A DC condition for the drain-to-source voltage and Early voltage were successfully applied to model an amplifier. Graphics for the gate-to-source voltage also presented accurate results. Common-source amplifier design and simulations validate the method.

Appendix - Intrinsic Cutoff Frequency

The short-channel effects in g_m also affect the intrinsic cutoff frequency once f_t is equal to $g_m/(C_{GS}+C_{GB})$. Therefore, ft given by equation (9) is better described by μ_{eff} and L_{eff} instead of μ and L. Equation (A.1), which shows that f_t is also function of V_{DS} [11], is the result of the assumption of $L_{eff}^2 \cong L_{eff}L$ in equation (9) and by using (12) to eliminate the ratio $\mu_{eff}/L_{eff.}$

$$f_T = \frac{\mu\phi_t}{2\pi L^2} 2\left(\sqrt{1+i_f}-1\right)\left(1-\frac{V_{DS}}{VA}\right) \qquad (A.1)$$

9. References

[1] P. L. Levin and R. Ludwig, "Crossroads For Mixed Signal Chips", IEEE Spectrum, pp. 38-43, March 2002.

[2] B. Martin, "Automation Comes to Analog", IEEE Spectrum, pp. 70-75, June 2001.

[3] A.I.A. Cunha.; Schneider, M.C.; Galup-Montoro, "An MOS transistor model for analog circuit design" IEEE Journal of Solid-state Circuits, vol. 33, No. 10, October 1998.

[4] BSIM 3V3.2.2 Mosfet Model User's Manual; University of California, Berkeley, USA, 1999.

[5] R. J. Baker, H. W. Li, D. E. Boyce, "CMOS – Circuit Design, Layout and Simulation", IEEE press 1998."K. Martin, D. A. Johns, "Analog Integrated Circuit Design", John Wiley & Sons, Inc, 1997.

[6] Schneider, M.C.; Galup-Montero, C.; Filho, O.C.G.; Cunha, A.I.A. A single-piece charge-based model for the output conductance of MOS transistors Electronics, Circuits and Systems, 1998 IEEE International Conference on, Volume: 1, 1998.

[7] J. P. Eggermont, D. D. Ceuster, D. Flandre, B. Gentine, P G. A. Jespers, J. P. Colinge, "Design of SOI CMOS Operational Amplifiers for Applications up to 300°C", IEEE Journal of Solid-State Circuits, vol. 31, no 2 February 1996.

[8] F. Silveira, D. Flandre, and P. G. A. Jespers, "A g_m/I_D Based Methodology for the Design of CMOS Analog Circuits and Its Application to the Synthesis of a Silicon-on-insulator Micropower OTA", IEEE Journal of Solid-State Circuits, vol. 31, no 9 September 1996.

[9] Bing Wang, James Hellums and Charles Sodini, "MOSFET Thermal Noise Modeling for Analog Integrated Circuits," IEEE Journal of Solid-state Circuits, vol. 29, No. 7, July 1994.

[10] Chih-Hung Chen; Deen, M.J. "Channel noise modeling of deep submicron MOSFETs**",** IEEE Transactions on Electron Devices, vol. 49, No. 08, August 2002.

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[11] A. A. Abidi, “High-Frequency Noise Measuremet on FET’s with Small Dimensions,” IEEE Transactions on Electron Devices, vol. Ed-33, No. 11, Nov. 1986.
[12] Operational amplifier power optimization for a given total (slewing plus linear) settling time Silveira, F.; Flandre, D.; Integrated Circuits and Systems Design, 2002. Proceedings. 15th Symposium on , 2002 Page(s): 247 -253

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