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***Abstract*—State-of-the-art high power density AC/DC and DC/AC converter systems typically employ Triangular Current Mode (TCM) modulation or conventional PWM. TCM is characterized by a wide variation of switching frequency over the mains period and ensures soft-switching in all operating points, but results in increased conduction and high-frequency losses due to the necessary large current ripple. In contrast, PWM with constant switching frequency features a lower RMS current and thus reduced conduction losses, but cannot achieve soft-switching over the entire mains period and suffers from turn-on losses. In this paper it is investigated if an optimal combination of these two operating modes, i. e. an optimal adjustment of switching frequency and/or current ripple amplitude throughout the mains period, can lead to an increase in conversion efficiency and how such an Optimal Frequency Modulation (OFM) control scheme can be implemented in practice. The presented analysis is based on an ultra compact 2kW, 400V DC/AC converter system designed to overcome the GOOGLE Little Box Challenge.**

***Index Terms*—Optimal Frequency Modulation, Efficiency Optimal Switching Frequency, Optimal Current Ripple Modulation, Minimum Loss Control**

I. Introduction

In kW-scale high power density AC/DC and DC/AC converter systems, typically a high switching frequency is selected in order to ensure a small size of the passive components [1]. As a consequence, Zero Voltage Switching (ZVS) of the power semiconductors over the entire mains period is desired to reduce switching losses and keep the conversion efficiency high and the volume of the cooling system small. Following this design philosophy, and with the insights gained from Pareto optimization results, a $8.2\,\mathrm{kW/dm^3}(134\,\mathrm{W/in^3})$ single-phase Triangular Current Mode (TCM) PV inverter was realized in [2] to overcome the GOOGLE Little Box Challenge (GLBC) [3]. Further research conducted in the aftermath of the GLBC revealed that by means of an alternative inverter topology based on a DC/|AC| buck-stage with subsequent |AC|/AC unfolder (cf. Fig. 1) the power density of the 2 kW PV inverter can be further improved. The buck-stage, highlighted in light blue in Fig. 1, is operated either with TCM modulation or conventional PWM with large current ripple, and is controlled such that the output voltage v_{C0} follows a rectified sinusoidal shape. In order to deal with reactive loads and retain full controllability of the inductor current, v_{C0} is actually kept above a defined voltage $v_{\mathrm{C0,min}}$ around the Zero Crossings (ZC) of the mains voltage as indicated in Fig. 1 (b). During this interval, the |AC|/AC unfolder initiates PWM operation in order to ensure a sinusoidal shape of v_{ac} at the converter output. The Pareto optimization presented in [2] identified that if the buck-stage is operated with PWM at EMI friendly $140\,\mathrm{kHz}$ and a $50\,\mu\mathrm{H}$ inductor is installed, a staggering power density of $14.7\,\mathrm{kW/dm^3}$ $(241\,\mathrm{W/in^3})$ at $98.1\,\%$ efficiency can be expected. Interestingly, TCM operation of the buck-stage with a $10\,\mu\mathrm{H}$ inductor results in a slightly lower power density $(14.0\,\mathrm{kW/dm^3})$. The resulting inductor current i_{L} and switching frequency variation over a mains period for the PWM and TCM design of the buck-stage are shown in Fig. 2 (a) and (b) for a $2\,\mathrm{kW}$ ohmic load. As it becomes evident from Fig. 2 (a), PWM features lower conduction and winding losses due to the comparably small current ripple and thus lower RMS value of the inductor current. However, a hard turn-on of the high-side transistor over a wide range of the mains period results in high switching losses. Regarding efficiency it might be beneficial to lower f_{s} between $1/8T_{\mathrm{m}}$ and $3/8T_{\mathrm{m}}$ in order to increase the current ripple and extend the region where ZVS applies. On the contrary, operation of the buck-stage with TCM modulation as shown in Fig. 2 (b) enables ZVS in all operating points throughout mains period, but the large current ripple significantly increases conduction and winding losses. In this case, it might be beneficial, in terms of overall efficiency, to limit the drop of f_{s} around the peak of the mains voltage (at $1/4T_{\mathrm{m}}$ and $3/4T_{\mathrm{m}}$) in order to decrease the current ripple despite ZVS is intermittently lost. Accordingly, the question arises, whether the benefits of TCM and PWM can be combined, if the switching frequency variation is considered as an additional degree of freedom to effectively minimize the power loss in the inverter at every instant in time over the course of the mains period. In [4] an optimal switching frequency for a full-bridge inverter was derived analytically by means of a sophisticated time-domain current ripple analysis. However, solely power losses in the transistors due to hard switching were considered in the optimization. The authors in [5] also included the power loss of the inductor in the analytical optimization. However, again, only hard-switching operation of the power transistors was considered. The optimal variable switching frequency for a 3-phase GaN based TCM inverter was derived in [6] based on approximate loss models of the involved power transistor

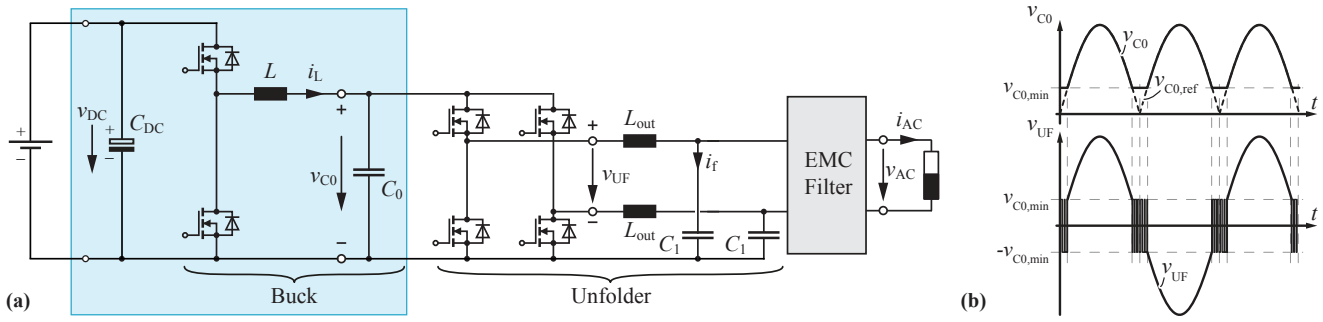

Fig. 1. (a) Inverter topology based on a DC/|AC| buck stage and a subsequent |AC|/AC full-bridge unfolder. (b) Buck stage output voltage and unfolder output voltage showing intermediate PWM operation around the zero-crossing of the mains.

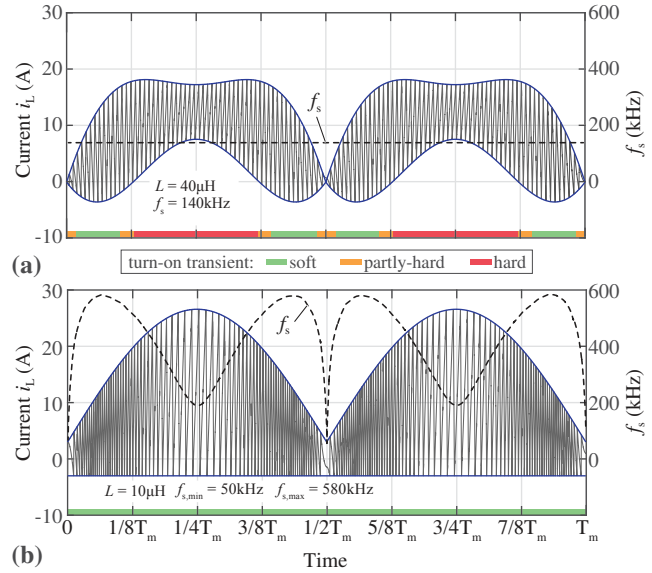

Fig. 2. Inductor current i_{L} and the variation of switching frequency f_s throughout a mains period T_{m} obtained for the Pareto optimal TCM and PWM DC/|AC| buck stage when operated at rated power, respectively.

and magnetic components. However, since ZVS operation was enforced in all operating points, the optimal trade-off between power transistor and filter component losses has not been completely investigated.

In this paper the optimal switching frequency variation is determined empirically by means of experimental hardware rather than based on mathematical loss models and simulations. Since it promises highest power density, the buck-unfolder inverter design with PWM operation of the buck stage presented in [2] will be the basis for the study presented in the following. In particular, the optimal switching frequency of the buck stage (cf. Fig. 1 (a)) in order to achieve loss minimal operation at every instant in time over the mains period is determined. Power losses in the remaining converter components, for instance conduction losses in the unfolder and losses in the subsequent EMC filter are assumed to be unaffected by the switching frequency of the buck stage and are therefore excluded from further consideration. The reader should be aware that EMI compliance imposes a stringent side condition which restricts the feasible range of switching frequency variation and/or requires a reevaluation of the EMC filter afterwards which possibly leads to a decrease in power density of the overall inverter. However, the EMC filter of the buck-unfolder inverter, considered herein, is dimensioned such to provide enough attenuation to handle the intermediate High Frequency (HF) switching of $v_{\mathrm{C0,min}}$ of the unfolder (cf. Fig. 1 (b)) and therefore provides enough margin to accommodate for a wide range of switching frequency variation in the DC/|AC| buck stage.

The loss minimization procedure based on switching frequency variation in quasi-stationary DC/DC operating points is outlined in Section II of this paper. The employed experimental test setup of the buck converter is introduced afterwards in Section III. The empirically obtained optimal switching frequency and the resulting inductor current envelope as a function of the point in time t_{k} and/or angle considered within a main period T_{m} are presented and discussed in Section IV. Finally, two control approaches to implement Optimal Frequency Modulation (OFM) in practice are briefly introduced in Section V.

II. Quasi-Stationary DC/DC Analysis

Since the buck-stage output voltage v_{C0} changes very slowly throughout T_{m} with respect to the actual switching period $T_{\mathrm{s}} = 1/f_{\mathrm{s}}$, the DC/|AC| operation of the buck converter can be approximated by a large number of consecutive, quasi-stationary DC/DC operating points defined by the DC-link voltage, the buck stage output-voltage

$$v_{\mathrm{C0}} \approx \max(v_{\mathrm{C0,min}}, |v_{\mathrm{AC}}(t_{\mathrm{k}})|), \tag{1}$$

and the average inductor current

$$\overline{i_L} = \operatorname{sgn}(v_{\mathrm{AC}}(t_{\mathrm{k}})) \cdot (i_{\mathrm{AC}}(t_{\mathrm{k}}) + i_{\mathrm{f}}(t_{\mathrm{k}})) \tag{2}$$

$$\approx \operatorname{sgn}(v_{\mathrm{AC}}(t_{\mathrm{k}})) \cdot i_{\mathrm{AC}}(t_{\mathrm{k}}) \tag{3}$$

at distinct points t_{k} over the mains period. Due to symmetry, it suffices to consider only the interval $\varphi = \omega t = [0, \pi/2]$ of the mains. In this paper, only operating points resulting from a purely ohmic 0.25 kW, 1.0 kW and 2.0 kW load are considered as illustrated in Fig. 3 (a). Furthermore, the reactive current demand of the EMC filter is neglected. In a

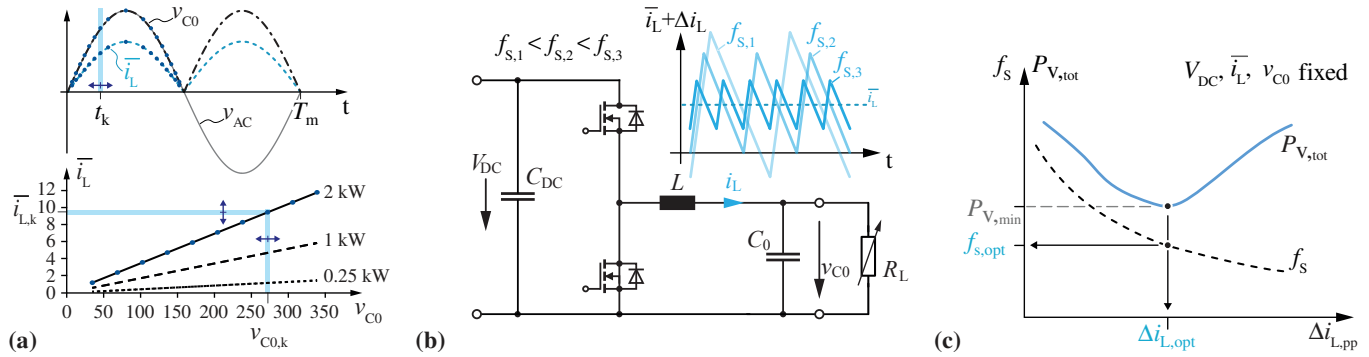

Fig. 3. Determining the switching frequency / current ripple which minimizes the total power loss of the DC/|AC| buck stage in a quasi-stationary DC/DC operating point. (a) Derived DC/DC operating points V_{DC}, $v_{C0,k}$ and $\overline{i_{L,k}}$ for ohmic load at several distinct points t_k throughout the mains period T_m. (b) Resulting current ripple amplitude for switching frequency variation in a specific DC/DC operating point. (c) Variation of the switching frequency in order to determine the loss minimum in a given DC/DC operating point.

stationary operating point, the switching frequency of the buck stage can be varied which results in different current ripple amplitudes in the filter inductor L as illustrated in Fig. 3 (b). The switching frequency $f_{s,opt}$ and current ripple amplitude $\Delta i_{L,opt}$ which minimizes the total power loss in the buck stage in the selected DC/DC operating point is considered optimal as shown in Fig. 3 (c). After repeating the measurement and/or optimization procedure for all defined DC/DC operating points, the individual $f_{s,opt}$ points are joined and interpolated in order to obtain the optimal switching frequency variation over the course of the mains period.

The quasi-stationary DC/DC approach implicates the following approximations. The dielectric loss in the filter capacitor C_0 due to the rectified sinusoidal voltage swing of v_{c0} is not covered by the quasi-stationary DC/DC approach. However, these losses are in a first approximation not affected by the switching frequency and can thus be treated as additional constant power loss. The winding losses in the inductor caused by the low-order spectral components in $\overline{i_L}$ are also not correctly covered, since the losses are caused solely by the DC winding resistance, $R_{w,DC}$, in the respective DC/DC operating point. Since the amplitude of the harmonics of $\overline{i_L}$ drops with $1/n^2$ and the frequency dependent winding resistance $R_{w,AC}(n \cdot f_m)$ is approximately constant up to several kHz, the resulting error is less than $1\,\%$ as a numeric calculation revealed. Furthermore, harmonic sidebands, present in the current spectrum due the modulation of the rectified sinusoidal variation of the duty-cycle during regular operation, are missing in case of the quasi-stationary analysis even if a large number of DC/DC operating points is considered because the duty-cycle is kept constant during the measurements and the spectral energy is located solely at multiples of the switching frequency. However, since the considered switching frequency range is much higher compared to the low-frequency harmonics in the baseband, the additional sidebands do not noticeably affect the losses. Moreover, the operating temperature of the power electronic components during the individual measurements of the quasi-stationary analysis (kept between $35\,°C$ – $45\,°C$ in every considered operating point) likely differs from the device temperature resulting from regular operation of the buck stage (max. $65\,°C$ according to [3]).

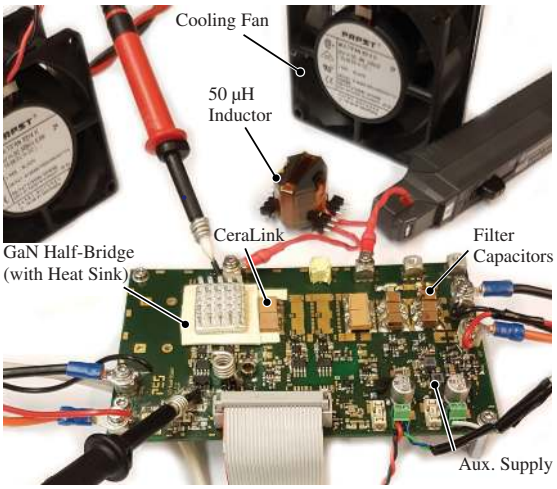

Fig. 4. **(a)** Picture of the experimental test setup showing the implemented buck converter (GaN half-bridge with externally connected inductor) with cooling fans and measurement probes. The employed DC source, electronic load and power analyzer are not shown.

III. Experimental Setup

The half-bridge circuit of the buck converter (cf. Fig. 1) is realized with normally-off gallium nitride gate (GaN) injection transistors (CoolGaN Samples from Infineon) in combination with a novel high-performance gate drive circuit, where two GaN transistors are connected in parallel per switch. The employed $50\,\mu H$ HF inductor is realized with 27 turns (3 layers with each 9 turns) of $180 \times 71\,\mu m$ litz wire on a RM10 N87 ferrite core. The DC-link capacitor $C_{DC} \approx 10\,\mu F$ is realized with individual $2\,\mu F/650\,V$ CeraLink capacitors featuring exceptional low ESR at high frequencies and elevated operating temperatures. It should be noted that C_{DC} is dimensioned to filter switching frequency noise and not to cope with the double-mains frequency power pulsation intrinsic to single-phase systems. The buck stage filter capacitor $C_0 \approx 20\,\mu F$ is composed of 12 parallel connected $2.2\,\mu F/450\,V$ X6S MLCCs. As mentioned in the introduction, the system parameters of the buck stage are in accordance with

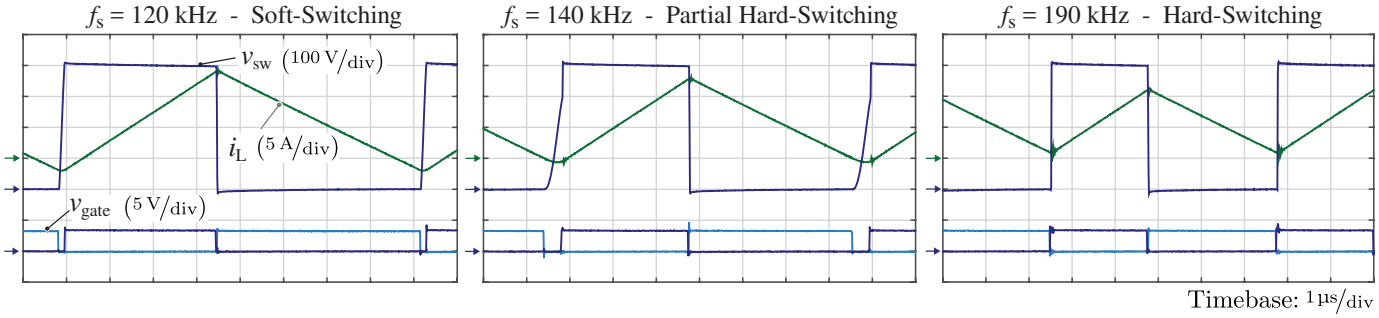

Fig. 5. Measured switch-node voltage v_{sw}, inductor current i_{L} and gate voltages in the DC/DC operating point $V_{\mathrm{DC}} = 400\,\mathrm{V}$, $v_{\mathrm{C0}} = 170\,\mathrm{V}$, $\overline{i_{\mathrm{L}}} = 5.9\,\mathrm{A}$ obtained with 120 kHz, 140 kHz and 190 kHz switching frequency.

the Pareto optimal buck-unfolder inverter design presented in [2]. The experimental test setup including cooling fans and attached measurement probes is depicted in Fig. 4. The duty-cycle of the half-bridge and an electronic load (Chroma 63202) are adjusted to meet the correct output voltage and output power (average inductor current) in every DC/DC operating point. Depending on the specific operating point and selected switching frequency, the rising- and falling-edge dead-time of the half-bridge, $t_{\mathrm{d,r}}, t_{\mathrm{d,f}} \in [20\,\mathrm{ns}, 400\,\mathrm{ns}]$, are adapted such to ensure a complete resonant transition of the drain-source voltage and, in addition, minimize the conduction time of the anti-parallel diode. In case that i_{L} remains strictly positive and hard-switching occurs, the rising-edge dead-time is set to the minimum value. The average power loss of the buck converter in every DC/DC operating point is measured with a Yokogawa WT3000 power analyzer. Auxiliary power for the digital control card and the gate drives are also included in the total power losses. Once the operating point of the buck converter is set, the total power loss at steady-state operation is recorded for several switching frequencies until a distinct loss-minimum can be identified. Fig. 5 shows experimental waveforms of the buck converter operating at $V_{\mathrm{DC}} = 400\,\mathrm{V}$, $v_{\mathrm{C0}} = 170\,\mathrm{V}$, $\overline{i_{\mathrm{L}}} = 5.9\,\mathrm{A}$ and switching frequencies of 120 kHz, 140 kHz and 190 kHz. It can be seen how the triangular ripple, and consequently the RMS value, of the inductor current reduces with increasing switching frequency. The depicted switch-node voltage v_{sw} reveals that the power-stage experiences complete soft-switching when operated with 120 kHz. If f_{s} is increased to 140 kHz, the slightly negative value of i_{L} at the start of the low- to high-side switching transition does not suffice to achieve a complete resonant transition of the the switch-node voltage for $t_{\mathrm{d,r}} = 400\,\mathrm{ns}$ and partial hard-switching occurs. Operating the buck converter with 190 kHz results in a hard turn-on of the high-side transistor since i_{L} remains above zero due to the reduced amplitude of the triangular ripple. In the DC/DC operating point examined in Fig. 5, the optimal loss trade-off between power transistors and filter components is attained with $f_{\mathrm{s}} = 140\,\mathrm{kHz}$.

IV. Empirically Determined Optimal Switching Frequency

Following the quasi-stationary approach, the loss-minimal switching frequency, $f_{\mathrm{s,opt}}$, was determined at 10 distinct DC/DC operating points within the interval $[0, \pi/2]$ of the mains period for an average output power of 250 W, 1 kW and 2 kW. The experimental results with interpolation between the discrete measured points are shown in Fig. 6. It should be noted that for a clearer visual representation, the measured points were mirrored at $\pi/2$ to complement the interval $[0, \pi]$. The switching frequency variation and instantaneous power loss in the buck converter when operated with a fixed switching frequency of 140 kHz (plotted in red) and with varying optimal switching frequency (plotted in sky-blue) are shown in Fig. 6 (a) and (b), respectively. The corresponding envelope of the inductor current is displayed in Fig. 6 (d)-(f) for the three measured output power levels. At 2 kW rated power, $f_{\mathrm{s,OFM}} = f_{\mathrm{s,opt}}(\varphi)$ falls below 140 kHz over a wide range of the considered phase angle. Saturation of the power inductor limits the switching frequency to fall below 70 kHz at $\omega t = \pi/2$. Observing the current ripple envelope of both PWM and OFM in Fig. 6 (d), it can be inferred that OFM tends to extend the interval where soft-switching applies despite the increased RMS value of the inductor current. As listed in Tab. I, the total losses in the buck converter decrease by roughly 14 % when operating with a variable switching frequency $f_{\mathrm{s,OFM}}$ instead of $f_{\mathrm{s,PWM}} = 140\,\mathrm{kHz}$. The loss distribution in Fig. 6 (c), calculated with experimentally verified mathematical loss model of the GaN transistors and power inductor, indicates that OFM significantly reduces the switching and core losses while it slightly increases the conduction and HF winding losses due to the larger current ripple. At half the nominal output power i.e. 1 kW, the optimal frequency curve exceeds $f_{\mathrm{s,PWM}}$ in the vicinity of $\pi/6$ reaching a peak of 243 kHz. Similar as before, the optimal frequency drops below 140 kHz in the interval $[\pi/3, 2\pi/3]$ and reaches the lowest value of 70 kHz at $\pi/2$. At 1 kW output power, 22 %

TABLE I
Frequency variation and loss saving of OFM for different output power levels

P_{out} (W)	$f_{\mathrm{s,OFM}}$ (kHz)	P_{v} (W) @ 140 kHz	P_{v} (W) @ $f_{\mathrm{s,OFM}}$	ΔP_{v} (W / %)
2000	[70, 149]	24.0	20.6	3.4 / 13.7
1000	[70, 243]	10.8	8.4	2.4 / 22.0
250	[140, 500]	6.5	5.5	1.0 / 15.7

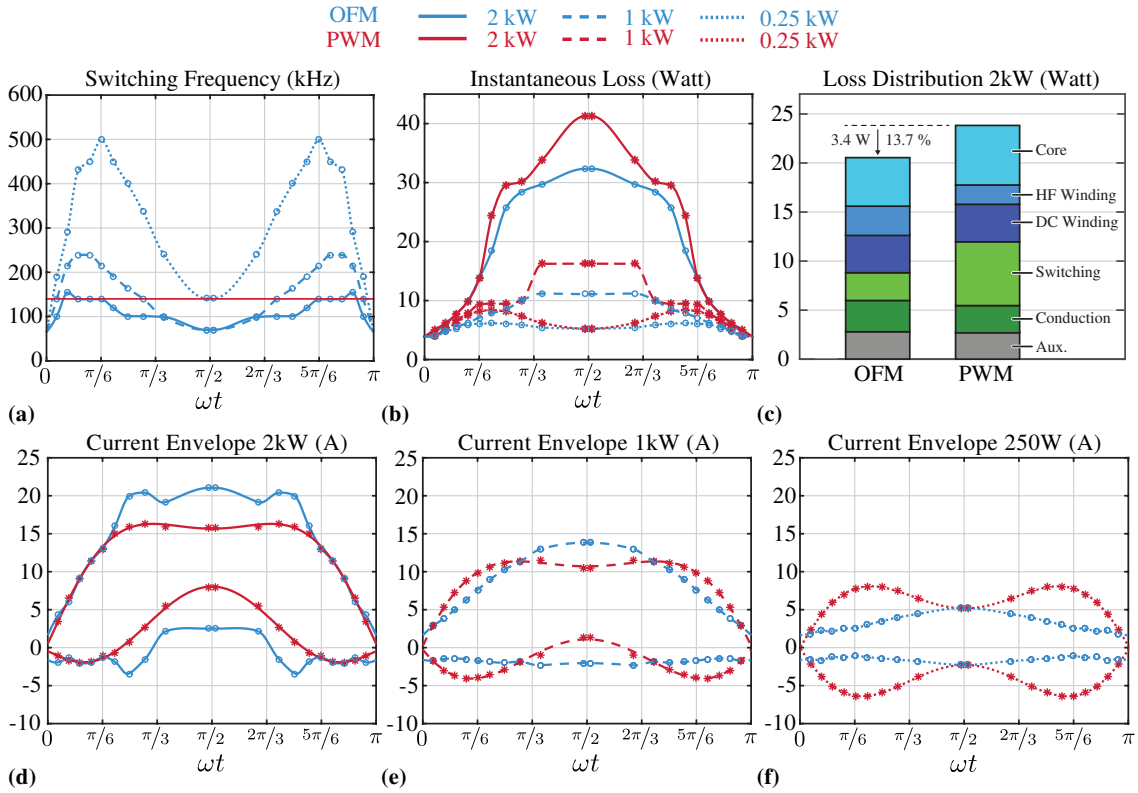

Fig. 6. Experimental results obtained with the test hardware depicted in Fig. 4 showing the optimal switching frequency $f_{\mathrm{s,OFM}} = f_{\mathrm{s,opt}}(\varphi)$ in (a), the total instantaneous power loss in the buck converter in (b), and the resulting envelope of the current ripple in (d)-(f) over the interval $\varphi \in [0, \pi]$ for 2 kW (solid lines), 1 kW (dashed lines) and 0.25 kW (dotted lines) ohmic load. The distribution of power loss between the individual components of the buck converter at 2 kW output power is shown in (c) for both OFM and 140 kHz PWM.

of losses can be saved when the converter is operated with $f_{\mathrm{s,OFM}}$ (cf. Tab. I). At 250 W part-load operation, $f_{\mathrm{s,OFM}}$ exceeds 140 kHz almost over the entire interval, attaining a peak of 500 kHz at $\omega t = \pi/6$ where $v_{\mathrm{C0}} = V_{\mathrm{DC}}/2$. As listed in Tab. I, nearly 16 % of the total power loss can be saved when operating the buck stage with OFM at 250 W output power.

V. Digital Control Implementation of OFM

The empirically determined optimal switching frequency, $f_{\mathrm{s,OFM}}$, and/or optimal current envelope, $\Delta i_{\mathrm{L,OFM}}$, is stored in form of a 3-dimensional Look-Up Table (LUT) in a fast, microcontroller accessible memory in order to provide the data to the digital controller. Every sample in the set defined by all feasible operating points, $\{V_{\mathrm{DC}}, v_{\mathrm{C0}}, \overline{i_{\mathrm{L}}}\}$, defines a single entry of $f_{\mathrm{s,OFM}}/\Delta i_{\mathrm{L,OFM}}$ in the LUT. Taking the actual value of V_{DC} into consideration allows to adapt for a possible double line-frequency variation and/or output power dependent sag of the DC-link voltage. However, for the sake of simplicity, the DC-link voltage is fixed to 400 V in this paper as already mentioned in the previous section which reduces the LUT to two dimensions. A graphical representation of the 2-dim $f_{\mathrm{s,OFM}}$-LUT obtained from interpolation of the measured data at 0.25 kW, 1.0 kW and 2 kW (cf. Fig. 6) is illustrated by means of a contour plot in Fig. 7. Since $f_{\mathrm{s,OFM}}$ was determined only for ohmic load, the combination of $\overline{i_L}$ and v_{C0} which would occur for a non-unity Power Factor ($-0.7 <$ PF < 0.7, [3]), is indicated by means of the grey-shaded

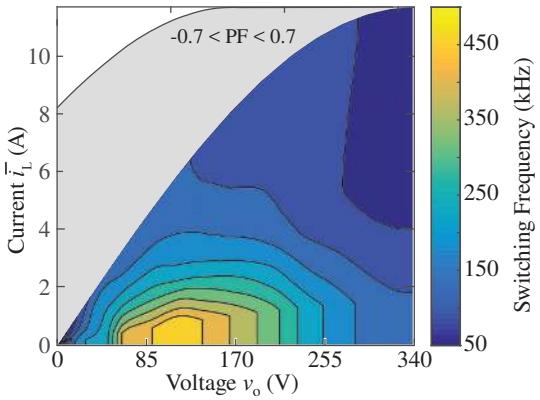

Fig. 7. Contour plot representation of the look-up table obtained from two-dimensional interpolation of the empirically determined $f_{\mathrm{s,OFM}}$ (cf. Fig. 6) as a function of $\overline{i_{\mathrm{L}}}$ and v_{C0}.

area. The envisioned digital control implementation of OFM is depicted in Fig. 8 (a) and follows a similar control structure as employed in classical PWM control. For the sake of clarity, the unfolder (cf. Fig. 1) and additional cascaded control loops to regulate voltages and currents in the EMI filter are omitted in this discussion. A more detailed description can be found in [7]. Moreover, it is assumed that the EMI filter does not affect the low-frequency harmonics in the buck stage output voltage, hence $v_{\mathrm{C0}} \approx v_{\mathrm{o}}$. The outer voltage and inner current control loop determine the modulation index d such that on

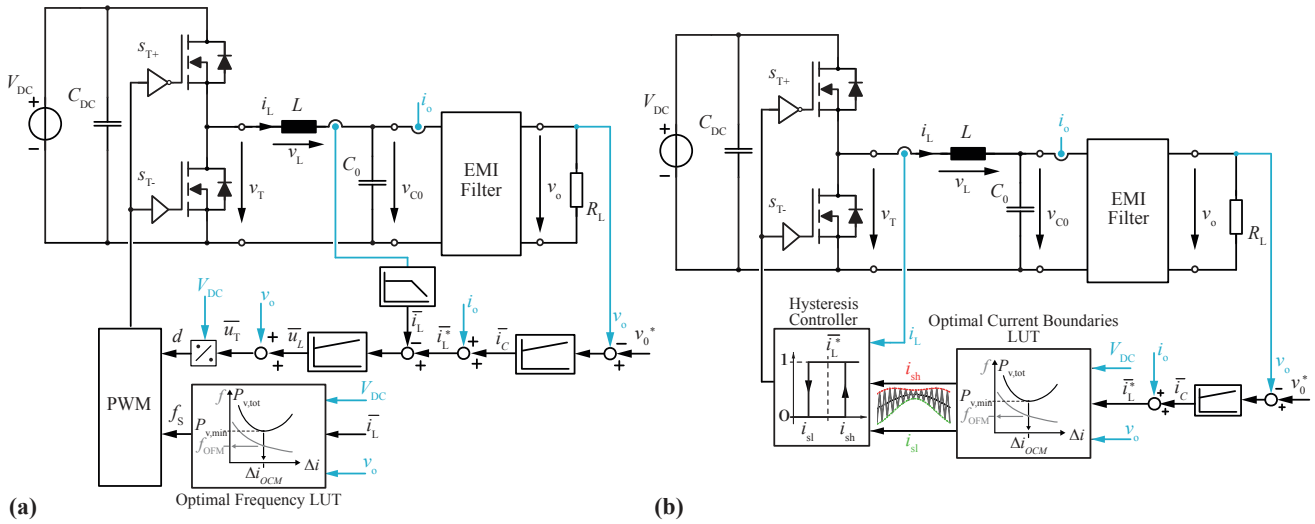

Fig. 8. Control implementation of OFM by means of conventional PWM with adjustable switching frequency in (a) where the optimal switching frequency is stored in a Look-Up Table (LUT), and by means of a hysteresis controller in (b) where the optimal upper and lower current boundary are accessed from a pre-computed LUT.

average over a switching period $\overline{v_\mathrm{T}}$ is applied by the power-stage. In contrast to classical PWM, the carrier frequency is not fixed but permanently updated from the stored LUT for the measured operating point $\left\{V_\mathrm{dc}, v_\mathrm{o}, \overline{i_L}\right\}$. The carrier frequency can be kept for a specified number of switching cycles before a new value is assigned to the PWM modulator from the LUT. Since the PWM frequency varies over time, the control law is executed asynchronously with defined frequency. Another option is to store the optimal envelope i.e. upper and lower boundary of the inductor current as shown in Fig. 6 (d)-(f) in the LUT instead of $f_\mathrm{s,OFM}$ and use a hysteresis regulator to control the power-stage such that the inductor current remains inside the boundaries. This control strategy, herein termed Optimal Current amplitude Modulation (OCM), is outlined in Fig. 8 (b). For highest performance, the hysteresis controller can be implemented with analog comparator circuits where the switching thresholds are continuously adjusted by means of digital-to-analog conversion of the LUT values provided by the microcontroller. This approach allows to tightly control i_L, but demands a current sensor with very high bandwidth.

VI. Conclusion

It has been shown that by combining the benefits of two well known and accepted switch-mode power converter modulation techniques, namely Triangular Current Mode (TCM) and Pulse Width Modulation (PWM), the overall conversion efficiency of a single-phase DC/AC converter can be improved. The presented novel operating mode, herein named Optimal Frequency Modulation (OFM), is characterized by a continuous adjustment of the actual switching frequency over the course of the mains period in order to minimize the converter power loss. Being relieved from the remaining inaccuracy and uncertainty of mathematical loss models, an experimental approach to determine the optimal switching frequency, $f_\mathrm{s,OFM}$, was presented. A quasi-stationary DC/DC approach was applied to the buck stage of a Pareto optimal 2 kW, single-phase DC/AC converter design comprising a DC/|AC| buck stage and a |AC|/AC unfolder. The total power loss can be reduced by 13.7 % at 2 kW output power when operated with $f_\mathrm{s,OFM}$. The potential loss saving increases to remarkable 22 % at half the rated power and reduces just slightly to 16 % at 250 W. Finally, two practical look-up table based control implementations of the proposed operating mode, PWM with updated carrier frequency and current hysteresis control with variable hysteresis width were presented. Naturally, the OFM approach presented herein can also directly be applied to single-phase PFC rectifier and DC/DC converter systems.

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