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Novel empty substrate integrated waveguide for high performance microwave integrated circuits

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Abstract—In the last years a great number of substrate integrated circuits has been developed. These new circuits are a compromise between the advantages of classical waveguide technologies, such as high quality factor and low losses, and the advantages of planar circuits, such as low cost and easy compact integration. Although their quality factor and losses are better than for planar circuits, these characteristics are worse than in the case of waveguides, mainly due to the presence of the dielectric substrate. In order to improve the performance of the integrated circuits, a new methodology for manufacturing empty waveguides, without dielectric substrate, but at the same time completely integrated in a planar substrate is proposed in this work. A wide band transition with return losses greater than 20 dB in the whole bandwidth of the waveguide allows the integration of the empty waveguide into the planar substrate, so that the waveguide can be directly accessed with a microstrip line. Therefore a microwave circuit integrated in a planar substrate, but at the same time with a very high quality factor (measured quality factor is 4.5 times higher than for the same filter in SIW) and very low losses is successfully achieved.

Index Terms—Empty substrate integrated waveguide, ESIW, substrate integrated waveguide, SIW, rectangular waveguide, substrate integrated circuit, SIC, Q-factor.

I. INTRODUCTION

THE first Substrate Integrated Waveguide (SIW) was proposed by Deslandes and Wu in 2001 [1]. It is therefore a recent technology with a great interest for many practical applications. Substrate integrated waveguides are a good compromise between the performance of classical waveguides and planar circuits in terms of quality factor and losses.

For this reason, much research has been devoted in the last years to this field, and a great variety of solutions for integrating non planar guides in printed circuit substrates have been proposed. Examples of these structures, generically known as Substrate Integrated Circuits (SIC), are the Substrate Integrated Slab Waveguide (SISW) [2], the Substrate Integrated Non-Radiating Dielectric (SINRD) guide [3], [4], which is based on the Nonradiative Dielectric Waveguide [5], or the Half Mode Substrate Integrated Waveguide (HMSIW) [6], among others. Of all of them, the SIW is the most popular,

because it is quite straightforward to apply the well known design techniques of rectangular waveguides to this topology. In recent years, many devices have been developed using SIWs: transitions to different planar lines [1], [7]–[9], filters [10]–[14], antennas [15]–[17], mixers and oscillators [18], [19], etc. The specific propagation characteristics of the SIW, initially modeled as an ideal equivalent rectangular waveguide, has been progressively better modeled thanks to increasingly accurate propagation and loss estimation models [20]–[22]. At the same time, specific analysis techniques for SIW have also been developed [23]–[28] which allow the full-wave analysis and design of SIW devices.

The SIW topology improves the performance of planar circuits in terms of losses and quality factor. And it also improves the performance of classical rectangular waveguides due to its low cost fabrication, integration in printed circuits, and higher compactness in the vertical dimension, since they are integrated in a printed circuit, and also in the longitudinal dimension, due to the fact that they are filled with a dielectric substrate. However, the compactness makes these devices more sensitive to manufacturing tolerances, which can become a serious problem at high frequencies, and the presence of the dielectric greatly increases the losses, which produces a significant reduction of the quality factor when compared to classical rectangular waveguides.

In [29] a novel transition allows the connection of a rectangular waveguide to a SIW line by means of a three step taper that, in the first place, reduces the dimensions of standard waveguide, and next matches to a SIW line with a dielectric triangular taper into the reduced empty rectangular waveguide. Finally the width of the SIW line is reduced exponentially until it reaches the desired SIW line width. This procedure allows the interconnection of a rectangular waveguide to a SIW line. But the height of the rectangular waveguide is higher than that of the SIW line, so the low profile of the SIW line is lost, and the fabrication cost is not as reduced as in the case of a standard planar circuit. Besides, the objective should be to reduce the presence of SIW lines as much as possible, so that its main disadvantage (dielectric losses) is minimized.

Consequently, it would be desirable to preserve the advantages of the rectangular waveguide in a greater measure than the SIW does, without losing the low profile and the low cost fabrication of a standard planar circuit. With the aim of advancing in this direction, in this work a simple and low cost procedure for integrating an empty waveguide into a dielectric substrate is presented. A wide band transition allows the excitation of the guide accessing with microstrip line, so that the guide can be connected to traditional planar circuit

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designs. Devices manufactured with this new technique present lower losses and greater quality factor than their equivalent designs in SIW technology (measured quality factor is 4.5 times higher than for the same filter in standard SIW), as it is shown in the results section. This novel structure has been called the Empty Substrate Integrated Waveguide (ESIW).

The ESIW is presented in section II. Section III shows the results of two filters designed and manufactured in the novel ESIW technology, and their performances are compared with the same devices manufactured in SIW. Conclusions are outlined in section IV.

II. EMPTY SUBSTRATE INTEGRATED WAVEGUIDE (ESIW)

A. Layout

In a traditional SIW, the electromagnetic waves are confined in a dielectric body enclosed by the upper and lower metallic walls of the substrate, and by lateral metalized circular holes. (see Fig. 1).

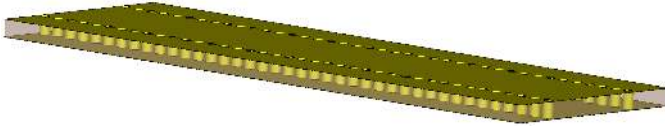


Fig. 1. Traditional SIW layout.

In the ESIW, the electromagnetic fields travel in the vacuum, and are confined by upper, lower and lateral metallic walls. This structure is manufactured by emptying a rectangular hole in a planar substrate. Next the substrate is metallized using the same procedure as for metallizing the via holes in the SIW. This way, the lateral walls of the empty waveguide are created. Finally, two thin upper and lower metallic walls are soldered to the substrate (see Fig. 2). A detailed description of the fabrication process is given in section II-C.

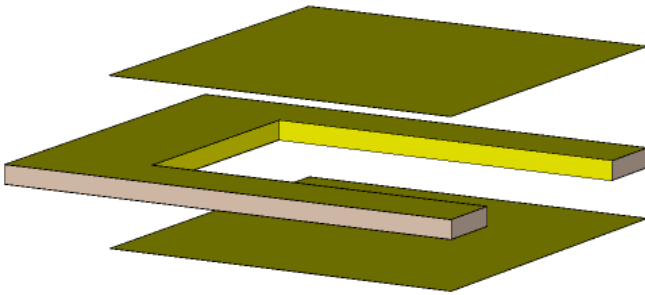


Fig. 2. ESIW layout.

B. Wideband microstrip to ESIW transition

The transition from microstrip to ESIW is shown in Fig. 3, and all the dimensions are detailed in Fig. 4. It can be considered as a two step transition. In the first step there is a transition from the microstrip line of width w_{ms} to a waveguide partially filled with a centered dielectric slab along the propagation direction of width w_{ti} . This slab is of the same

permittivity as in the microstrip substrate. An iris of width w_{ir} improves the transition from microstrip to waveguide with dielectric slab. The dimension of the iris along the propagation direction is just the width of the metallization layer. There is little reflection in this step because there is a strong similarity between the fundamental modes of the microstrip line and the empty waveguide with dielectric slab. Immediately after the step from microstrip to waveguide with dielectric slab, the width of the slab is exponentially reduced in order to match to a completely empty waveguide. Since the taper cannot be of infinite length, and in order to provide it with certain mechanical stability, it is limited to a length l_t , and the end is rounded. The final width of the exponential taper is w_{tf} .

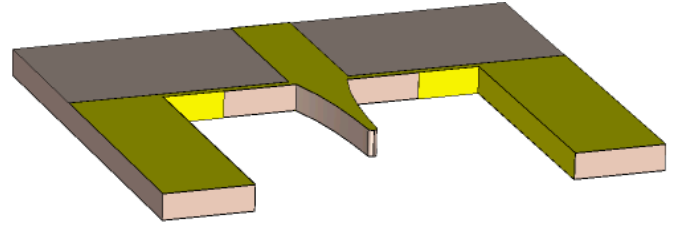


Fig. 3. Transition layout (3D view).

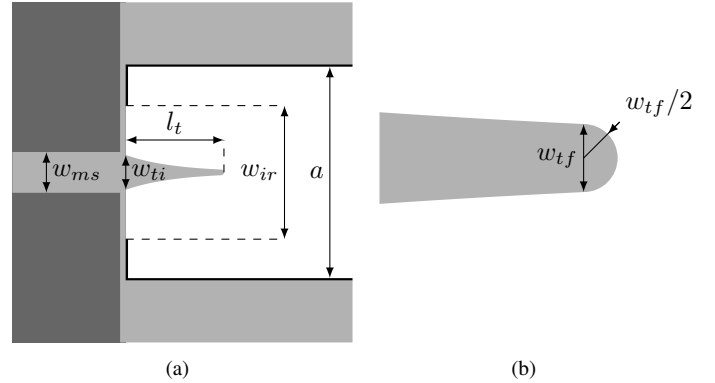


Fig. 4. (a) Taper layout (top view). Dark gray is dielectric substrate; light gray represents the copper metallization on top layer; black represents the border metallization which has been used to close the ESIW; and white is air. (b) Detail of the taper end.

The width of the taper $W(z)$ decreases with the distance z as

$$W(z) = \frac{w_{ti} (e^{-cl_t} - e^{-cz}) + w_{tf} (e^{-cz} - 1)}{e^{-cl_t} - 1} \quad (1)$$

where c is a parameter that controls the velocity with which the taper width is reduced. As it can be seen at the beginning of the taper the width is $W(z = 0) = w_{ti}$, and at the end $W(z = l_t) = w_{tf}$.

The optimum values of the four design parameters of the transition (w_{ti} , w_{ir} , l_t and c) are optimized for minimum reflection using the optimization tool of CST Studio SuiteTM. Good initial values for the optimization parameters are very important in order to speed up the convergence of the optimization procedure, and in order to ensure that a good solution with very low reflection is obtained. The initial values used for the four design parameters are shown in Table I.

TABLE I
INITIAL VALUES FOR THE DESIGN PARAMETERS OF THE MICROSTRIP TO
ESIW TRANSITION

Parameter	Initial value
l_t	$\frac{\lambda_{g0}}{4}$
w_{ti}	$0.8 \cdot w_{ms}$
w_{ir}	$\frac{a+w_{ti}}{2}$
c	$\frac{2}{l_t}$

Using the optimization tool of CST Studio Suite™, and considering the initial values of Table I, two transitions have been designed for the Rogers 4003C™ substrate ($\epsilon_r = 3.55$, $\tan \delta = 0.0027$, $h = 1.524$ mm). w_{tf} is fixed to 0.5 mm. The first transition has been designed for a waveguide of width $a = 19.05$ mm that can be used for the X and Ku frequency bands (10-15 GHz). The second transition allows the excitation of a waveguide of $a = 10.668$ mm, suitable for the K frequency band (18-27 GHz). All the physical dimensions of both transitions are shown in Table II.

TABLE II
DIMENSIONS OF THE TAPERS ($\epsilon_r = 3.55$)

	Fixed values			
	WR-75		WR-42	
a	19.0500 mm		10.6680 mm	
h	1.5240 mm		1.5240 mm	
w_{ms}	3.5964 mm		3.5964 mm	
w_{tf}	0.5000 mm		0.5000 mm	
	Optimization parameters			
	WR-75		WR-42	
	Initial	Final	Initial	Final
l_t	7.7254 mm	8.4095 mm	4.2697 mm	3.9734 mm
w_{ti}	2.8771 mm	3.0716 mm	2.8771 mm	2.4410 mm
w_{ir}	10.9635 mm	11.780 mm	6.7725 mm	6.0752 mm
c	0.258 mm^{-1}	0.236 mm^{-1}	0.4684 mm^{-1}	0.511 mm^{-1}

Figures 5 and 6 show the scattering parameters simulated with CST Studio Suite™ for both transitions.

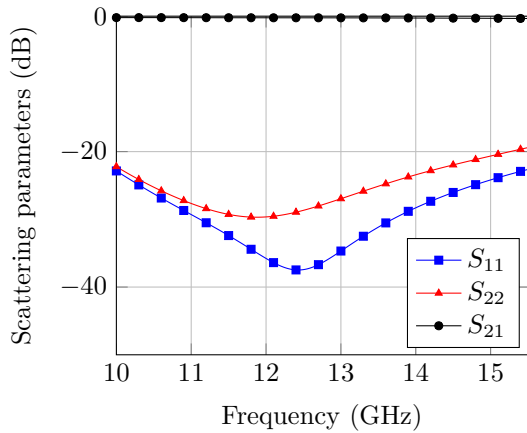


Fig. 5. Scattering parameters (CST Studio Suite™) of a transition from microstrip ($\epsilon_r = 3.55$, $h = 1.524$ mm) to an ESIW of 19.05 mm width (same width as WR-75).

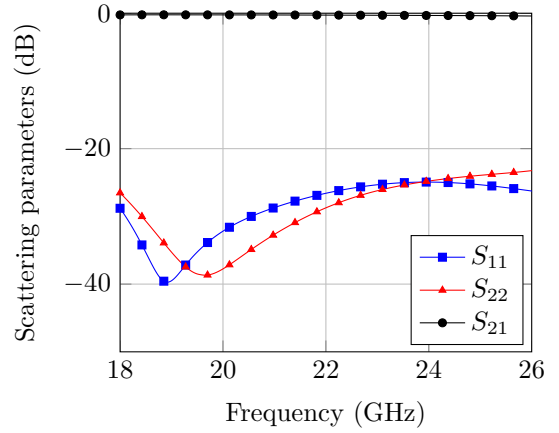


Fig. 6. Scattering parameters (CST Studio Suite™) of a transition from microstrip ($\epsilon_r = 3.55$, $h = 1.524$ mm) to an ESIW of 10.668 mm width (same width as WR-42).

Similar transitions have been designed for other substrates, even for high permittivity values, which proves the validity of the proposed transition.

C. Fabrication

In this work two ESIW filters have been manufactured. For comparison, the same filters in SIW technology have also been manufactured. The fabrication process for those types of filters (ESIW and SIW) is very similar. As a matter of fact, they have been manufactured at the same time, using the same substrate sheet (see Fig. 7).

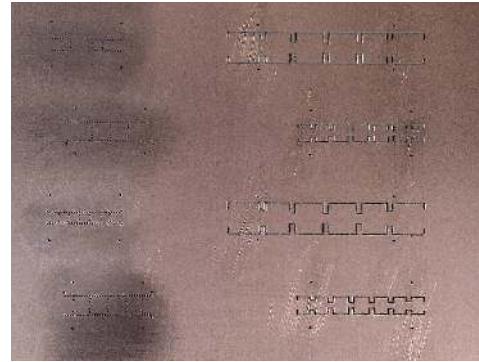


Fig. 7. Substrate sheet after cutting the ESIW filters and drilling the SIW filters.

The fabrication process for producing ESIW and SIW filters at the same time can be summed up in the following steps

- 1) In the first step the SIW holes are drilled (see filters at the left side of Figure 7) and the lateral walls of the ESIW are cut (see filters at the right side of Figure 7). For this process a LPKF Protomat S103 circuit board plotter is used, which provides with a manufacturing resolution of $0,5 \mu\text{m}$, and a repeatability of $\pm 0,001$ mm.
- 2) The substrate is metallized following a through-hole electroplating procedure. The LPKF Mini Contac RS system has been used for the electroplating. The elec-

troplating metallizes, at the same time, the SIW holes and the lateral walls of the ESIW (see Fig. 8).



Fig. 8. Border metallization synthesizing the lateral walls of an ESIW. (a) 11 GHz prototype, (b) 19.5 GHz prototype.

- 3) The exponential transitions in each ESIW are cut, and the interior of the ESIW is detached and it becomes an empty waveguide (see Fig. 8).
- 4) The upper metallic layer is milled to form the microstrip lines.
- 5) Each device is cut and separated from the substrate sheet. The SIW devices are already finished. Up to now all the fabrication processes are the standard ones for producing planar circuits (drilling, milling and metallizing).
- 6) Finally, the upper and lower walls of the ESIW are placed, aligned using some holes drilled around the waveguide, and soldered using tin solder plate which is dried in a reflow oven (see Fig. 9).

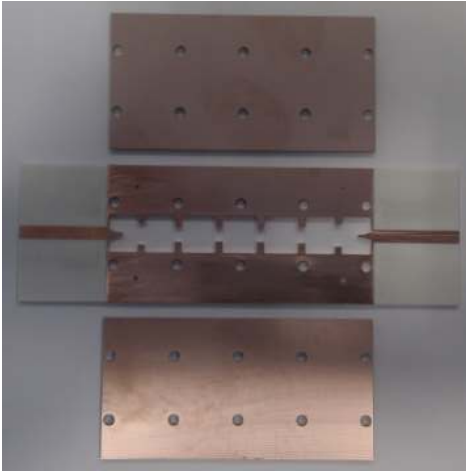


Fig. 9. ESIW 19 GHz filter before assembling.

III. RESULTS

A. Design

Two bandpass filters have been manufactured in order to test the performance of this novel waveguide.

The first filter is a four pole Chebyshev filter, with 0.01 dB ripple in the bandpass, centered at 11 GHz and with 300 MHz bandwidth. The second filter is a five pole Chebyshev filter, with 0.01 dB ripple, centered at 19.5 GHz and with 500 MHz bandwidth.

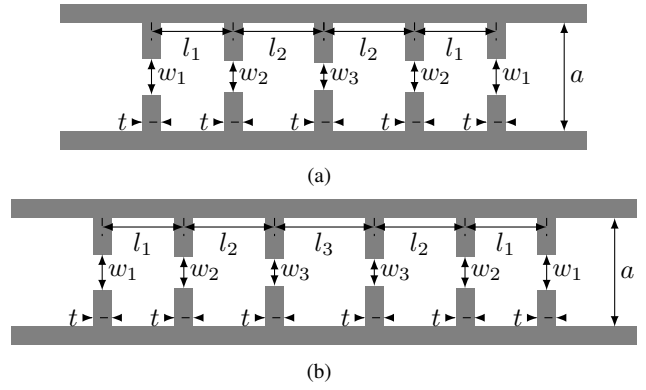


Fig. 10. (a) Layout of the ESIW fourth order filter. (b) Layout of the ESIW fifth order filter

ESIW filters are rectangular waveguides embedded in a planar circuit, and therefore the design process followed in order to design these filters is exactly the same as the classical well known method based on equivalent circuits with inversors and resonators used for designing filters in standard rectangular waveguides [30], [31]. The dimensions of the two filters, as depicted in Fig. 10, are shown in Table III.

TABLE III
DIMENSIONS OF THE ESIW FILTERS

	11 GHz		19.5 GHz	
a	19.0500	mm	10.6680	mm
l_1	17.6800	mm	10.4504	mm
l_2	19.6050	mm	11.6939	mm
l_3	—	mm	11.8419	mm
w_1	10.5200	mm	6.3930	mm
w_2	7.0980	mm	4.5373	mm
w_3	6.5200	mm	4.1630	mm
t	2.0000	mm	2.0000	mm

For comparison purposes, identical filters have also been designed in classical SIW technology. For the comparison to be a fair one, the SIW lines have been selected to have the same cutoff frequency as the ESIW. The layout of the designed prototypes can be seen in Fig. 11, and the dimensions are shown in Table IV. For designing the SIW filters, the accurate and efficient analysis method of [24] has been used.

TABLE IV
DIMENSIONS OF THE SIW FILTERS

	11 GHz		19.5 GHz	
w	10.8800	mm	6.4250	mm
l_1	9.2247	mm	5.4433	mm
l_2	10.2381	mm	6.0674	mm
l_3	—	mm	6.1413	mm
w_1	5.3260	mm	3.1276	mm
w_2	3.4686	mm	2.1072	mm
w_3	3.1368	mm	1.9005	mm
p	1.5000	mm	1.5000	mm
r_v	0.5000	mm	0.5000	mm

For the SIW filters to be connected to the accessing microstrip lines, transitions are needed. When the impedance of the microstrip line is higher than the impedance of the SIW, the conventional taper in the microstrip line [1], [8] is used.

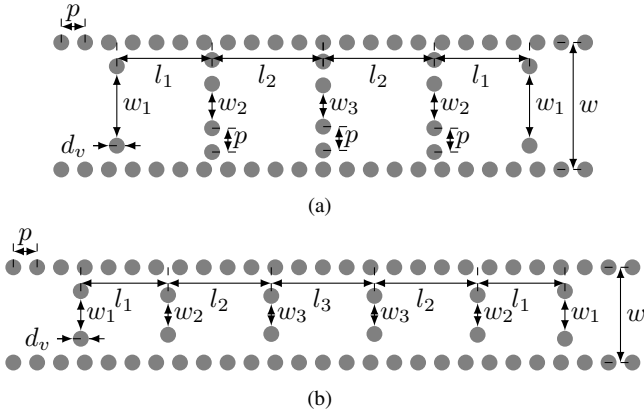


Fig. 11. (a) Layout of the 11 GHz SIW filter. (b) Layout of the 19.5 GHz SIW filter

When the impedance of the SIW line is higher, better results are obtained if the taper is implemented in the SIW line [9]. In this particular case, both lines (SIW and microstrip) present very similar impedance, and it has been possible to adequately match both lines in the whole bandwidth with a simple taper consisting in shifting the first via hole of the SIW, as shown in Fig. 12. For the X band SIW the first via position is given by $\Delta x = 0.9$ mm and $\Delta y = 1.81$ mm, and for the K band SIW $\Delta x = 1.8$ mm and $\Delta y = 0.48$ mm.

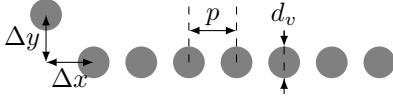


Fig. 12. Layout of the transition used for both SIW designs.

B. Measurements

The SIW and ESIW filters have been simulated, and they have also been measured. In Fig. 13, the manufactured prototypes are shown. For the upper and lower walls of the ESIW filter, sheets of FR4 have been soldered to the empty waveguide cut in the main substrate (see Fig. 9). FR4 sheets have been used because it is a low cost solution for this work, with the aim of proving the viability of this new line. Much lower profile prototypes could be obtained using thin copper plates (0.3-0.4 mm) or thinner substrate sheets.

The simulation results and the measurements for both filters are shown, respectively, in Figures 14 and 15.

If the SIW and ESIW filters are analyzed without considering losses, their responses are almost identical. However, when the losses are considered, there is a significant difference, as shown in Figures 14 and 15. The transitions to microstrip and the feeding 10 mm lines are also included in the simulations.

Measurements are in good agreement with the simulation results. The losses are significantly lower for the ESIW filters, 0.9 dB for the 11 GHz filter, and 1.3 dB for the 19.5 GHz filter. These values include the losses of the microstrip accessing lines and the transitions from microstrip to ESIW. If these losses are subtracted (they have been obtained simulating

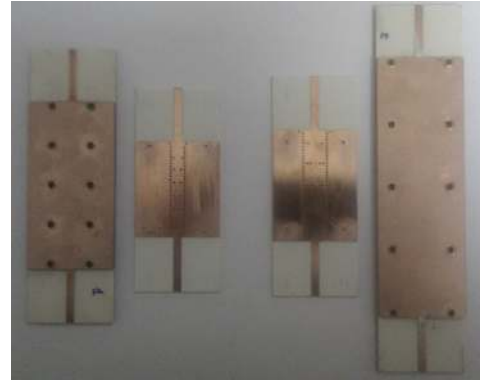


Fig. 13. Fabricated ESIW and SIW prototypes. 11 GHz prototypes on the right, 19.5 GHz prototypes on the left.

back-to-back transitions with CST), the losses of the filters are 0.5 dB for 11 GHz, and 0.8 dB for 19.5 GHz.

C. Quality factor

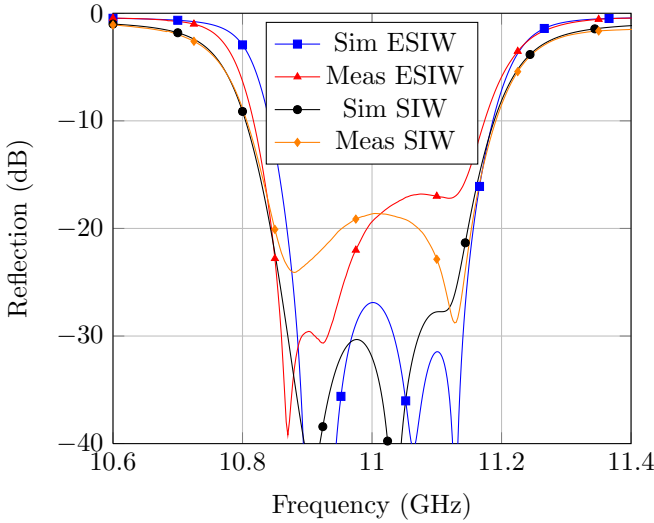
The comparison between ESIW and SIW responses when losses are considered shows a great difference in the insertion losses for both types of filters, and therefore also in the corresponding quality factors. The unloaded quality factor has been calculated for both filters and the results are shown in tables V and VI. The results in Table V have been calculated simulating with a commercial software (CST Studio) a single cavity weakly coupled through very small accessing irises. Then the quality factor is computed as the inverse of the fractional bandwidth. This has been repeated for all the cavities in the filter, and the worst result (smaller quality factor), is shown in the table. The results of table VI have been calculated using the analytical expressions for the quality factor of a lossy rectangular cavity excited with the fundamental mode [32]. The quality factor has been calculated using this expressions for all the filter cavities, and the worst result (lower quality factor) is shown in the table. There is a good agreement between the simulated and the analytical values.

The quality factor is compared for the the same filter in SIW, in ESIW and in the standard rectangular waveguide with the same width a than the ESIW, but with the height $b = a/2$.

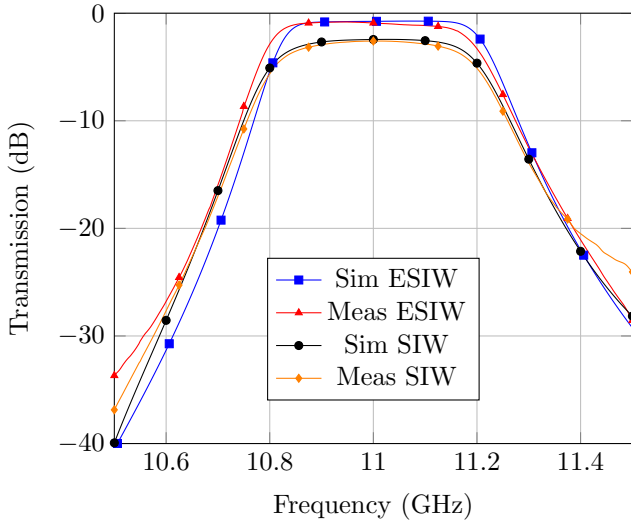
TABLE V
QUALITY FACTORS (SIMULATED WITH CST)

	Q_{SIW}	Q_{ESIW}	Q_{WR}
11.0 GHz	314	2219	8701
19.5 GHz	321	2750	5531
	Q_{WR}/Q_{SIW}	Q_{ESIW}/Q_{SIW}	Q_{WR}/Q_{ESIW}
11.0 GHz	27.71	7.06	3.92
19.5 GHz	17.23	8.57	2.01

It can be observed that for 11 GHz the quality factor of the ESIW is theoretically around 7 times higher than for the same filter in SIW. However, the quality factor is still higher in the standard rectangular waveguide (almost 4 times higher than in the ESIW, and around 26 times higher than in the SIW). This is because the height of the ESIW is the same as the height of the substrate ($h = 1.524$ mm), while in the standard



(a)



(b)

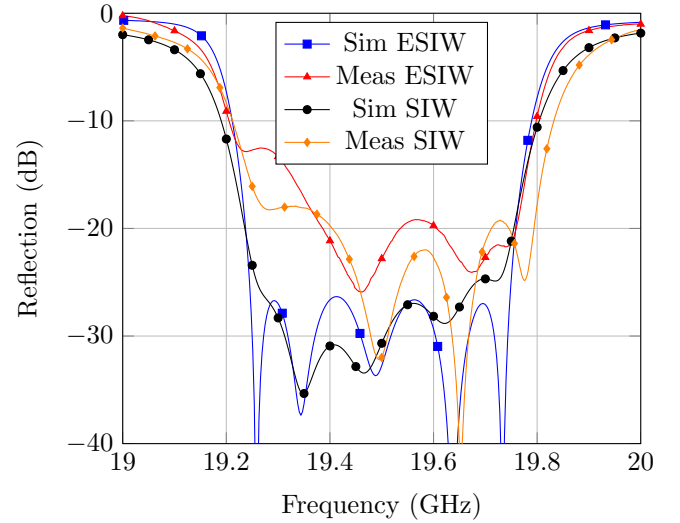
Fig. 14. Comparison of simulated results considering transitions and feeding lines with measured responses for the filter at 11 GHz. (a) Reflection, (b) Transmission

TABLE VI
QUALITY FACTORS (ANALYTICAL)

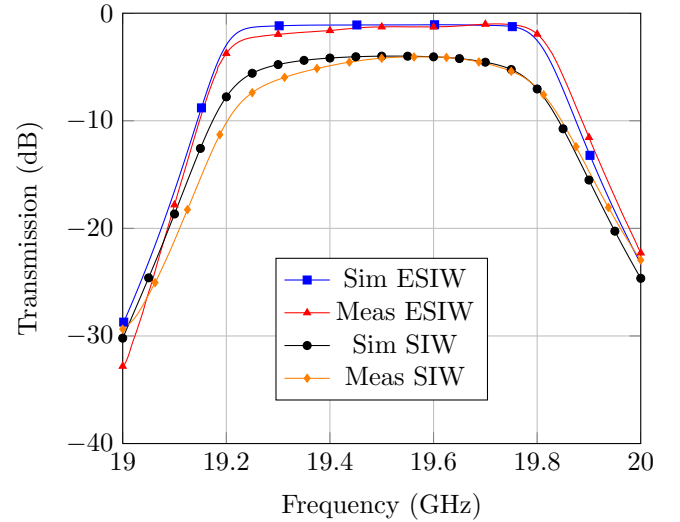
	Q_{SIW}	Q_{ESIW}	Q_{WR}
11.0 GHz	301	2183	7798
19.5 GHz	307	2577	5146
	Q_{WR}/Q_{SIW}	Q_{ESIW}/Q_{SIW}	Q_{WR}/Q_{ESIW}
11.0 GHz	25.9	7.25	3.57
19.5 GHz	16.76	8.39	1.99

rectangular waveguide the height is greater ($b = 9.525$ mm), so there is more volume, and more energy can be stored than in the ESIW.

For 19.5 GHz, the quality factor of the ESIW is around 8.5 times higher than in the SIW, and in the standard rectangular waveguide the quality factor is only 2 times higher than in the ESIW, and around 17 times higher than in the SIW. The difference in the quality factor between ESIW and standard rectangular waveguide is not so high at this frequency because



(a)



(b)

Fig. 15. Comparison of simulated results considering transitions and feeding lines with measured responses for the filter at 19.5 GHz. (a) Reflection, (b) Transmission

there is not so much difference as in 11 GHz between the substrate height ($h = 1.524$ mm) and the height of the standard rectangular waveguide ($b = 5.334$ mm). It can also be observed that when the frequency increases the difference in quality factor between the ESIW and the SIW increases.

TABLE VII
QUALITY FACTORS (MEASURED)

	Q_{SIW}	Q_{ESIW}	Q_{WR}
11.0 GHz	273	1226	-
19.5 GHz	266	1196	-
	Q_{WR}/Q_{SIW}	Q_{ESIW}/Q_{SIW}	Q_{WR}/Q_{ESIW}
11.0 GHz	-	4.49	-
19.5 GHz	-	4.49	-

These measured values of the losses have been used to compute the measured quality factor. It is shown in Table VII. As already predicted by the simulation, the quality factor is

higher for the ESIW filters, although the difference is not so high. This is probably due to the fact that the manufacturing process is not a professional one. The upper and lower walls on the ESIW have been soldered, and the current continuity is not as good as if all the guide walls were of the same conductor. Still, the measured quality factor of the ESIW, is 4.5 times greater than for the SIW for both filters, at 11 GHz and 19.5 GHz. In consequence, the selectivity in the ESIW filters is greater, and the bandpass response is flatter. This could even be improved with a more professional manufacturing technique.

IV. CONCLUSIONS

A novel integrated line, the Empty Substrate Integrated Waveguide (ESIW), is presented in this work. It consists on an empty rectangular waveguide integrated in a planar circuit, thanks to an innovative taper that connects the accessing microstrip line to the empty waveguide. This taper has been successfully implemented for several substrate thickness, thus validating its usefulness for all type of substrates.

The fabrication technique just requires standard manufacturing processes for printed circuits (drilling, milling and cutting), plus the soldering of upper and lower walls. If a thin copper sheet is used for the upper and lower walls, the profile of the ESIW is almost identical to that of the equivalent SIW. This means that the new integrated waveguide can be manufactured at low cost in any laboratory with standard facilities for producing printed circuits.

In order to test the performance of the ESIW, two sets of identical filters have been manufactured in SIW and ESIW technologies. The measurements of the prototype responses prove that the ESIW technology provides lower losses and better quality factor (measured quality factor 4.5 times higher for the filters at 11 GHz and 19.5 GHz). This quality factor is not still as good as for the standard rectangular waveguide, but it is much better than for the SIW, still maintaining the advantages of being integrated in a planar circuits and the low cost fabrication. The difference in quality factor between ESIW and standard rectangular waveguide decreases as the difference in height between the substrate where the ESIW is fabricated and the height of the standard rectangular waveguide decreases.

The ESIW devices are not so compact as the equivalent SIW devices, due to the absence of dielectric. However, for high frequency devices, fabrication tolerances have a greater impact in SIW filters, due to the smaller dimensions and due to the tolerance of the substrate permittivity. Besides, at high frequency, the outperformance of the ESIW in terms of losses and quality factor increases. Therefore, it can be concluded that the ESIW is a very promising alternative to SIW, especially as the frequency increases.

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