Novel Extensible Multilevel Inverter Based on Switched-Capacitor Structure

Yaoqiang Wang[1,2] · Juncheng Ye[1,2] · Ruohan Ku[1,3] · Yi Wang[1,2*] · Jun Liang[1,4]

Abstract

Multilevel inverters (MLIs) play an important role in research on renewable energy conversion. However, in traditional designs, the high voltage stress of switching devices and the large number of switches limit the wide application of the inverter. In order to ameliorate these problems, this paper proposes a switched-capacitor multilevel inverter (SCMLI). When compared with traditional MLIs, the proposed SCMLI utilizes a switched-capacitor structure, where the capacitors can achieve voltage self-balancing without auxiliary methods. Thus, it permits changes of the positive and negative polarity of the output level without the need for an H-bridge. In addition, with the augment of the level in the expanded SCMLI structure, the maximum blocking voltage can be kept constant. To show the advantages of the proposed structure, an extensible single dc source five-level SCMLI prototype has been built. Through a comparative analysis with different topologies, this paper also presents the advantages of the proposed topology in terms of the output voltage gain, number of output levels, and voltage stress. Finally, the correctness and feasibility of the proposed inverter are validated by extensive experiments.

Keywords: Multilevel inverter, Switched-capacitor, Self-balancing, Voltage gain, Low voltage stress

1 Introduction

In recent years, multilevel inverters (MLIs) have become attractive converters in numerous applications such as renewable energy systems, motor drives, distributed generation systems, UPS systems, and flexible alternating current transmission system (FACTS) [1-3]. When compared with the traditional two-level inverters, MLIs have many advantages such as lower total harmonic distortion, reduced dv/dt stresses, lower switching frequency, etc. [4]. In general, classic MLIs include neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) inverters. However, NPC and FC inverters employ a large number of clamping diodes and capacitors along with the increase of output levels, which inevitably raises the cost of topologies and the complexity of control strategies [5, 6]. Cascaded H-bridge MLIs have problems in terms of the lack of boost capacity and the need for multiple isolated dc sources [7, 8].

To alleviate the problems of traditional MLIs, switched-capacitor multilevel inverters (SCMLIs) have been proposed in [9-14]. SCMLIs can achieve multilevel output with a single dc source and fewer power devices. The five-level inverter proposed in [9] uses only eight switches, but the topology contains two extra diodes and the working states for most of the switch pairs are inconsistent. In [10], a seven-level inverter with a single dc voltage source and twelve switches was proposed. Although the topology in [11] employs ten switches to output seven levels, there are still four extra diodes and ten gate drivers are required. The same issue can be found in [13], where the nine-level inverter can achieve twice voltage gain by using many diodes and drivers. In addition, two capacitors are discharged for most of a cycle, which may bring about a large voltage ripple and the imbalance of capacitor voltage.

Meanwhile, the extensible capability is important for SCMLIs to improve their output voltage. In many low-input dc voltage applications such as photovoltaic power generation and other renewable energy power generation systems, the output voltage needs to be promoted. Although the output voltage can be increased by adding a transformer to the AC side of the inverter [15, 16], this seriously increases the volume and weight of the inverter. Therefore, DC-AC SCMLIs with extensible capability to increase output voltage are also a focus of research.

In addition, the SCMLIs developed in [17-20] can realize the expansion of the topology, and increase both the output voltage gain and the number of output levels. The inverter in [21] can achieve the purpose of raising the voltage gain through the sequential charging of the dc

* Corresponding author: Yi Wang
Email: wangyi1414599008@163.com

1 School of Electrical Engineering, Zhengzhou University, Zhengzhou, China
2 Henan Engineering Research Center of Power Electronics and Energy Systems, Zhengzhou, China
3 Xuchang Power Supply Company, State Grid Henan Electric Power Co., Ltd., Xuchang, China
4 School of Engineering, Cardiff University, Cardiff, WLS, UK

source and the capacitors. By utilizing two capacitors, the four times voltage gain and the more output levels can be achieved. However, the losses of the capacitor are high.

The above-mentioned extensible topologies require the addition of H-bridge to achieve the changes of the positive and negative polarities of the output level. However, for the inverter with associated with H-bridge, the voltage stress on the switches grows with the increase of output voltage gain. Therefore, high performance (expensive) switching devices are required, which increases the cost of extended structures. Voltage stress is a bottleneck limiting the application range. To address this problem, SCMLIs without H-bridge were proposed in [22-25]. In [23], the proposed multilevel inverter achieved a high voltage gain. However, the voltage stress of the switching devices in the expanded topology cannot be kept constant. However, the SCMLI without H-bridge in [25] can keep the voltage stress of the switching devices constant. However, it cannot be ignored that the inverter has a problem in terms of its high total standing voltage (TSV).

Based on the above analysis, this paper presents a novel expansible switched-capacitor multilevel inverter, which can output five levels and achieve twice voltage gain with a single dc source. When compared with existing topologies, the proposed SCMLI has the following salient features.

- The proposed topology removes backend H-bridge due to the inherent polarity reversal capability, and the polarity of the output level can be changed with proper control of switches.
- Only two switches have voltage stress of $2V_{dc}$, which significantly reduce the total voltage stress and maximum blocking voltage of switches.
- Although the inverter uses ten switches, only five gate drivers are required. This is due to the fact that many pairs of switches have the same working state. Thus, the cost and complexity of control are both reduced.
- The voltage of two capacitors can be self-balanced without any auxiliary circuits.
- The inverter has the ability of expansion. With the increase of output levels, the maximum blocking voltage for all of the switches is kept within $2V_{dc}$.

The remainder of this paper is organized as follows. Section 2 introduces the structure and operation principle of the proposed SCMLI. Section 3 gives the modulation method of the topology, analyzes self-balance of the capacitor voltage, and presents the capacitor selection method. Section 4 verifies the characteristics of the proposed inverter by comparing the proposed inverter with the existing topologies in terms of the power losses and the number of used circuit elements. Section 5 presents the simulation and experimental results of the proposed inverter. Finally, Section 6 gives some concluding remarks.

2 Proposed Topology

2.1 Topology of Proposed Inverter

The topology of the proposed MLIs is shown in Fig. 1, which consists of a dc source and a switched-capacitor structure. The switched-capacitor structure is composed of the capacitors C_1 and C_2, and the switching devices S_1-S_{10}. Among them, S_4 and S_8 are IGBTs without anti-parallel diodes, and the other switching devices are IGBTs with anti-parallel diodes. By controlling the on and off of the switching device to control the charging and discharging state of the capacitor, the inverter can output five levels: $2V_{dc}$, V_{dc}, 0, $-V_{dc}$, and $-2V_{dc}$.

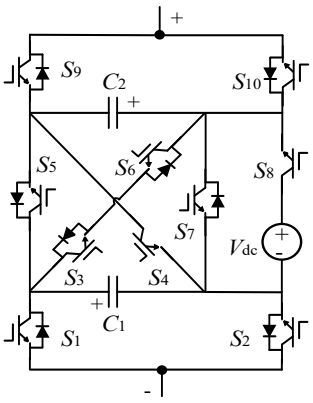


Fig. 1 Topology of the five-level inverter.

2.2 Operating Principle of the Five-Level Inverter

To obtain a five-level voltage output, the different switch combinations of the proposed MLIs are listed in Table 1, where “C”, “D”, and “–” indicate the charging, discharging, and idle status in the capacitance, respectively. In Table 1, the five working stages are divided into one control period, and the corresponding working mode in each stage is shown in Fig. 2.

Table 1 Operation States of Inverter Components

Levels	On-state Switches	Capacitors C_1, C_2
2	S_2, S_5, S_{10}	D, D
1	S_2, S_3, S_4, S_6, S_8, S_{10}	C, C
0	S_1, S_5, S_9,	–, –
-1	S_1, S_3, S_4, S_6, S_8, S_9	C, C
-2	S_1, S_7, S_9,	D, D

For ease of analysis, the following assumption are made:

- All of the power devices are ideal, without on-resistance and forward voltage drop.
- The voltage between capacitances remains at the rated voltage, and there is no obvious voltage fluctuation.

With the above assumptions, the working principle of the MLIs is summarized in Fig. 2.

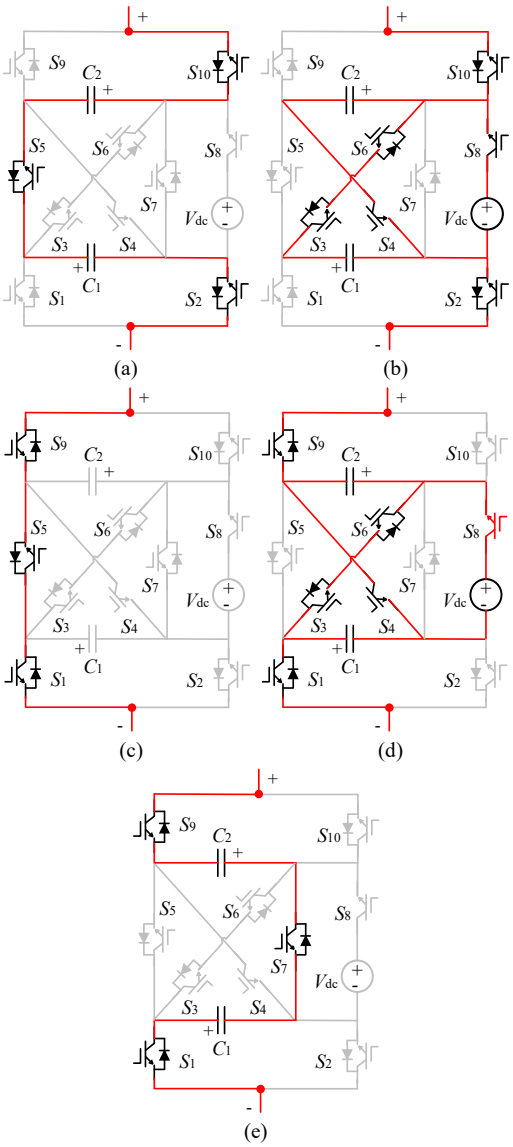


Fig. 2 Working modes of the proposed inverter: (a) +2 level; (b) +1 level; (c) 0 level; (d) -1 level; (e) -2 level.

+2 Level: As shown in Fig. 2(a), the switches S_2, S_5, and S_{10} in the inverter are in the on-state, and the remaining switching devices are in the off-state. The capacitors C_1 and C_2 are discharged in series. Thus, the inverter output voltage is $2V_{dc}$. In this situation, the inverter is in the $+2V_{dc}$ working mode.

+1 Level: As depicted in Fig. 2(b), the switches S_2, S_3, S_4, S_6, S_8, and S_{10} in the inverter are in the on-state, and the remaining switches are in the off-state. At this time, the dc source charges the capacitors C_1 and C_2, and the inverter output voltage is V_{dc}. Thus, the inverter is working in the $+V_{dc}$ mode.

0 Level: As can be seen in Fig. 2(c), the switches S_1, S_5, and S_9 in the inverter are in the on-state, and the remaining switches are in the off-state. The capacitors C_1 and C_2 are in the hold state. Thus, the inverter output voltage is 0, which is working in the zero output level mode.

-1 Level: In Fig. 2(d), the switches S_1, S_3, S_4, S_6, S_8, and S_9 in the inverter are in the on-state, and the remaining switches are in the off-state. The dc source charges the capacitors C_1 and C_2, and the inverter output voltage is $-V_{dc}$.

-2 Level: As shown in Fig. 2(e), the switches S_1, S_7, and S_9 in the inverter are in the on-state, and the remaining switches are in the off-state. The capacitors C_1 and C_2 are discharged in series. Thus, the inverter output voltage is $-2V_{dc}$.

It is worth pointing out that the proposed inverter can provide a closed current loop in any of the above operating modes. Therefore, the proposed inverter can be connected to inductive loads.

2.3 Expansion of the Proposed Inverter

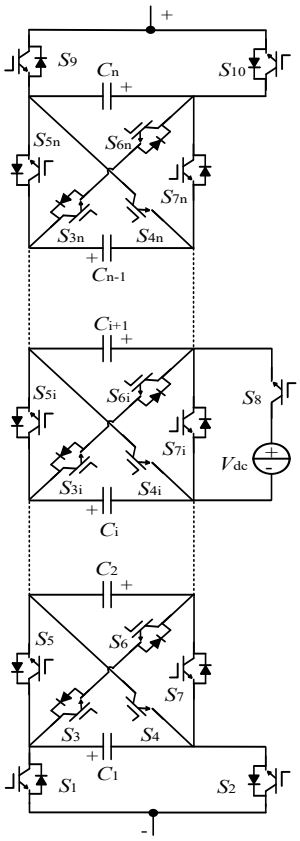


Fig. 3 Proposed space-type switched-capacitor inverter.

From the above detailed analysis, the proposed five-level inverter topology is able to output five voltage levels with twice voltage gain. In addition, to further increase the both the number of output levels and the output voltage gain, as well as to broaden the scope of practical application, the proposed inverter is expanded in Fig. 3. The expanded topology only increases the switched-capacitor structure, which consists of a capacitor and five switches. The addition of every two switched-capacitor structures increases four output levels and enhances the voltage gain

by twice. When the output voltage is nV_{dc}, the number of output levels is 2n + 1. More importantly, the maximum voltage stress sustained by the switches does not increase with the expansion of the structure, which is still 2V_{dc}.

3 Modulation and Capacitance Design

3.1 Modulation Strategy

For the modulation of multilevel inverters, many pulse width modulation (PWM) strategies have been used, such as space vector pulse width modulation (SV-PWM), selective harmonic elimination pulse width modulation (SHE-PWM), sinusoidal pulse width modulation (SPWM), etc. [26]. The SV-PWM scheme is suitable for a small number of output levels, since the complexity of the modulation will increase with growth in the number of output levels. The SHE-PWM strategy can abate the switching frequency and improve the utilization of dc voltage. However, its implementation is not trivial. The most commonly used modulation technique is SPWM. This is because that it is easy to implement and the quality of output waveform is superb. The phase disposition pulse width modulation (PD-PWM) method, which is a kind of SPWM, is utilized to modulate the proposed inverter, and the schematic of the modulation is shown in Fig. 4.

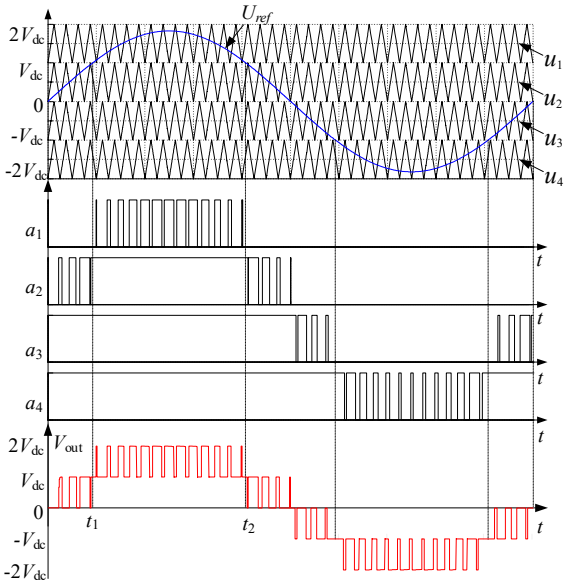


Fig. 4 Modulation schematic.

As shown in Fig. 4, the four triangular carriers u_1~u_4 are compared with a sinusoidal reference wave to give rise to the basic pulse signals a_1~a_4, and these carriers have the same amplitude (A_c) and frequency (f_c). The amplitude and frequency of the sinusoidal reference wave are A_{ref} and f_{ref}, respectively. The modulation index M is set to 0.9. It can be seen that the proposed inverter outputs five levels. The logical combination of switches can be seen in Fig. 5. It is worth noting that there are two complementary switch pairs (S_1 & S_{10} and S_2 & S_9), and that the switches S_3, S_4, S_6, and S_8 have the same operation states in one cycle. Thus, only five gate divers are required.

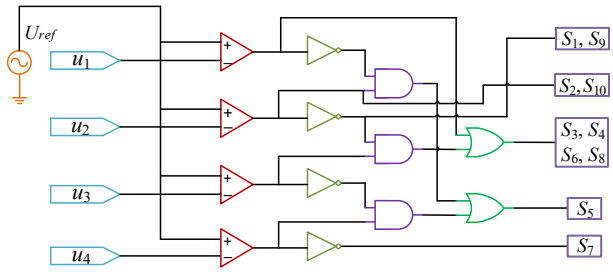


Fig. 5 Logic modulation of the proposed inverter.

3.2 Capacitance Voltage Self-Balancing Analysis

The operation status of the capacitors C_1 and C_2 is summarized in Table 2. From Table 2, it can be noted that the dc source charges or discharges the capacitors C_1 and C_2 at the levels of ± 1. Thus, by setting the charging and discharging states of the capacitors, C_1 and C_2 are in the same modulation wave period.

According to the modulation of the proposed inverter in Fig. 4, it can be known that dc source only charges the capacitors C_1 and C_2 at the level of V_{dc}. Table 2 shows the charging and discharging working states of the two capacitors. It can be seen that the charging and discharging states of the capacitors C_1 and C_2 are the same in one modulation wave period. Thus, the capacitor voltage can be balanced.

Table 2 Operation Status of Two Capacitors

State	C_1	C_2	Mode
Charging	±1 level	±1 level	Fig.2b and Fig.2d
Discharging	±2 level	±2 level	Fig.2a and Fig.2e
Idle	0 level	0 level	Fig.2c

3.3 Capacitance Calculation

The capacitance is the key factor to determine the levels and the gain of the output voltage. In addition, the effect of the capacitor voltage ripple on the output voltage can be reduced effectively when the proper value for the capacitance is selected. Therefore, this part is devoted to analyzing the calculation of the capacitance.

The t_1 and t_2 in Fig. 4 can be calculated by:

$$t_1 = \frac{\sin^{-1}(1/2)}{2\pi f_{ref}} \tag{1}$$

$$t_2 = \frac{\pi - \sin^{-1}(1/2)}{2\pi f_{ref}} \tag{2}$$

where f_{ref} is the frequency of the reference waveform.

The capacitor voltage ripple is related to the maximum

continuous discharge of the capacitor. According to the analysis of the working principle in Section 2 and the working modes of each level in Fig. 2, it can be known that the longest discharge time of the capacitors C_1 and C_2 is [t_1, t_2]. Therefore, the maximum discharge of the capacitor can be calculated as:

$$Q_{C_i} = \int_{t_1}^{t_2} I \sin(2\pi f_{ref} t)\,\mathrm{d}t \tag{3}$$

In addition, the capacitor voltage ripple is set to k times the rated voltage of the capacitor, and k generally does not exceed 0.1. Thus, the value of the capacitor C_1 should satisfy the following constraint:

$$C_i \geq \frac{Q_{C_i}}{kV_{C_i}} = \frac{Q_{C_i}}{\Delta V_{rip}} \tag{4}$$

where V_{ci} indicates the rated voltage of the capacitor, and ΔV_{rip} represents the capacitor voltage ripple. Therefore, a proper capacitor needs to be selected to achieve the normal operation of the inverter.

4 Comparison Analysis and Losses Calculation

4.1 Comparison Analysis

In this section, to verify the effectiveness and superior performance of the proposed SCMLI, the non-extensible SCMLI in [10, 13], the extensible SCMLI in [17-19], the SCMLIs without H-bridge in [22, 23] are also tested to make comparisons. The results of this comparison are summarized in Fig. 6 and Table 3, which includes the output voltage gain, number of levels, number of capacitors, diodes, and switches, etc.

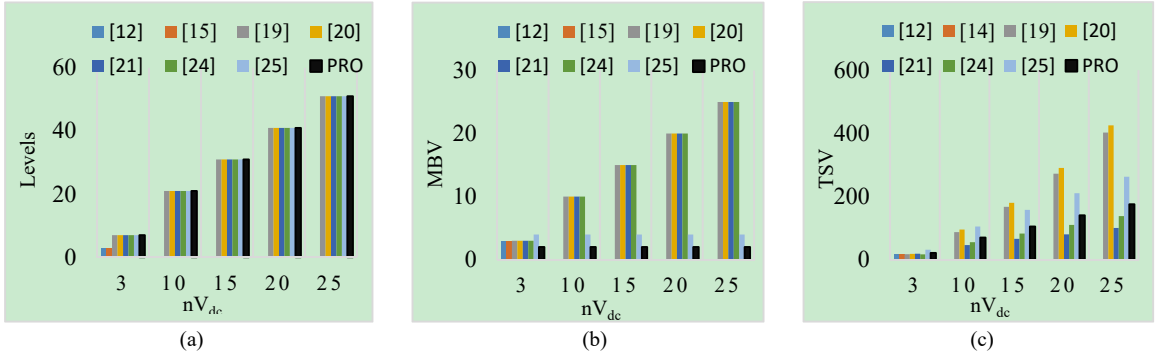
When the output voltages of these topologies are nV_{dc} (the non-expandable inverters are calculated based on the maximum output voltage), comparison results of various parameters are shown in Table 3. This part makes a detailed analysis from the aspects of levels, maximum blocking voltage (MBV), and total standing voltage (TSV) to illustrate the advantages of the proposed inverter. MBV is the maximum voltage stress of the switching device.

Fig. 6(a) presents a comparison of the output level number of the proposed inverter topology and several existing topologies with changes in the voltage gain. It can be seen from the figure that the proposed inverter and the expandable SCMLI have basically the same level number changes, while the non-extensible SCMLIs stop changing only to the number of their highest output level. With the increase of the number of output levels, the quality of the output voltage is greatly improved, and its output voltage waveform gets closer to a sine wave.

Fig. 6(b) presents a comparison of the MBVs. The MBV in [12] and [15] is 3V_{dc}, while the output voltage gain does not increase. The MBVs in [19-21] and [24] increase with the number of capacitors. The topology in [25] keeps 4V_{dc} constant. Thus, not all of the non-H-bridges SCMLIs can keep the MBV unchanged. However, the MBV in the proposed inverter is only 2V_{dc}. When compared with the above inverters, the proposed inverter reduces the inverter requirements in terms of the performance of switching devices.

In Table 3, the available switches indicate whether the switch has to make the inverter work normally when the topology of the inverter expands. It can be seen that with the increase of output level, the MBV of the proposed inverter remains at a low value of 2V_{dc}. When it is expanded to a certain degree, there are no switches meeting the operating conditions of the inverter. However, the MBV in the proposed topology remains unchanged in an expanded structure. Thus, no matter how the topology of the proposed inverter expands, the switch devices are able to satisfy the conditions.

Fig. 6(c) presents a comparison of the TSV. The non-extensible topology stops changing after its maximum output voltage, and the extensible topology changes with the increase of the output voltage. When compared with most of the existing inverter topologies, the TSV of the proposed inverter is greatly reduced. Thus, during the operation of the inverter, the switching losses can be effectively reduced, and the service life of the switching devices can be increased.



(a) (b) (c)

Fig. 6 Comparison of various SCMLIs: (a) levels; (b) MBV; (c) TSV.

Table 3 Parameter Comparison of Various Inverters

Comparing Items	[12]	[15]	[19]	[20]	[21]	[24]	[25]	Proposed
Gain	$3V_{dc}$	$3V_{dc}$	nV_{dc}	nV_{dc}	nV_{dc}	nV_{dc}	nV_{dc}	nV_{dc}
Levels	7	7	2n+1	2n+1	2n+1	2n+1	2n+1	2n+1
Capacitors	2	3	n-1	n-1	Log_2n-1	$2Log_2n$-2	n/2	n
Switches	8	10	2n+2	n+4	$3Log_2n$-3	$6Log_2n$-2	2n+2	5n
Extra diodes	2	0	n-1	2n-2	0	2	n/2	0
MBV	$3V_{dc}$	$3V_{dc}$	nV_{dc}	nV_{dc}	nV_{dc}	nV_{dc}	$4V_{dc}$	$2V_{dc}$
TSV	$18V_{dc}$	$18V_{dc}$	$(n^2+7n+4)\ V_{dc}/2$	$(n^2+9n)V_{dc}/2$	$(4n+6-2/n)V_{dc}$	11n/2-3	$21nV_{dc}/2$	$(7n-2)V_{dc}$
Available Switches	Yes	Yes	No	No	No	No	No	Yes

From the above comparative study, the salient features of the proposed SCMLI are summarized as follows.

(1) The H-bridge is not utilized in the proposed SCMLI.

(2) The MBV of switches remains unchanged with the increases of output levels in the expanded structure.

(3) The number of the utilized capacitance, switch and diode are all reduced.

(4) The TSV of the proposed inverter is greatly reduced.

4.2 Calculation of Losses

The proposed inverter losses are mainly composed of three aspects: the ripple losses in the capacitance, the conduction losses, and the switching losses in the power switch. This part analyzes and calculates these three losses.

A. Ripple Losses

When the capacitor is charging, there is a voltage ripple. The related energy loss in this voltage ripple can be calculated by:

$$E_{rip}=\frac{1}{2}C_i\Delta V_{rip} \tag{5}$$

where E_{rip} is the energy losses during the capacitor charging process.

By combining (4) and (5), the value of E_{rip} can be obtained by:

$$E_{rip}=\frac{Q_{C_i}^2}{2C_i} \tag{6}$$

After acquiring E_{rip}, the ripple losses of the proposed inverter can be denoted as:

$$\begin{aligned} P_{rip}&=f_o\sum_1^2 2E_{rip} \\ &=2f_o\left(\frac{Q_{C_1}^2}{2C_1}+\frac{Q_{C_2}^2}{2C_2}\right) \end{aligned} \tag{7}$$

where f_o indicate the output voltage frequency.

B. Conduction Losses

The conduction losses are related to the total parasitics of the conductive elements contained in the load current path. Due to the symmetry of the operating principle, the conduction losses of the topology can be analyzed in ½ of a cycle. The parasitic parameters in the load current path includes the on-resistance r_s of the switches, and the internal resistance r_c of the capacitors. The equivalent circuit of the output load current path at +2 level and +1 level is shown in Fig. 7. It can be seen from Fig. 7(a) that the total equivalent parasitic resistance at the +2 level can be expressed as:

$$r_{eq(2)}=2r_C+3r_S \tag{8}$$

The duration of the +2 level is $(t_2\text{-}t_1)$. Thus, the conduction losses of the +2 level at ½ of a cycle can be calculated as:

$$E_{con(2)}=I_{R(2)}^2\cdot r_{eq(2)}\cdot(t_2-t_1) \tag{9}$$

where $I_{R(2)}$ is the output current, which can be calculated by:

$$I_{R(2)}=\frac{2V_{dc}}{R_{Load}} \tag{10}$$

where R_{Load} denotes the load resistance.

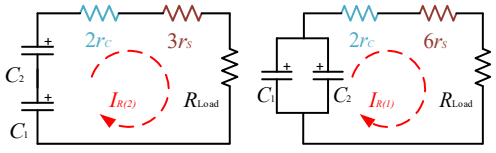
Therefore, the conduction losses of the +1 level can be obtained by:

$$\begin{aligned} E_{con(1)}&=I_{R(1)}^2\cdot r_{eq(1)}\cdot\left(\frac{T}{2}\text{-}t_2+t_1\right) \\ &=\left(\frac{V_{dc}}{R_{Load}}\right)^2\cdot 6r_S\cdot\left(\frac{T}{2}\text{-}t_2+t_1\right) \end{aligned} \tag{11}$$

where T is the working time of the inverter for one cycle.

Thus, the total conduction losses of the proposed inverter can be calculated by:

$$P_{con}=E_{con(1)}+E_{con(2)} \tag{12}$$



(a) (b)

Fig. 7 Equivalent circuit of the load current path considering the parasitic parameters: (a) at +2 level; (b) at +1 level.

C. Switching Losses

The switching losses are usually caused by the inherent switching delay of the semiconductor device, which can

be approximated by the parasitic shunt capacitor C_s of the switch. The energy losses of the switch S_j are:

$$E_{S_j} = \frac{1}{2} C_S V_{b(j)}^2 \tag{13}$$

where j = 1,2,3…10, $V_{b(j)}$ is the blocking voltage generated by the switch at the moment of on and off.

From the working principle and Table 1, the on-off conditions of the proposed inverter can be acquired. Thus, the total switching losses can be calculated by:

$$P_S = f_o \sum_{j}^{10} N_{S(j)} E_{S_j} \tag{14}$$

where $N_{S(j)}$ is the total number of times that the switch S_j is turned on and off in one cycle.

In summary, the efficiency of the five-level inverter can be calculated as:

$$\eta = \frac{P_o}{P_o + P_{rip} + P_{con} + P_S} \tag{15}$$

where η and P_o are the efficiency and output power of the proposed topology, respectively.

From the above analysis, the losses of the inverter can be obtained. It is worth noting that r_s, r_c, C_s, $C_{1,2}$, and f_o are set to 0.15 Ω, 0.06 Ω, 500 pF, 2200 μF, and 50 Hz, respectively. When the dc source is set to 30V and the load is 50 Ω-15 mH, the three kinds of loss can be calculated as: P_{rip} = 0.48 W, P_{con} = 0.53 W, and P_S = 0.18 W. A power losses distribution is shown in Fig. 8, and Fig. 9 shows the theoretical efficiency and experimental efficiency of the proposed inverter under different output powers. It can be seen that the overall efficiency is around 94.5%, while the overall efficiencies of the topologies proposed in [24] and [25] are 91.5% and 90%, respectively. Hence, it can be seen that the proposed inverter has better performance.

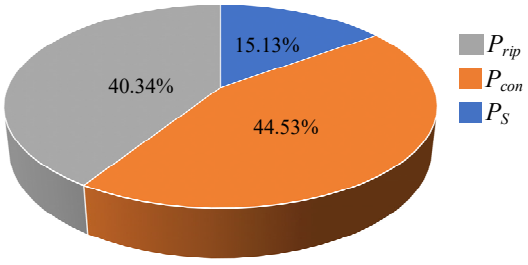


Fig. 8 Power losses distribution.

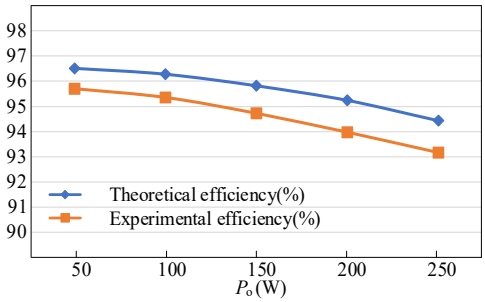


Fig. 9 Efficiency curves of the proposed topology.

5 Simulation and Experiment Analysis

5.1 Simulation Results

In order to examine the performance of the proposed topology and modulation scheme, a simulation model of five-level inverter is developed in MATLAB/Simulink. The simulation parameters are shown in Table 4.

Table 4 Simulation Parameters

Parameters	Values
Input voltage	30 V
Capacitors C_1 and C_2	2200 μF
Switching frequency	2 kHz
Reference wave frequency	50 Hz
Modulation index(M)	0.9
Resistive-Inductive load	50 Ω−15 mH

The simulation results are shown in Fig. 10 - Fig. 12. The output voltage and current of proposed inverter are shown in Fig. 10. It can be seen that voltage of the two capacitors can maintain stability with a small ripple. Fig. 11 shows the voltage stress for each of the switches. It can be seen that only the voltages of S_5 and S_7 are $2V_{dc}$. The current stress for each of the switches is shown in Fig. 12.

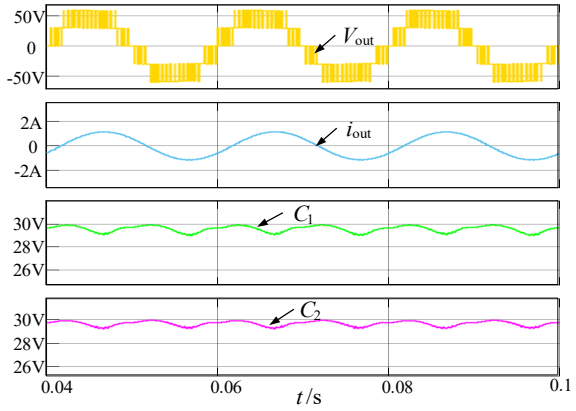
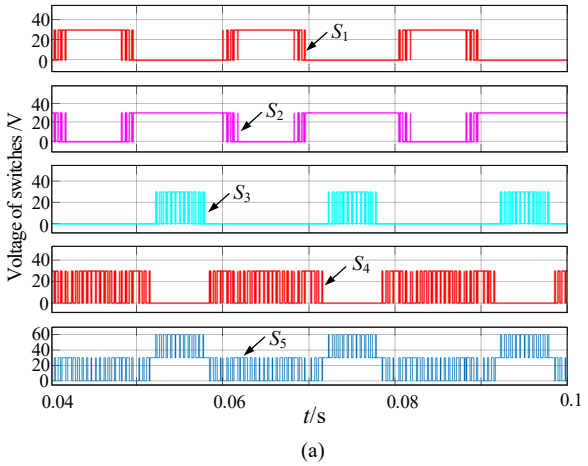


Fig. 10 Simulation results of output voltage, load current, and capacitors voltage.



(a)

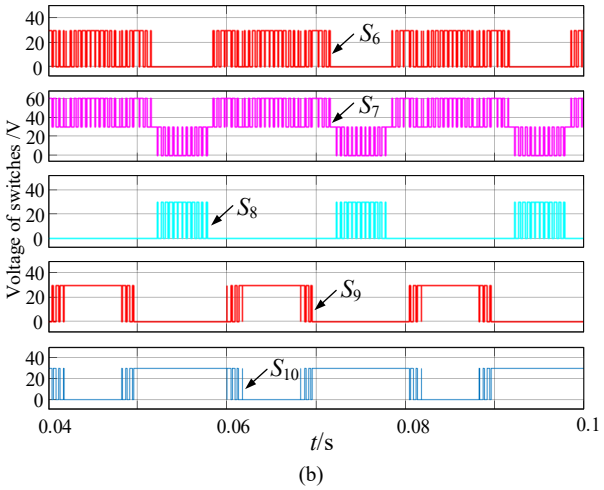


Fig. 11 Voltage stress for each of the switches: (a) voltage across the switches S_1-S_5; (b) voltage across the switches S_6-S_{10}.

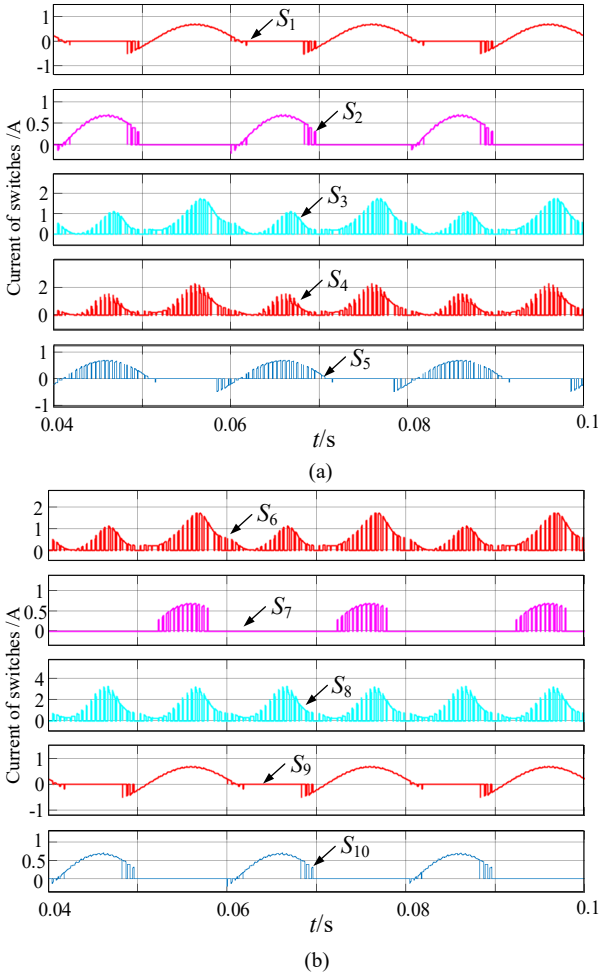


Fig. 12 Current stress for each of the switches: (a) current across the switches S_1-S_5; (b) current across the switches S_6-S_{10}.

5.2 Experimental Results

To validate the feasibility of proposed topology, a five-level prototype was established. The corresponding experiment results and experiment parameters are provided in Fig. 13 and Table 5, respectively.

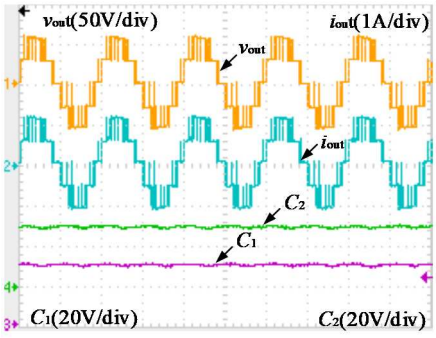
Table 5 Experimental Parameters

Parameters	Values
Input voltage	30 V
Capacitors C_1 and C_2	2200 μF
Switching frequency	2 kHz
Modulation index(M)	0.9, 0.4
Resistive load	50 Ω
Resistive-Inductive load	50 Ω−15 mH

Fig. 13(a) shows experimental waveforms of the output voltage, load current, and capacitors voltage under purely resistive load conditions. It can be seen from this figure that the output voltage levels are ± 60V, ± 30V, and 0, which are consistent with the theoretical analysis of ± $2V_{dc}$, ± V_{dc}, and 0. In addition, the capacitors voltage waveforms are stable and can be maintained at near 30V, which meets the inverter ripple setting requirements. These results confirm the correctness of the inverter structure and modulation method from the experimental point of view.

Fig. 13(b) shows experimental waveforms of the inverter output voltage, load current, and capacitors voltage under a resistive-inductive load. The output voltage in the figure is a five-level wave, the output current is a standard sine wave, and the waveform is stable. The voltage waves of the capacitors C_1 and C_2 both fluctuate at 30V. The capacitor voltage is self-balanced and the ripple fluctuations are less than 3V, which is consistent with the theoretical analysis.

Fig. 13(c) - Fig. 13(e) show voltage waveforms for each of the switching devices of the inverter. It can be seen that the MBV withstood by the ten switches is 60V, that is $2V_{dc}$, which is consistent with the theoretical analysis.



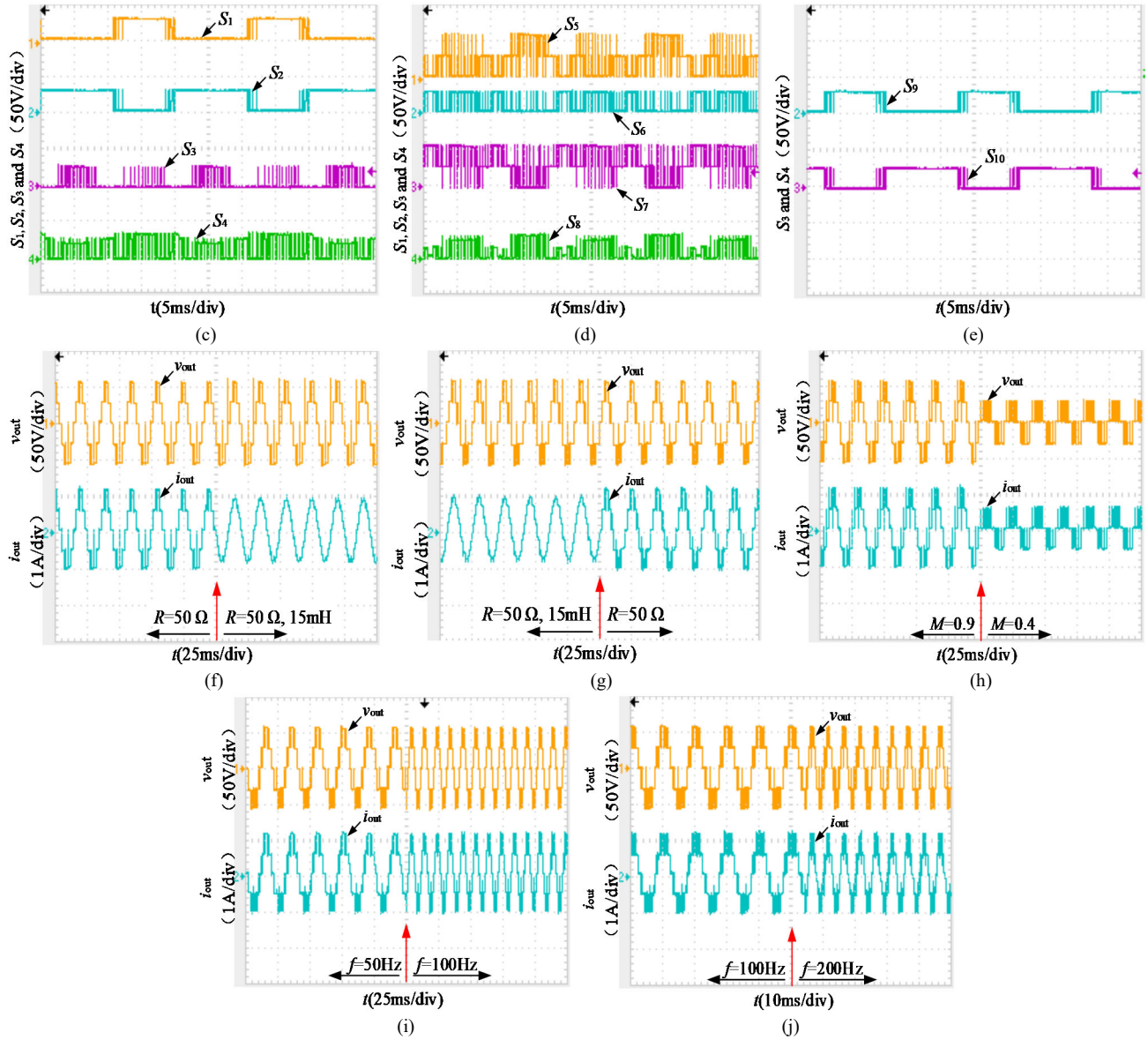


Fig. 13 Experimental results: (a) waveforms of output voltage, output current, and voltage of the capacitors C_1 and C_2 under pure resistive loading conditions; (b) waveforms of output voltage, output current, voltage of the capacitors C_1 and C_2 under resistive-inductive loading conditions; (c) through (e) voltage waveforms of switches; (f) and (g) output voltage and output current when the load changes; (h) output voltage and output current when the modulation changes; (i) and (j) output voltage and output current when the output frequency changes.

The above experiment is a steady-state experiment. It can be seen that the proposed inverter shows good steady-state performance. In order to verify the stability of the proposed inverter structure, the following experiment verifies the dynamic performance of the inverter from three angles: load change, modulation change, and output frequency change. Fig. 13(f) and Fig. 13(g) show waveforms of the output voltage and output current of the proposed inverter from a purely resistive load to a resistive-inductive load, and from a resistive-inductive load to a pure resistive load, respectively. It can be seen that when the load changes, the response is fast, and the proposed inverter can still work stably.

When the modulation index M of the inverter changes, the resulting experimental waveforms of the output voltage and output current are shown in Fig. 13(h). When the index M varies from 0.9 to 0.4, the resulting output voltage changes from five levels to three levels. In this experiment, when M changes, the inverter works normally, and the output voltage and output current can quickly reach the expected waveform.

Fig. 13(i) and Fig. 13(j) show experimental results of the inverter output voltage and output current when the modulation frequency of the inverter is changed. In Fig. 13(i), the inverter output frequency is changed from 50Hz to 100Hz, and in Fig. 13(j), the inverter output frequency is changed from 100Hz to 200Hz. As can be seen from these results, when the frequency of the modulation wave

changes, the output voltage and output current quickly reach the target waveform, and the inverter responds quickly.

Based on the above discussion, it can be seen that the inverter can respond quickly and operate stably when the modulation degree and output frequency change suddenly, which shows the good dynamic performance of the inverter.

6 Conclusion

This study presents an extensible single dc source five-level MLI based on a switched-capacitor structure. The proposed MLI eliminates the need for H-bridge due to the inherent polarity reversal capability. In addition, the voltage of two capacitors can be self-balanced without any auxiliary circuits. Although ten switches are employed, only two switches have a voltage stress of $2V_{dc}$, and only five gate drivers are required, which significantly reduces the total voltage stress and cost of proposed inverter. In addition, the output levels and boosting factor can be raised by employing multiple switched-capacitor cells. Moreover, the maximum blocking voltage for all of the switches is kept within $2V_{dc}$ in the extended structure. A comparative study with other topologies showed that the proposed inverter has the advantages of reducing the TSV, the MBV, and the number of the power devices. Finally, the correctness and feasibility of the proposed multilevel inverter are validated through the simulation and experiment results obtained from a laboratory prototype.

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Yaoqiang Wang received his B.S. degree from Hangzhou Dianzi University, Hangzhou, China, in 2006; and his M.S. and Ph.D. degrees from the Harbin Institute of Technology, Harbin, China, in 2008 and 2013, respectively. He is presently working in the School of Electrical Engineering, Zhengzhou University, Zhengzhou, China. He is also serving as the Director of the Institute of Power Electronics and Energy Systems of Zhengzhou University (PEES-ZZU); the Zhengzhou Municipal Engineering Research Center of Power Control and Systems (ZERC-PCS); and the Henan Provincial Engineering Research Center of Power Electronics and Energy Systems (HERC-PEES). He has authored or coauthored more than 60 technical papers including over 50 journal papers, and is a holder of more than 20 patents. His current research interests include power electronics, renewable power generation, flexible power distribution, electric motor drives, and electrified transportation.

Juncheng Ye was born in Zhoukou, China, in 1999. He received his B.S. degree in Electrical Engineering and Automation from the Henan Polytechnic University, Jiaozuo, China, in 2020. He is presently working towards his M.S. degree in Electrical Engineering at Zhengzhou University, Zhengzhou, China. His current research interests include electric energy conversion and renewable energy generation.

Ruohan Ku received his B.S. degree in Electrical Engineering and Automation from Shihezi University, Shihezi, China, in 2017; and his M.S. degree in Electrical Engineering from Zhengzhou University, Zhengzhou, China, in 2020. He is presently working in the Xuchang Power Supply Company, State Grid Henan Electric Power Co., Ltd., Xuchang, China. His current research interests include electric energy conversion and renewable energy generation.

Yi Wang received his Ph.D. degree from Hohai University, Nanjing, China, in 2020. He is presently working as a Lecturer in the School of Electrical Engineering, Zhengzhou University, Zhengzhou, China. His current research interests include theoretical and algorithmic studies in power system estimation, parameters identification, power system dynamics, signal processing, and cyber security. He is an active reviewer for many international journals.

Jun Liang received his B.S. degree in Electric Power System and Automation from the Huazhong University of Science and Technology, Wuhan, China, in 1992; and his M.S. and Ph.D. degrees in Electric Power System and Automation from the China Electric Power Research Institute (CEPRI), Beijing, China, in 1995 and 1998, respectively. From 1998 to 2001, he was a Senior Engineer with CEPRI. From 2001 to 2005, he was a Research Associate at the Imperial College London, London, ENG, UK. From 2005 to 2007, he was a Senior Lecturer at the University of Glamorgan, Treforest, WLS, UK. He is presently working as a Professor of Power Electronics in the School of Engineering, Cardiff University, Cardiff, WLS, UK. He is also the Coordinator and Scientist-in-Charge of two European Commission Marie-Curie Action ITN/ETN projects: MEDOW (€3.9M) and InnoDC (€3.9M). His current research interests include HVDC, MVDC, FACTS devices, power system stability control, power electronics, and renewable power generation. Professor Liang is a Fellow of the Institution of Engineering and Technology (IET). He is serving as a Chair of both the IEEE UK, and the Ireland Power Electronics Chapter. He is an Editorial Board Member of CSEE JPES. He is an Editor of the IEEE Transactions on Sustainable Energy.