Novel High Step-Up DC-DC Converter for Distributed Generation System

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***Abstract* – In this paper, a novel high step-up DC-DC converter for distributed generation (DG) system is proposed. The concept is to utilize two capacitors and one coupled-inductor. The two capacitors are charged in parallel during the switch-off period and are discharged in series during the switch-on period by the energy stored in the coupled inductor to achieve high step-up voltage gain. In addition, the leakage-inductor energy of the coupled inductor is recycled with a passive clamp circuit. Thus, the voltage stress on the main switch is reduced. The switch with low resistance $R_{DS(ON)}$ can be adopted to reduce the conduction loss. In addition, the reverse-recovery problem of the diodes is alleviated, and thus, the efficiency can be further improved. The operating principle and steady-state analyses are discussed in detail. Finally, a prototype circuit with 24-V input voltage, 400-V output voltage, and 200-W output power is implemented in the laboratory to verify the performance of the proposed converter.**

***Index Terms* – High step-up, DG system, coupled inductor**

I. INTRODUCTION

In recent years, distributed generation (DG) systems based on renewable energy sources (RES) have rapidly developed. The DG systems are composed of microsource like fuel cells, photovoltaic cells, and wind power [1-7]. However, fuel cells and photovoltaic (PV) source are low-voltage source to provide enough DC voltage for generating AC utility voltage. Although PV cells can connect in series to obtain sufficient DC voltage, it is difficult to avoid shadow effect [8-10]. Thus, high step up DC-DC converters are usually used as the front-end converters to step from low voltage up to high voltage which are required to have a large conversion ratio, high efficiency, and small volume [11].

Theoretically, the boost converter can provide high step-up voltage gain with extremely high duty cycle [12]. In practice, the step-up voltage gain is limited by the effect of power switch, rectifier diode, and the equivalent series resistance (ESR) of the inductors and capacitors. Also, the extreme duty cycle operation may result in serious reverse-recovery problem and electromagnetic interference (EMI) problem [13].

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Some converters like the forward, flyback converters can adjust the turns ratio of the transformer to achieve high step-up voltage gain. However, the main switch will suffer high voltage spike and high power dissipation caused by the leakage inductor of the transformer [14]. Although the non-dissipative snubber circuits and active-clamp circuits can employed, the cost is increased due to the extra power switch and high side driver [15].

To improve the conversion efficiency and achieve high step-up voltage gain, many step-up converters have been proposed [16-30]. High step-up voltage gain can be achieved by the use of the switched-capacitor [16], [17] and voltage-lift [18-20] techniques. However, the switch will suffer high charged current and conduction loss.

The converters use the coupled-inductor technique to achieve high step-up gain [21]. However, the leakage inductor leads to a voltage spike on the main switch and affects the conversion efficiency. For this reason, the converters using a coupled-inductor with an active clamp circuit have been proposed [22], [23]. An integrated boost-flyback converter is presented, in which the secondary side of the coupled-inductor is used as a flyback converter [24], [25]. Thus, it can increase the voltage gain. Also, the energy of the leakage inductor is recycled to the output load directly, limiting the voltage spike on the main switch. Additionally, the voltage stress of the main switch can be adjusted by the turns ratio of the coupled-inductor. To achieve high step-up gain, it has been proposed that the secondary side of the coupled-inductor can be used as a flyback and a forward converter [26], [27]. Also, several converters that combine output-voltage stacking to increase voltage gain are proposed [28]. Additionally, a high step-up boost converter that uses multiple coupled inductor with output stacking have been proposed [29], [30].

To achieve high step-up voltage gain and high efficiency, this paper proposes a novel high step-up ratio and clamp-mode converter. The proposed converter adds two capacitors and two diodes on the secondary side of the coupled inductor to achieve high step-up voltage gain. The coupled-inductor can charge two capacitors in parallel and discharge in series. However, the leakage inductor of the coupled-inductor may cause high power loss and a high voltage spike on the switch. Thus, a passive clamping circuit is needed to clamp the voltage level of the main switch and to recycle the energy of the leakage inductor.

II. OPERATING PRINCIPLE OF THE PROPOSED CONVERTER

(A) Derivation of the Proposed Converter

Fig. 1 shows the circuit topology of the proposed converter, which is composed of DC input voltage V_{in}, main switch S, coupled-inductor N_p and N_s, one clamp diode D_1, clamp capacitor C_1, two capacitors C_2 and C_3, two diodes D_2 and D_3, output diode D_o, and output capacitor C_o. The equivalent circuit model of the coupled inductor includes magnetizing inductor L_m, leakage inductor L_k and an ideal transformer. The leakage-inductor energy of the coupled inductor is recycled to capacitor C_1, and thus the voltage across the switch S can be clamped. The voltage stress on the switch is reduced significantly. Thus, low conducting resistance $R_{ds(on)}$ of the switch can be used.

The original voltage-clamp circuit was firstly proposed in Ref. [11] to recycle the energy stored in the leakage inductor. Based on the topology, the proposed converter combines the concept of switched-capacitor and coupled-inductor techniques. Switched-capacitor technique in Ref. [17] has proposed that capacitors can be parallel-charged and series-discharged to achieve high step-up gain. Based on the concept, the proposed converter put capacitors C_2 and C_3 on the secondary-side of coupled inductor. Thus, capacitors C_2 and C_3 are charged in parallel and are discharged in series by the secondary-side of coupled inductor when switch is turned off and turned on. Because the voltage across the capacitors can adjust by turns ratio, the high step-up gain can be achieved significantly. Also, the voltage stress of switch can be reduced. Compared to earlier studies [16-20], the parallel-charged current is not inrush. Thus, the proposed converter has low conduction loss. Besides, the secondary-side leakage inductor of the coupled inductor can alleviate the reverse-recovery problem of diodes, the loss can be reduced. In addition, the proposed converter adds capacitors C_2 and C_3 to achieve high step-up gain without additional winding stage of coupled inductor. The coil is less than other coupled inductor converters.

The main operating principle is that when switch is turned on, the coupled inductor induce voltage on the secondary-side and magnetic inductor L_m is charged by V_{in}. The induced voltage makes V_{in}, V_{C1}, V_{C2} and V_{C3} released energy to output in series. The coupled inductor is used as transformer in forward converter. When switch is turned off, the energy of magnetic inductor L_m is released via the secondary-side of coupled inductor to charge capacitors C_2 and C_3 in parallel. The coupled inductor is used as transformer in flyback converter.

To simplify the circuit analysis, the following conditions are assumed:

1) Capacitors C_1, C_2, C_3 and C_o are large enough. Thus, V_{c1}, V_{c2}, $V_{c3,}$ and V_o are considered as constant in one switching period.
2) The power devices are ideal, but the parasitic capacitor of the power switch is considered.
3) The coupling-coefficient of the coupled-inductor k is equal to $L_m/(L_m+L_k)$ and the turns ratio of the coupled-inductor n is equal to N_s/N_p.

The proposed converter operating in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are analyzed as follows.

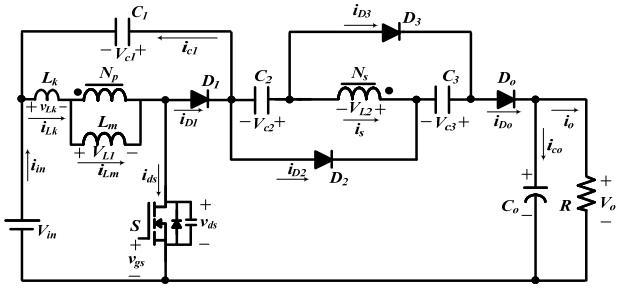


Fig. 1. Circuit configuration of the proposed converter

(B) CCM Operation

This section presents the operation principle of the proposed converter. The following analysis contains the explanation of the power flow direction of each mode. In CCM operation, there are five operating modes in one switching period. Fig. 2 shows typical waveforms and Fig. 3 shows the current-flow path of each modes of the circuit. The operating modes are described as follows:

1) Mode I [t_0, t_1]: During this time interval, S is turned on. Diodes D_1 and D_o is turned off, and D_2 and D_3 are turned on. The current-flow path is shown in Fig. 3(a). The voltage equation on the leakage inductor and magnetic inductor of coupled inductor on the primary-side is expressed as $V_{in}=V_{Lk}+V_{Lm}$. The leakage inductor L_k starts to charge by V_{in}. Due to the leakage inductor L_k, the secondary-side current i_s of the coupled inductor is decreased linearly. Output capacitor C_o provides its energy to load R. When current i_{D2} becomes zero at $t = t_1$, this operating mode is end.
2) Mode II [t_1, t_2]: During this time interval, S remains turned on. Diodes D_1, D_2 and D_3 are turned off and D_o is turned on. The current-flow path is shown in Fig. 3(b). Magnetizing inductor L_m stores energy generated by DC-source V_{in}. Some of the energy of DC-source V_{in} transfers to the secondary-side via the coupled inductor. Thus, the induced voltage V_{L2} on the secondary-side of coupled inductor makes V_{in}, V_{c1}, V_{c2} and V_{c3} connect in series discharge to high-voltage output capacitor C_o and load R. This operating mode ends when switch S is turned off at $t = t_2$.
3) Mode III [t_2, t_3]: During this time interval, S is turned off. Diodes D_1, D_2 and D_3 are turned off, and D_o is turned on. The current-flow path is shown in Fig. 3(c). The energies of leakage inductor L_k and magnetizing inductor L_m charge the parasitic capacitor C_{ds} of main switch S. Output capacitor C_o provides its energy to load R. When the capacitor voltage V_{c1} is equal to $V_{in}+V_{ds}$ at $t = t_3$, diode D_1 conducts and this operating mode is end.
4) Mode IV [t_3, t_4]: During this time interval, S is turned off. Diodes D_1 and D_o are turned on, and D_2 and D_3 are turned off. The current-flow path is shown in Fig. 3(d). The energies of leakage inductor L_k and magnetizing inductor L_m charge clamp capacitor C_1. The energy of leakage inductor L_k is recycled. Current i_{Lk} decreases quickly. Secondary-side voltage V_{L2} of the coupled inductor continues charging high-voltage output capacitor C_o and load R in series until secondary current of the coupled inductor i_s equals to zero. Meanwhile, diodes D_2 and D_3

start to turn on. When i_{Do} is equal to zero at $t = t_4$, this operating mode is end.

5) Mode V [t_4, t_5]: During this time interval, S is turned off. Diodes D_1, D_2 and D_3 are turned on and D_o is turned off. The current-flow path is shown in Fig. 3(e). Output capacitor C_o is discharged to load R. The energy of leakage inductor L_k and magnetizing inductor L_m charge clamp capacitor C_1. Magnetizing inductor L_m released via the secondary-side of coupled inductor and charges capacitors C_2 and C_3. Thus, capacitors C_2 and C_3 are charged in parallel. As the energy of leakage inductor L_k charges capacitor C_1. The current i_{Lk} decreases and i_s increases gradually. This mode ends at $t = t_6$ when S is turned on at the beginning of the next switching period.

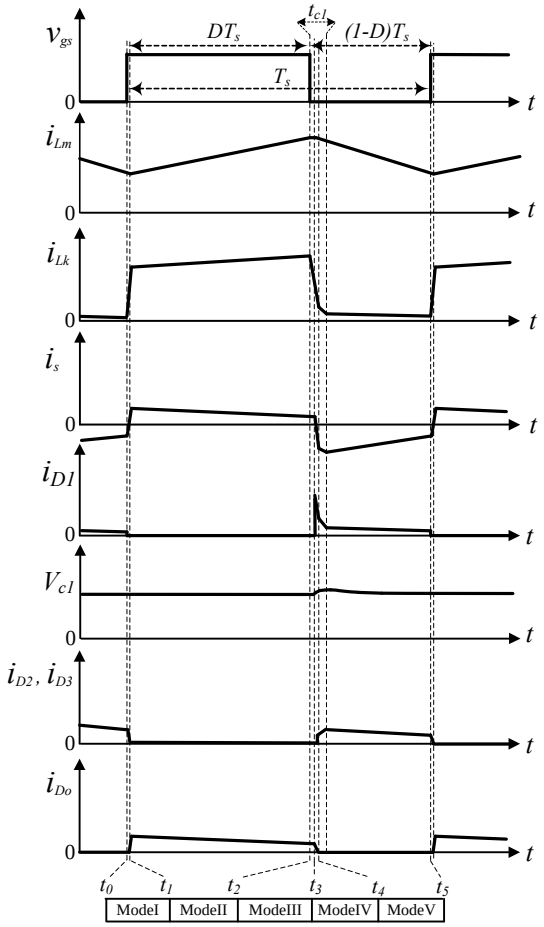
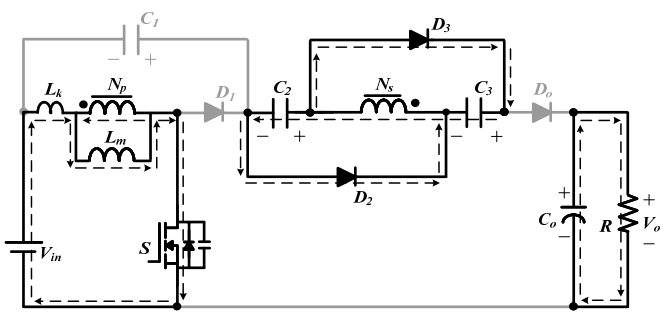
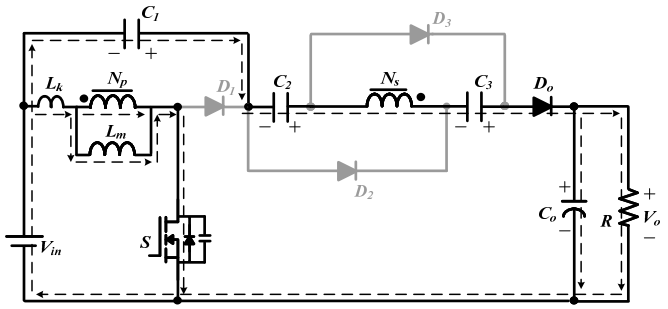


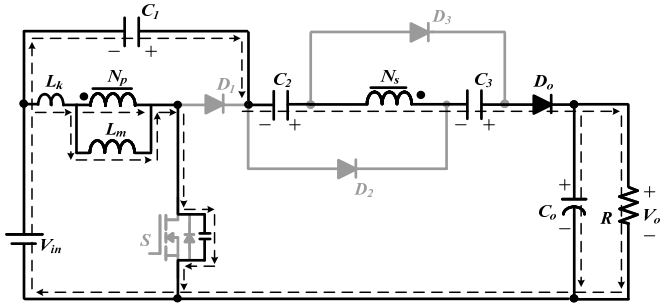
Fig. 2. Some typical waveforms of the proposed converter at CCM operation.



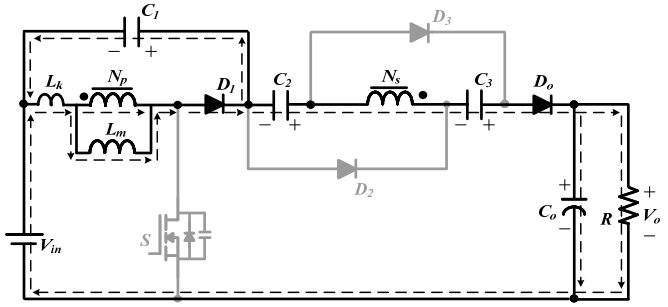
(a) Mode I



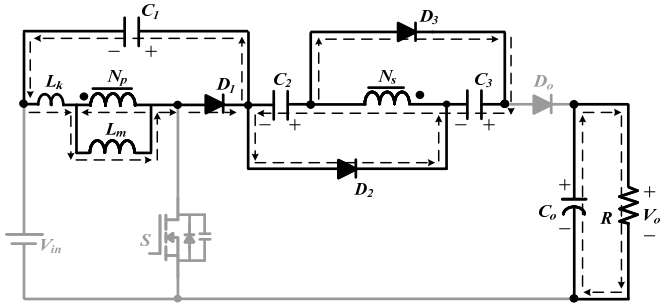
(b) Mode II



(c) Mode III



(d) Mode IV



(e) Mode V

Fig.3. Current-flow path of operating modes during one switching period at CCM operation. (a) Modes I. (b) Modes II. (c) Mode III. (d) Mode IV. (e) Mode V

(C) DCM Operation

To simplify the analysis of DCM operation, leakage inductor L_k of the coupled-inductor is neglected. Fig. 4 shows typical waveforms when the proposed converter operates in DCM, and Fig. 5 shows each mode of operating stages. In this section, there are three modes and the operating modes are described as follows:

1) Mode I [t_0, t_1]: During this time interval, S is turned on. The current-flow path is shown in Fig. 5(a). The magnetizing inductor L_m stores the energy from DC-source V_{in}. Thus,

i_{Lm} increases linearly. Also, the energy of DC-source V_{in} is transferred to the secondary side of the coupled inductor, which is connected with capacitors C_2 and C_3 in series to provide their energies to output capacitor C_o and load R. This mode is end when S is turned off at $t = t_1$.

2) Mode II [t_1, t_2]: During this time interval, S is turned off. The current-flow path is shown in Fig. 5(b). The energy of magnetizing inductor L_m transfers to capacitors C_1, C_2 and C_3. Output capacitor C_o provides its energy to load R. This mode is end when the energy stored in L_m is depleted at $t = t_2$.

3) Mode III [t_2, t_3]: During this time interval, S remains turned off. The current-flow path is shown in Fig. 5(c). Since the energy stored in L_m is depleted, the energy stored in C_o is discharged to load R. This mode is end when S is turned on at $t = t_3$.

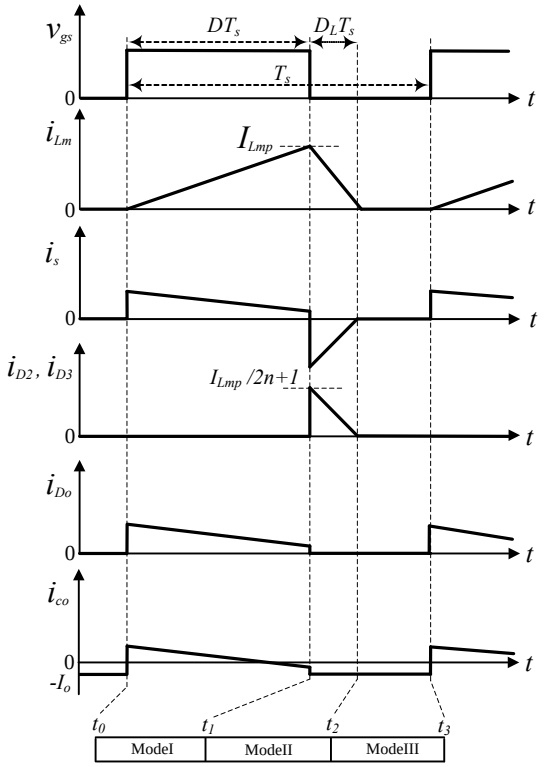
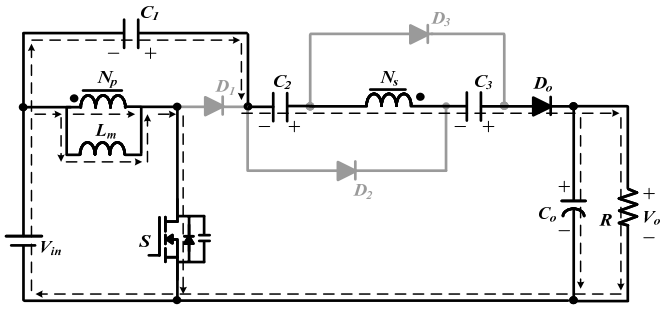
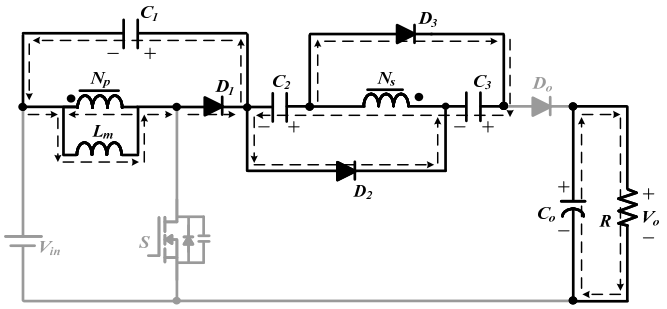


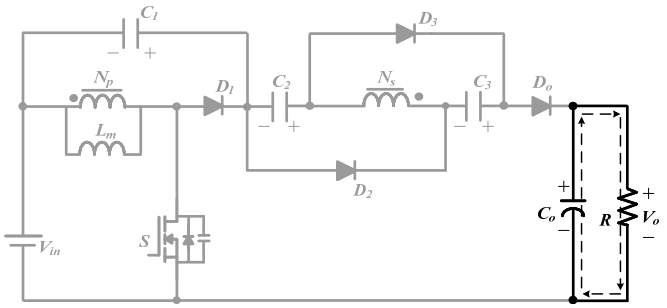
Fig. 4. Some typical waveforms of the proposed converter at DCM operation.



(a) Mode I



(b) Mode II



(c) Mode III

Fig. 5. Current-flow path of operating modes during one switching period at DCM operation. (a) Modes I. (b) Mode II. (c) Modes III.

III. Steady-State Analysis of the Proposed Converter

(A) CCM Operation

According to previous work Ref. [11], the energy stored in the leakage inductor L_k of the coupled inductor releases to capacitor C_1. The energy released duty cycle D_{c1} can be expressed as

$$D_{c1} = \frac{t_{c1}}{T_s} = \frac{2(1-D)}{n+1}, \tag{1}$$

where t_{c1} is the time interval showed on Fig. 2.

Because the time of modes I and III are significantly short, only modes II, IV and V are considered in the steady-state analysis at CCM operation.

In mode II, the following equations can be written based on Fig. 3(b).

$$v_{Lk}^{II} = \frac{L_{k1}}{L_m + L_{k1}} V_{in} = (1-k)V_{in}, \tag{2}$$

$$v_{L1}^{II} = \frac{L_m}{L_m + L_{k1}} V_{in} = kV_{in}, \tag{3}$$

$$v_{L2}^{II} = nv_{L1}^{II} = nkV_{in}. \tag{4}$$

$$V_o = V_{in} + V_{c1} + V_{c2} + v_{L2}^{II} + V_{c3}. \tag{5}$$

By applying the voltage-second balance principle of inductor, the following equations are given as

$$\int_0^{DT_s} v_{Lk}^{II} dt + \int_{DT_s}^{T_s} v_{Lk}^{V} dt = 0. \tag{6}$$

$$\int_0^{DT_s} v_{L1}^{II} dt + \int_{DT_s}^{T_s} v_{L1}^{V} dt = 0. \quad (7)$$

$$\int_0^{DT_s} v_{L2}^{II} dt + \int_{DT_s}^{T_s} v_{L2}^{V} dt = 0. \quad (8)$$

Substituting (1), (2), (3) and (4) into (6), (7), (8), the voltages in mode V can be derived. According to the definition of voltage direction, the voltages are expressed as

$$v_{Lk}^{V} = -\frac{D(n+1)(1-k)}{2(1-D)} V_{in}, \quad (9)$$

$$v_{L1}^{V} = -\frac{Dk}{1-D} V_{in}, \quad (10)$$

$$v_{L2}^{V} = -\frac{nDk}{1-D} V_{in}, \quad (11)$$

Also, capacitors of C_1, C_2 and C_3 are charged in mode V. The voltage across capacitors C_1, C_2 and C_3 can be represented based on Fig. 3(e)

$$V_{c1} = -V_{Lk}^{V} - V_{L1}^{V} = \frac{D}{1-D} \cdot V_{in} \cdot \frac{(1+k)+(1-k)n}{2}, \quad (12)$$

$$V_{c2} = V_{c3} = -v_{L2}^{V} = \frac{nDk}{1-D} V_{in}. \quad (13)$$

Substituting (4), (12) and (13) into (5), the voltage gain is obtained as

$$M_{CCM} = \frac{V_o}{V_{in}} = \frac{1+nk}{1-D} + \frac{D}{1-D} \cdot \frac{(k-1)+n(1+k)}{2}. \quad (14)$$

At k = 1, the ideal voltage gain is written as

$$M_{CCM} = \frac{1+n+nD}{1-D} \quad (15)$$

The schematic of the voltage-gain versus the duty-ratio under various coupling-coefficients of the coupled-inductor is shown in Fig. 6. It shows that voltage gain is not very sensitive to the coupling-coefficient.

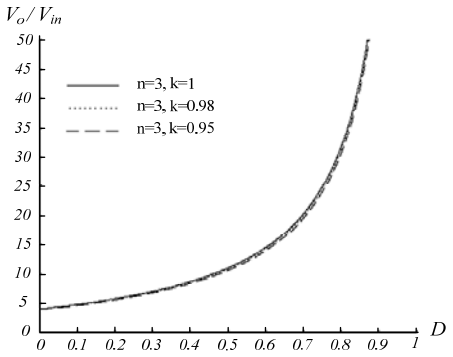


Fig. 6. Voltage-gain versus duty-ratio at CCM operation under n = 3 and various k.

Fig. 7 shows the voltage gain versus the duty ratio of the proposed converter which compared with the converters in previous work [27] and [28] at CCM operation under k =1 and n =3. The voltage gain of the proposed converter is higher than the converters in [27] and [28].

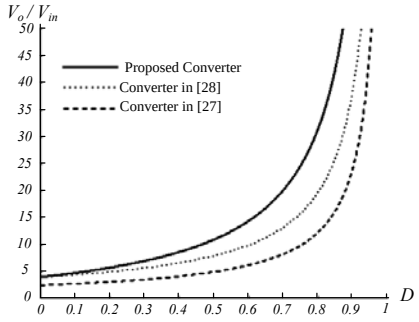


Fig. 7. Voltage-gain versus duty-ratio of the proposed converter, the converters in [27] and [28] at CCM operation under n = 3 and k =1.

According to the description of operating modes, voltage stresses on active switch S and diodes D_1, D_2, D_3, and D_o are given as

$$V_{ds} = \frac{1}{1-D} V_{in} = \frac{V_o + nV_{in}}{2n+1}, \quad (16)$$

$$V_{D1} = \frac{1}{1-D} V_{in} = \frac{V_o + nV_{in}}{2n+1}, \quad (17)$$

$$V_{D2} = V_{D3} = V_{Do} = \frac{n}{1-D} V_{in} = \frac{n}{2n+1}(V_o + nV_{in}). \quad (18)$$

Equations (16) - (18) mean that under the same voltage ratio, the voltage stresses can be adjusted by the turns ratio of the coupled inductor.

(B) DCM Operation

In DCM operation, three modes are discussed. The typical waveforms are shown in Fig. 4. In mode I, switch S is turned on. Thus, the following equations can be formulated based on Fig. 5(a)

$$v_{L1}^{I} = V_{in}, \quad (19)$$

$$v_{L2}^{I} = nV_{in}. \quad (20)$$

$$V_o = V_{in} + V_{c1} + V_{c2} + v_{L2}^{I} + V_{c3}. \quad (21)$$

The peak value of the magnetizing-inductor current is calculated as

$$I_{Lmp} = \frac{V_{in}}{L_m} DT_s. \quad (22)$$

In mode II, the following equation can be expressed based on Fig. 5(b):

$$v_{L1}^{II} = -V_{c1}, \quad (23)$$

$$v_{L2}^{II} = -V_{c2} = -V_{c3}. \quad (24)$$

In mode III, the following equation can be derived from Fig. 5(c):

$$v_{L1}^{III} = v_{L2}^{III} = 0. \tag{25}$$

By applying the voltage-second balance principle of coupled inductor, the following equations are given as

$$\int_0^{DT_s} v_{L1}^{I} dt + \int_{DT_s}^{(D+D_L)T_s} v_{L1}^{II} dt + \int_{(D+D_L)T_s}^{T_s} v_{L1}^{III} dt = 0, \tag{26}$$

$$\int_0^{DT_s} v_{L2}^{I} dt + \int_{DT_s}^{(D+D_L)T_s} v_{L2}^{II} dt + \int_{(D+D_L)T_s}^{T_s} v_{L2}^{III} dt = 0. \tag{27}$$

Substituting (19), (20), (23), (24), and (25) into (26) and (27), the voltage across the capacitors C_1, C_2 and C_3 are obtained as follows:

$$V_{c1} = \frac{D}{D_L} V_{in}, \tag{28}$$

$$V_{c2} = V_{c3} = \frac{nD}{D_L} V_{in}, \tag{29}$$

Substituting (20), (28) and (29) into (21), the voltage gain is obtained as follows:

$$V_o = \left[\frac{D}{D_L}(2n+1) + (n+1) \right] V_{in}. \tag{30}$$

According to (30), the duty cycle D_L can be derived as

$$D_L = \frac{(1+2n)DV_{in}}{V_o - (1+n)V_{in}}. \tag{31}$$

From Fig. 4, the energy stored on capacitor C_2 is fully released to capacitor C_o and load R in steady state. Also, the average current I_{Do} is equal to I_{D2}, thus the average current of i_{co} is computed as

$$I_{co} = I_{Do} - I_o = I_{D2} - I_o = \frac{1}{2} D_L \frac{I_{Lmp}}{2n+1} - I_o. \tag{32}$$

Because I_{co} is equal to zero under steady state, Equations (22), (31) can be substitute into (32) yields

$$\frac{D^2 V_{in}^2 T_s}{2\left[V_o - (1+n)V_{in}\right] L_m} = \frac{V_o}{R}. \tag{33}$$

Then, the normalized magnetizing-inductor time constant is defined as

$$\tau_{Lm} \equiv \frac{L_m}{RT_s} = \frac{L_m f_s}{R}, \tag{34}$$

where f_s is the switching frequency.
Substituting (34) into (33), the voltage gain is given by

$$M_{DCM} = \frac{V_o}{V_{in}} = \frac{1+n}{2} + \sqrt{\frac{(1+n)^2}{4} + \frac{D^2}{2\tau_{Lm}}}. \tag{35}$$

The curve of the voltage gain, shown in Fig. 8, illustrates the voltage-gain versus the duty-ratio under various τ_{Lm}.

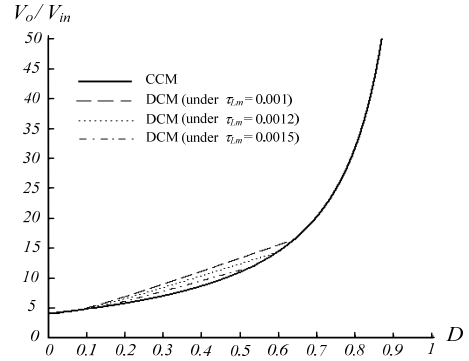


Fig. 8. Voltage-gain versus duty-ratio at DCM operation under various τ_{Lm} and at CCM operation under n = 3 and k = 1.

(C) Boundary Operating Condition between CCM and DCM

If the proposed converter is operated in boundary-condition mode (BCM), the voltage gain of CCM operation is equal to the voltage gain of DCM operation. From (15) and (35), the boundary normalized magnetizing-inductor time constant, τ_{LmB}, can be derived as

$$\tau_{LmB} = \frac{D(1-D)^2}{2(1+2n)(1+n+nD)}. \tag{36}$$

The curve of τ_{LmB} versus the duty ratio of the proposed converter is plotted in Fig. 9. If τ_{Lm} is larger than τ_{LmB}, the proposed converter is operated in CCM operation.

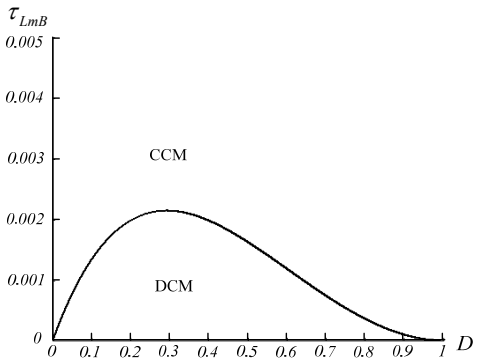


Fig. 9. Boundary condition of the proposed converter under n = 3.

IV. Design and Experiment of the Proposed Converter

To verify the performance of the proposed converter, a prototype circuit is implemented in the laboratory. The specifications are as follows:

1) input DC voltage V_{in} : 24 V
2) output DC voltage V_o: 400 V
3) maximum output power: 200 W
4) switching frequency: 50 kHz
5) MOSFET S: IRFB4410ZPBF

6) Diodes D_1: SBR20A100CTFP, D_2/D_3 : DESI30, and D_o : BYR29

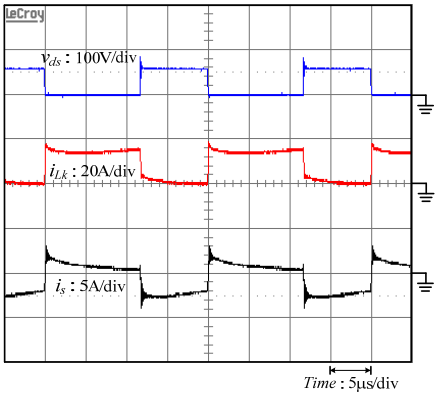
7) Coupled inductor: ETD-59, core pc40, $N_p : N_s = 1 : 4$ $L_m = 48$ μH; $L_k = 0.25$ μH

8) Capacitors C_1: 56 μF/ 100 V, C_2/C_3 : 22 μF/ 200 V, and C_o : 180 μF/ 450 V

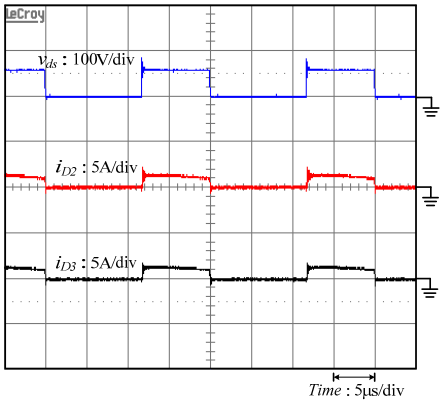
Fig. 10 shows the measured waveforms for full-load P_o = 200 W and V_{in} = 24 V. The proposed converter is operated in CCM under full-load condition. The steady-state analysis can demonstrate in the experimental results. In the measured waveforms, the voltage V_{ds} across the main switch is clamped at appropriately 84 V during the switch-off period. Therefore, a low-voltage-rated switch can be adopted to make the proposed converter reduce its conduction loss.

In Fig. 10(a), the waveform of secondary current i_s of the coupled inductor shows that the proposed converter is operated in CCM because the current is not equal to zero when the switch is turned on. In Fig. 10(b), the waveforms of i_{D2} and i_{D3} show that capacitors C_2 and C_3 are charged in parallel, which verify the concept of the proposed converter. Fig. 10(c) shows that the energy of leakage inductor L_k is released to capacitor C_1 through diode D_1. Fig. 10(d) reveals that V_{c1} and V_{c2} are satisfied Equations (12) and (13). In addition, output voltage V_o is consistent with Equation (15). Fig. 10(e) shows the voltage stress of main switch and diodes, and demonstrates the consistency of Equations (16), (17), and (18). Fig. 11 shows the light-load waveforms. The output voltage is about 400 V and the analysis of the DCM of the proposed converter is demonstrated. Fig. 12 shows the proposed converter under the output power variation between light-load 30 W and full-load 200 W.

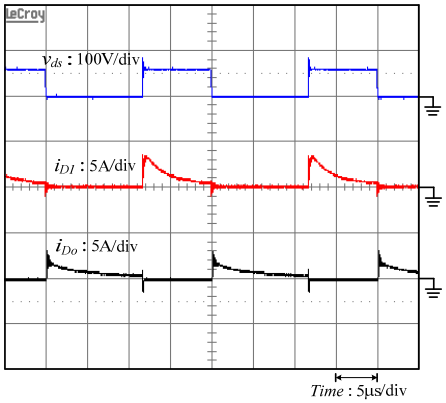
Fig. 13 shows the conversion efficiency of the proposed converter, which the maximum efficiency is around 95.88% at P_o= 100 W and the full-load efficiency is appropriately 95.03 % at P_o= 200 W.



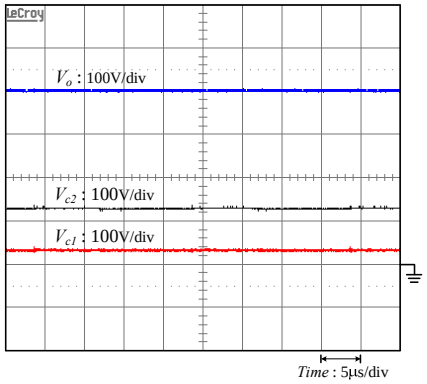
(a)



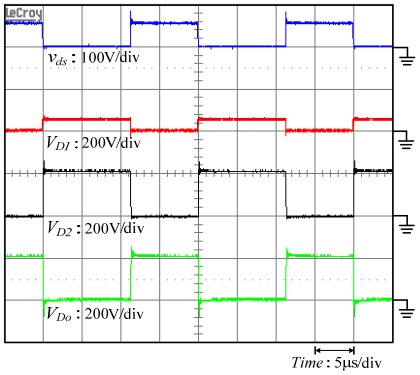
(b)



(c)

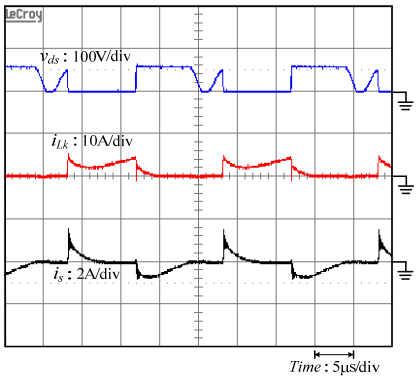


(d)

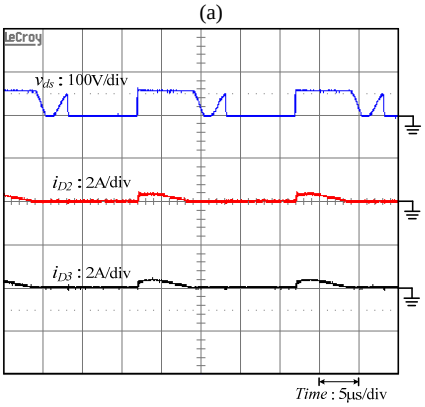


(e)

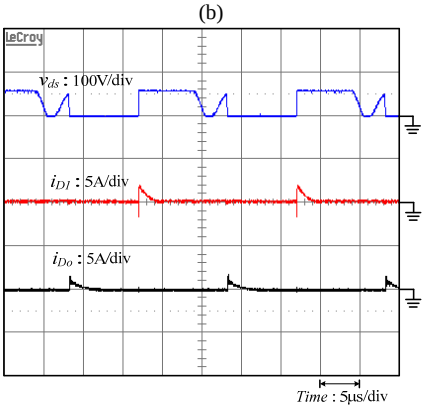
Fig. 10. Experiment results under full-load P_o = 200 W.



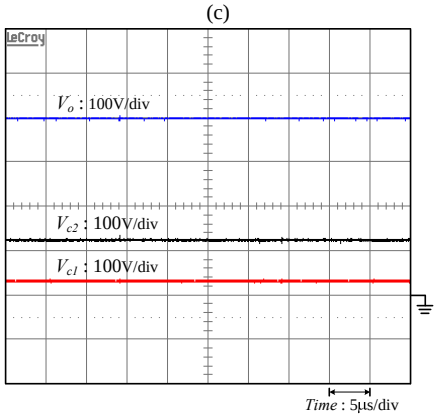
(a)



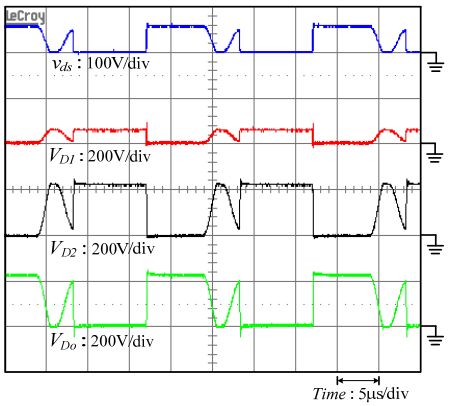
(b)



(c)



(d)



(e)

Fig. 11. Experiment results under light-load P_o = 30 W.

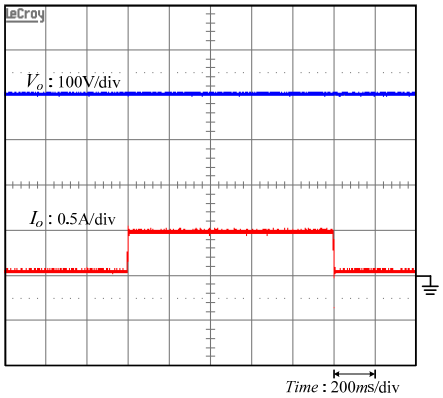


Fig. 12. Load variation between light-load P_o = 30 W and full-load P_o = 200 W.

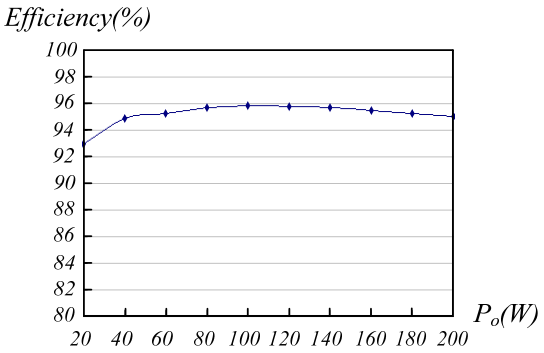


Fig. 13. Experimental conversion efficiency.

V. Conclusions

This paper proposed a novel high step-up DC-DC converter for DG system. By using the capacitor charged in parallel and discharged in a series by the coupled-inductor, high step-up voltage gain and high efficiency are achieved. The steady-state analyses are discussed in detail. Finally, a 24-400 V / 200 W prototype circuit of the proposed converter is put into operation in the laboratory. Experimental results confirm that high efficiency and high step-up voltage gain can be achieved. The peak efficiency is 95.88%. Additionally, the voltage on the main switch is clamped at 84 V, thus low voltage ratings and low on-state resistance $R_{DS(ON)}$ switch can be selected.

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