Novel High Step-Up DC-DC Converter with Coupled-Inductor and Switched-Capacitor Techniques

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***Abstract* –A novel high step-up DC-DC converter with coupled-inductor and switched-capacitor techniques is proposed in this paper. The capacitors are charged in parallel and are discharged in series by the coupled inductor, stacking on the output capacitor. Thus, the proposed converter can achieve high step-up voltage gain with appropriate duty ratio. Besides, the voltage spike on the main switch can be clamped. Therefore, low ON-state resistance $R_{DS(ON)}$ of the main switch can be adopted to reduce the conduction loss. The efficiency can be improved. The operating principle and steady-state analyses are discussed in detail. Finally, a prototype circuit with 24-V input voltage, 400-V output voltage, and 200-W output power is implemented in the laboratory. Experiment results confirm the analysis and advantages of the proposed converter.**

***Index Terms* – High step-up voltage gain, coupled-inductor, switched capacitor**

I. INTRODUCTION

Renewable energy systems are more and more widely used to provide electric energy. However, the fuel cells, photovoltaic arrays source are low-voltage source, needing step-up DC-DC converter as the front-stage to boost low voltage to high voltage for inverter to feed AC utility. Although the PV solar cell can connect in series to get high voltage for grid-connected, the voltage might effect by shadow effect. Also, the broken of one of the PV array leads to shut down the system. By using the high step-up converters, modules can worked independently to generated power as microgrid and avoid the effect [1]-[3]. Theoretically, Boost and buck-boost converters can provide high step-up voltage gain with extremely high duty ratio. In practice, the voltage gain is limited by the effect of power switch, rectifier diode, and equivalent series resistance (ESR) of inductor and capacitor. Also, the extreme high duty-ratio operation may result in serious reverse-recovery problem, low efficiency and the electromagnetic interference (EMI) problem [4].

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Generally speaking, high step-up converter is used for these applications which required to have high voltage gain, and high efficiency [5], [6]. To achieve high step-up voltage gain, many converters have been proposed. The means on the literature can be discussed in two sections: capacitor means and magnetic means.

Capacitor means include cascade technique, switched-capacitor technique and voltage-lift technique. Two cascade boost converter can achieve high step-up voltage gain but it has energy-two-processing structure [7]. Thus, the efficiency is low and needs two switches. The voltage-lift technique and switched-capacitor can achieve high step-up voltage gain [8]-[12]. However, the main switch suffers high transient current, the conduction loss is increased.

Magnetic means include coupled-inductor technique. The switched coupled-inductor technique is proposed. The converters can achieve high step-up voltage gain by adjusting the turns ratio of coupled inductor [13]. Although the leakage energy can send to the output directly, the voltage stress of switch is equal to output voltage. It is difficult to chose low $R_{ds(on)}$ switch. Thus, the converter is proposed [14]. The third winding is added and the voltage stress of main switch is reduced. Low $R_{ds(on)}$ switch can be chose to reduce conduction loss. The switched coupled-inductor technique is a very good method to achieve high step-up voltage gain. This technique can apply in many converters and achieve a good performance [15]. However, once the voltage of secondary-side is build, the current-flowing path of leakage inductor is cut. If the energy of leakage inductor cannot release to output totally, some energy may dissipation on switch. The passive clamp circuit for coupled inductor converter is proposed which can recycle the energy of leakage inductor totally [16]. Also, the converters using a coupled inductor with an active clamp circuit have been proposed, but the cost increases due to the extra power switch and high-side driver [17], [18]. An integrated boost-flyback converter is proposed. The coupled-inductor is used as a transformer in flyback converter and the converter uses output-voltage stacking to achieve high step-up voltage gain. Besides, the energy of leakage inductor is recycled into the output capacitor directly. Thus, the voltage spike of the main switch is limited. [19], [20]. To have large high step-up voltage gain, some converters have been proposed which use the coupled-inductor as a transformer in flyback and forward converter. The utilization of core is added [21]-[23]. Additionally, many converters using three-output-voltage

stacking to increase voltage gain are proposed [24]-[26]. The boost-sepic converter with the coupled-inductor and output stacking techniques has been proposed [27]. The high step-up boost converter uses multiple coupled-inductor of output stacking is proposed [28], [29]. To increase the voltage gain, the converters add the number of turns ratio and extra additional winding stages. The complexity is added.

This paper proposes a novel high step-up voltage gain converter. The proposed converter uses the coupled-inductor and switched-capacitor techniques. The coupled inductor is operated as transformer in flyback and forward converters. Thus, the capacitors on the output-stacking are charged in parallel and are discharged in series to achieve high step-up gain. Also, the voltage spike of the main switch is limited and voltage stress can be adjusted by the turns ratio of the coupled-inductor. Therefore, low ON-state resistance $R_{DS(ON)}$ of the main switch can be adopted to reduce the conduction loss.

II. Operating Principle of the Proposed Converter

Fig. 1 shows the circuit topology of the proposed converter. The equivalent circuit model of the coupled inductor includes the magnetizing inductor L_m, leakage inductor L_k and an ideal transformer. This converter consists of one power switch, six diodes and six capacitors. The leakage-inductor energy of the coupled inductor is recycled to the capacitor C_1, and thus the voltage across the switch S can be clamped. Also, the voltages across the capacitors C_2, C_3, C_4 and C_5 can be adjusted by the turns ratio of the coupled inductor. The voltage level of the switch is reduced significantly and low conducting resistance $R_{ds(on)}$ of the switch can be used. Thus, the efficiency of the proposed converter can be increased and high step-up voltage gain can be achieved.

When switch S is turned on, DC source V_{in} charges leakage inductor L_k, magnetic inductor L_m and the coupled inductor induced voltage V_{L2} on the secondary-side. Voltages V_{L2} and V_{c4} connected in series to charge capacitor C_5. Meanwhile, Voltages V_{L2} and V_{c3} connected in series to charge capacitor C_2. Thus, two capacitors C_2 and C_5 are charge in parallel. When switch S is turned off, the energy of leakage inductor L_k is released to output capacitor C_1 directly and magnetic energy of L_m released by the coupled inductor. The induced voltage V_{L2} on the secondary-side of coupled inductor charges capacitors C_3 and C_4 in parallel. Also, voltages V_{L2}, V_{c2} and V_{c5} are connected in series to charge output capacitor C_6. The output voltage is stacked by capacitors C_1 and C_6. The high step-up voltage gain is achieved. The energy of leakage inductor is sent to output. The voltage stress of main switch is clamped.

To simplify the circuit analysis, the following conditions are assumed:

1) Capacitors C_1-C_6 are large enough. Thus, V_{c1}-V_{c6} are considered as constant in one switching period.
2) The power devices are ideal, but the parasitic capacitor of the power switch is considered.
3) The coupling-coefficient of the coupled-inductor k is equal to $L_m/(L_m+L_k)$ and the turns ratio of the coupled-inductor n is equal to N_s/N_p.

The proposed converter operating in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are analyzed as follows.

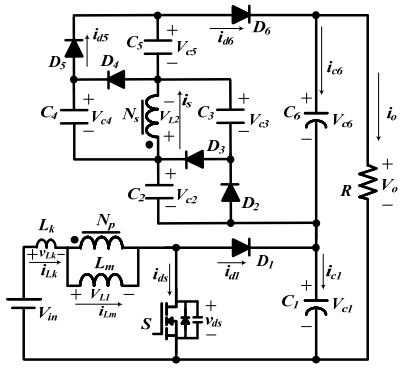


Fig. 1 Circuit configuration of the proposed converter

(A) CCM Operation

Based on the above assumptions, fig. 2 illustrates the typical waveforms and fig. 3 shows the topological stages of the proposed converter. The operating modes are described as follows:

1) Mode I [t_0, t_1]: During this time interval, S is turned on. Diodes D_1, D_2, and D_5 are turned off, and D_3, D_4 and D_6 are turned on. The current-flow path is shown in fig. 3(a). The voltage of primary-side is V_{in}= v_{Lk}+V_{L1}. Thus, leakage inductor L_k and magnetic inductor L_m is charged by DC-source V_{in}. The primary current i_{Lk} increases linearly. Due to leakage inductor L_k, the secondary-side current i_s decreases linearly. Secondary-side voltage V_{L2}, V_{c2} and V_{c5} are connected in series to charge output capacitor C_6 and to provide the energy to load R. Because i_s decreases linearly, the reverse-recovery problem of the diode is alleviated. When current i_s becomes zero at $t = t_1$, this operating mode is ended.
2) Mode II [t_1, t_2]: During this time interval, S is still turned on. Diodes D_1, D_3, D_4 and D_6 are turned off, and D_2 and D_5 are turned on. The current-flow path is shown in fig. 3(b). The magnetizing inductor L_m is charged by DC-source V_{in}. The coupled inductor induces voltage V_{L2} on the secondary-side. Voltage V_{L2} which is connecting V_{C3} in series and connecting V_{C4} in series charge C_2 and C_5 in parallel. A part of the energy of DC-source V_{in} is transferred to capacitors C_2 and C_5 via the coupled inductor. Also, the energies of C_3 and C_4 are transferred to capacitors C_2 and C_5 together. Meanwhile, voltages V_{c2} and V_{c5} are approximately equal to nV_{in}+V_{c3}. The output capacitor and C_1 and C_6 provides its energy to load R. This operating mode is ended when switch S is turned off at $t = t_2$.
3) Mode III [t_2, t_3]: During this time interval, S is turned off. Diodes D_1, D_3, D_4 and D_6 are turned off, and D_2 and D_5 are turned on. The current-flow path is shown in fig. 3(c). The energies of leakage inductor L_k and magnetizing inductor L_m are released to the parasitic capacitor C_{ds} of switch S. Capacitors C_2 and C_5 are charged by DC-source V_{in}. Output capacitors C_1 and C_6 provide energy to load R. When the capacitor voltage V_{c1} is equal to V_{in}+V_{ds} at $t = t_3$, diode D_1 is conducted and this operating mode is ended.

4) Mode IV [t_3, t_4]: During this time interval, S is turned off. Diodes D_1, D_2, and D_5 are turned on, and D_3, D_4, and D_6 are turned off. The current-flow path is shown in fig. 3(d). The energies of leakage inductor L_k and magnetizing inductor L_m is released to capacitor C_1. Thus, the voltage across the switch is clamped at V_{c1}. The current i_{Lk} decreases quickly. The secondary-side voltage of the coupled inductor V_{L2} charges capacitors C_2 and C_5 in parallel until the secondary-side current i_s equals zero. Thus, diodes D_2 and D_5 are cut off at $t = t_4$. This operating mode is ended.
5) Mode V [t_4, t_5]: During this time interval, S is turned off. Diodes D_1, D_3, D_4 and D_6 are turned on, and D_2 and D_5 are turned off. The current-flow path is shown in fig. 3(e). The energies of leakage inductor L_k and magnetizing inductor L_m is released to capacitor C_1. Capacitors C_3 and C_4 are charged in parallel by the magnetizing-inductor energy via coupled inductor. Simultaneously, secondary-side voltage V_{L2} is connected with V_{c2} and V_{c5} in series and charges output capacitor C_6. This operating mode is ended when capacitor C_1 starts to discharge at $t = t_5$.
6) Mode VI [t_5, t_6]: During this time interval, S is still turned off. Diodes D_3, D_4 and D_6 are turned on, and D_1, D_2 and D_5 are turned off. The current-flow path is shown in fig. 3(f). The magnetizing energy of L_m is transferred to capacitors C_3 and C_4 by coupled inductor. Thus, two capacitors are charged in parallel. Also, V_{L2}, V_{c2} and V_{c5} are connected in series and charge capacitor C_6. This mode is ended at $t = t_6$ when S is turned on at the beginning of the next switching period.

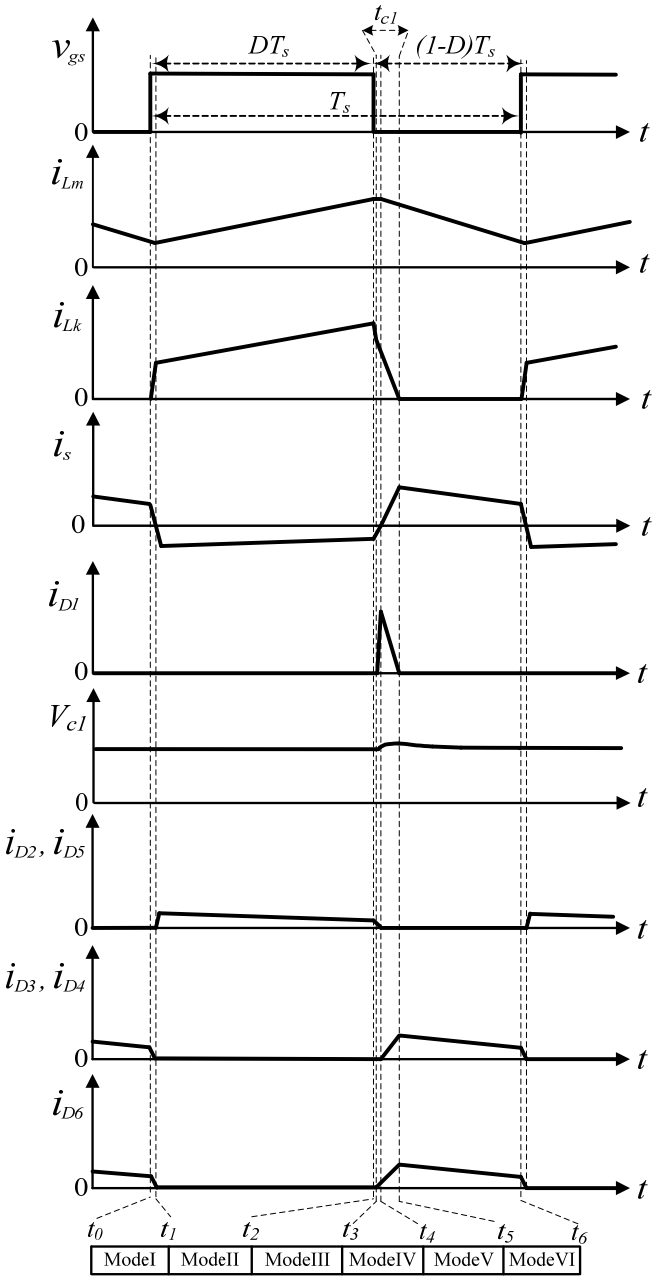
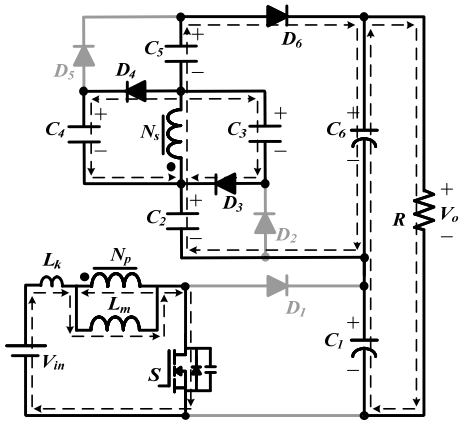
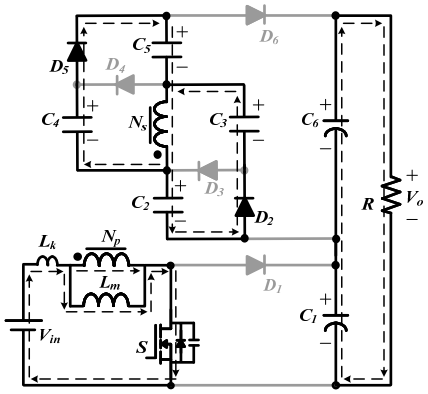


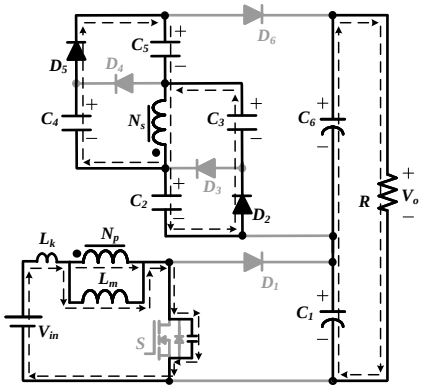
Fig. 2 Some typical waveforms of the proposed converter at CCM operation.



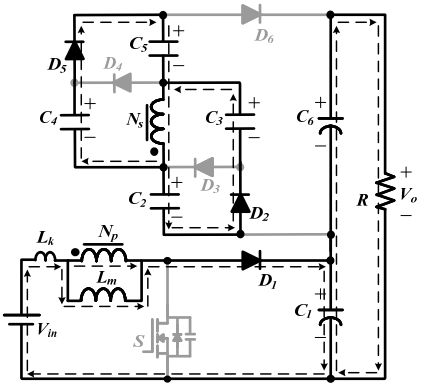
(a) Mode I



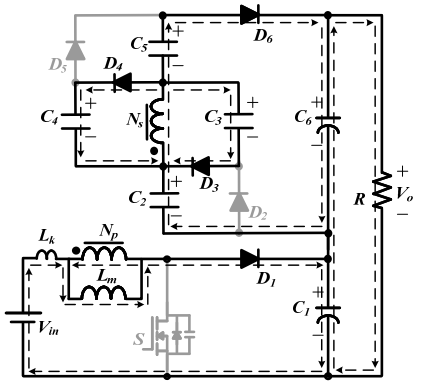
(b) Mode II



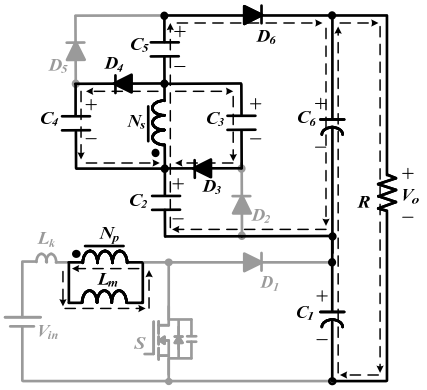
(c) Mode III



(d) Mode IV



(e) Mode V



(f) Mode VI

Fig. 3 Current-flow path of operating modes during one switching period at CCM operation. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V. (f) Mode VI.

(B) DCM Operation

To simplify the analysis of DCM operation, the leakage inductor L_k of the coupled-inductor is neglected. Fig. 4 shows typical waveforms of the proposed converter operated in DCM. Fig. 5 shows the operating stages of each mode. The operating modes are described as follows:

1) Mode I [t_0, t_1]: During this time interval, S is turned on. The current-flow path is shown in fig. 5(a). The energy of DC-source V_{in} charges magnetizing inductor L_m. Thus, i_{Lm} is increased linearly. Also, the secondary side of the coupled inductor is connected series with capacitor C_3 or C_4 and releases their energies to charge capacitors C_2 and C_5 in parallel. Output capacitors C_1 and C_6 provide energy to load R. This mode is ended when S is turned off at $t = t_1$.
2) Mode II [t_1, t_2]: During this time interval, S is turned off. The current-flow path is shown in fig. 5(b). The energies of DC source V_{in} and magnetizing inductor L_m are transferred to capacitors C_1 and load R. Similarly, capacitors C_2 and C_5 are discharged in series with DC source V_{in} and magnetizing inductor L_m to capacitor C_6 and load R. Meanwhile, the energy of magnetizing inductor L_m is transferred to capacitors C_3 and C_4 by coil N_s. This mode is ended when the energy stored in L_m is empty at $t = t_2$.
3) Mode III [t_2, t_3]: During this time interval, S is turned off. The current-flow path is shown in fig. 5(c). Since the energy stored in L_m is empty, the energy stored in C_1 and C_6 are discharged to load R. This mode is ended when S is turned on at $t = t_3$.

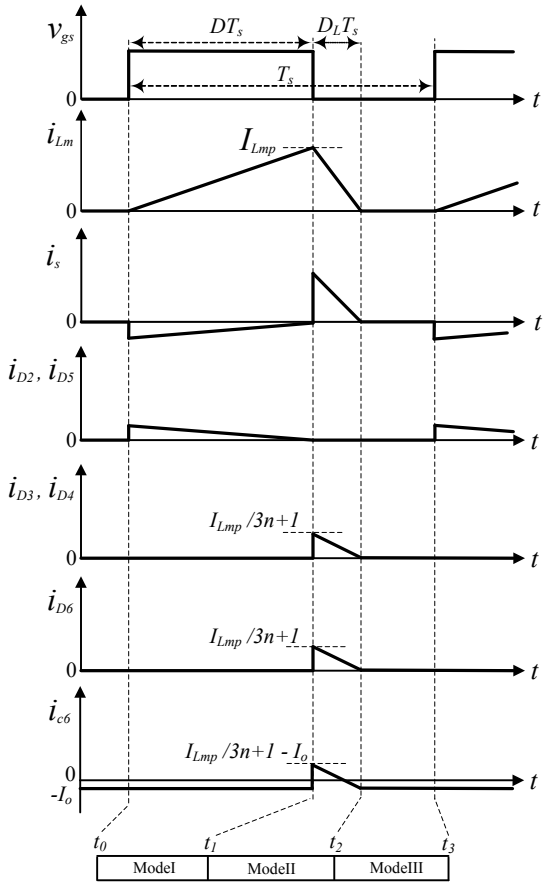
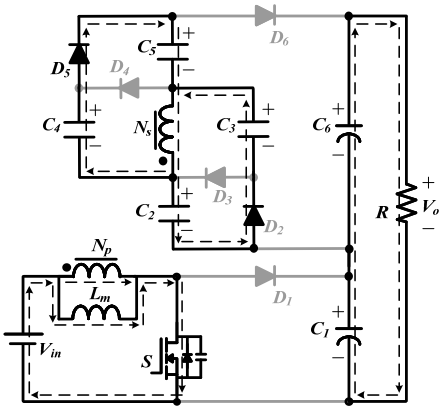
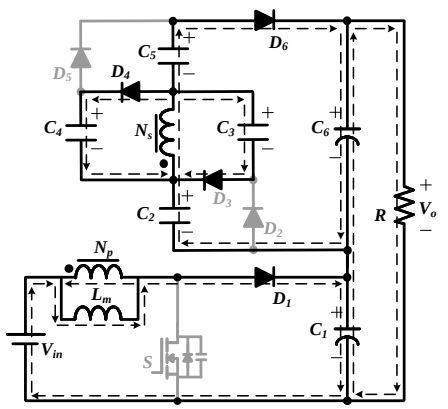


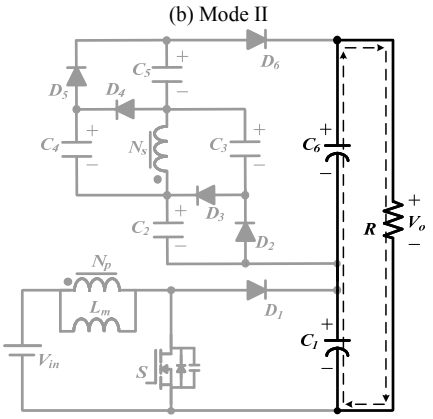
Fig. 4 Some typical waveforms of the proposed converter at DCM operation.



(a) Mode I



(b) Mode II



(c) Mode III

Fig. 5 Current-flow path of operating modes during one switching period at DCM operation. (a) Mode I. (b) Mode II. (c) Mode III.

III. Steady-State Analysis of the Proposed Converter

(A) CCM Operation

At modes IV and V, the energy of the leakage inductor L_k is released to capacitor C_1. According to Ref. [16], the energy released duty cycle D_{c1} can be expressed as

$$D_{c1} = \frac{t_{c1}}{T_s} = \frac{2(1-D)}{n+1}, \tag{1}$$

where t_{c1} is the time interval from modes IV to V which is shown in fig. 2.

Since the time durations of modes I, III, and IV are significantly short, only modes II, V, and VI are considered at CCM operation for the steady-state analysis.

The voltage equation of mode II can be written based on fig. 3(b).

$$v_{Lk}^{II} = (1-k)V_{in}, \tag{2}$$

$$v_{L1}^{II} = \frac{L_m}{L_m + L_k} V_{in} = kV_{in}, \tag{3}$$

$$v_{L2}^{II} = nv_{L1}^{II} = nkV_{in}. \tag{4}$$

Also, the voltage across capacitors C_2 and C_5 can be written as

$$V_{c2} = v_{L2}^{II} + V_{c3}. \tag{5}$$

$$V_{c5} = v_{L2}^{II} + V_{c4}. \tag{6}$$

During the time duration of modes V and VI, the following voltage equations can be derived based on fig. 3(f).

$$v_{L1}^{V} = v_{L1}^{VI} = V_{in} - V_{Lk}^{VI} - V_{c1}. \tag{7}$$

$$v_{L2}^{V} = v_{L2}^{VI} = V_{c3} = V_{c4} = V_{c2} + V_{c5} - V_{c6}. \tag{8}$$

$$v_{L2}^{V} = nv_{L1}^{V}. \tag{9}$$

By applying the volt-second balance principle on N_p and N_s, the following equation is given

$$\int_0^{DT_s} v_{L1}^{II} dt + \int_{DT_s}^{(D+D_{c1})T_s} v_{L1}^{VI} dt = 0. \quad (10)$$

$$\int_0^{DT_s} v_{L2}^{II} dt + \int_{DT_s}^{T_s} v_{L2}^{VI} dt = 0. \quad (11)$$

Substituting (1), (3) and (7) into (10), the voltage of capacitors C_1 is obtained as

$$V_{c1} = (\frac{1}{1-D} + \frac{D(1-k)(n-1)}{2(1-D)})V_{in} = v_{ds}. \quad (12)$$

And substituting (4) and (8) into (11), the voltage across capacitors C_3 and C_4 can expressed as

$$V_{c3} = V_{c4} = \frac{Dnk}{1-D} V_{in}. \quad (13)$$

Substituting (4) and (13) into (5) and (6) the voltage of capacitors C_2 and C_5 are obtained as

$$V_{c2} = V_{c5} = (nk + \frac{Dnk}{1-D})V_{in}. \quad (14)$$

And substituting (4), (8) and (12) into (11), the voltage of capacitor C6 is obtained as

$$V_{c6} = (2nk + \frac{3Dnk}{1-D})V_{in}. \quad (15)$$

Also, the output voltage can be expressed as

$$V_o = V_{c1} + V_{c6} \quad (16)$$

Substituting (12) and (15) into (16), the voltage gain is obtained as

$$M_{CCM} = \frac{V_o}{V_{in}} = \frac{1+2nk}{1-D} + \frac{D[n(k+1)-(1-k)]}{2(1-D)}. \quad (17)$$

The voltage-gain versus the duty-ratio under various coupling-coefficients of the coupled-inductor is shown in fig. 6. It shows that the coupling coefficient results the voltage gain decline. However, voltage gain is less sensitive to the coupling-coefficient. When k = 1, the ideal voltage gain is rewritten as

$$M_{CCM} = \frac{1+2n+nD}{1-D} \quad (18)$$

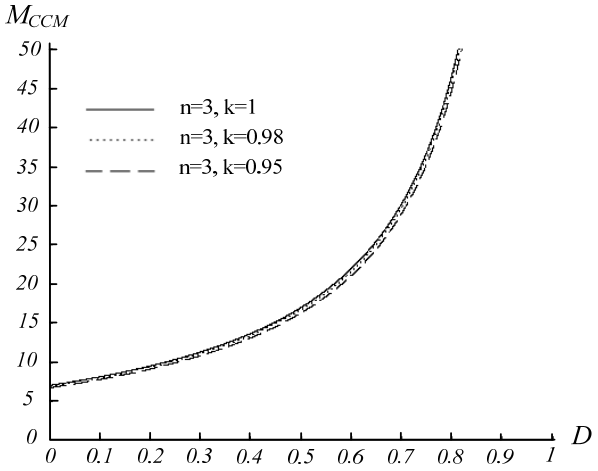


Fig. 6 Voltage-gain versus duty-ratio at CCM operation under n = 3 and various k.

In fig. 7, the curve shows the voltage gain versus the duty ratio of the proposed converter, and other converters in [23] and [24] at CCM operation under k =1 and n =3. As two winding of coupled inductor is used, the voltage gain of proposed converter is higher than other converters in [23] and [24]. The proposed converter can using less turns ratio to achieve the same voltage gain.

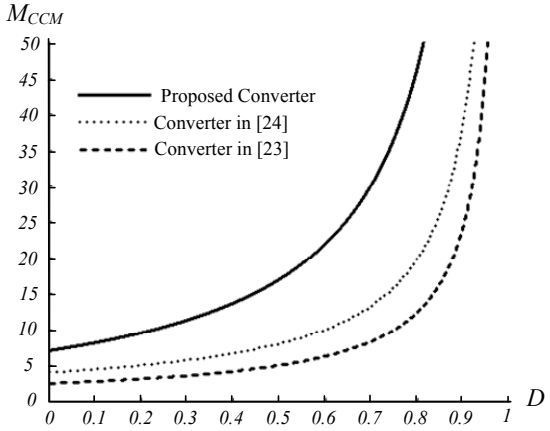


Fig. 7 Voltage-gain versus duty-ratio of the proposed converter, the converters in [23] and [24] at CCM operation under n = 3 and k =1.

According to the analysis of the operating modes, the voltage stresses on main switch S and diodes D_1-D_6 are given as

$$v_{ds} = \frac{1}{1-D} V_{in} = \frac{V_o - nV_{in}}{n+1}, \quad (19)$$

$$V_{D1} = \frac{1}{1-D} V_{in} = \frac{V_o - nV_{in}}{n+1}, \quad (20)$$

$$V_{D2} = V_{D3} = V_{D4} = V_{D5} = V_{D5} = \frac{n}{1-D} V_{in} = \frac{n}{n+1}(V_o - nV_{in}). \quad (21)$$

Equations (19), (20) and (21) mean that under the same voltage gain, the voltage stresses of the proposed converter on main switch and diodes can be adjusted by the turns ratio.

(B) DCM Operation

In DCM operation, the typical waveforms are shown in fig. 4. In the time duration of mode I, switch *S* is turned on. Thus, the following equations can be formulated based on fig. 5(a)

$$v_{L1}^{I} = V_{in}, \tag{22}$$

$$v_{L2}^{I} = nV_{in}. \tag{23}$$

The peak value of the magnetizing-inductor current is given as

$$I_{Lmp} = \frac{V_{in}}{L_m} DT_s. \tag{24}$$

Furthermore, the voltage across capacitors C_2 and C_5 can be written as

$$V_{c2} = v_{L2}^{I} + V_{c3}, \tag{25}$$

$$V_{c5} = v_{L2}^{I} + V_{c4}. \tag{26}$$

In the time interval of mode II, the following equations can be expressed based on fig. 5(b):

$$v_{L1}^{II} = V_{in} - V_{c1}, \tag{27}$$

$$v_{L2}^{II} = V_{c3} = V_{c4} = V_{c2} + V_{c5} - V_{c6}, \tag{28}$$

$$v_{L2}^{II} = nv_{L1}^{II}. \tag{29}$$

During the time interval of mode III, the following equation can be derived from Fig. 5(c).

$$v_{L1}^{III} = v_{L2}^{III} = 0. \tag{30}$$

By applying the voltage-second balance principle on coupled inductor, the following equations are given as

$$\int_0^{DT_s} v_{L1}^{I} dt + \int_{DT_s}^{(D+D_L)T_s} v_{L1}^{II} dt + \int_{(D+D_L)T_s}^{T_s} v_{L1}^{III} dt = 0. \tag{31}$$

$$\int_0^{DT_s} v_{L2}^{I} dt + \int_{DT_s}^{(D+D_L)T_s} v_{L2}^{II} dt + \int_{(D+D_L)T_s}^{T_s} v_{L2}^{III} dt = 0. \tag{32}$$

Substituting (22) and (27) into (31), the voltage is obtained as

$$V_{c1} = (1 + \frac{D}{D_L}) V_{in}, \tag{33}$$

Similarly, substituting (23) and (28) into (32), the voltage across capacitors C_2, C_3, C_4, C_5 and C_6 are derived as

$$V_{c3} = V_{c4} = \frac{nD}{D_L} V_{in}, \tag{34}$$

$$V_{c2} = V_{c5} = (n + \frac{nD}{D_L}) V_{in}, \tag{35}$$

$$V_{c6} = (2n + \frac{3nD}{D_L}) V_{in}, \tag{36}$$

Also, the voltage gain is expressed as

$$V_o = V_{c1} + V_{c6} = \left[\frac{D}{D_L} (3n+1) + (2n+1) \right] V_{in}. \tag{37}$$

According to (37), the duty cycle D_L can be derived as

$$D_L = \frac{(1+3n) D V_{in}}{V_o - (1+2n) V_{in}}. \tag{38}$$

From fig. 4, the average value of i_{c6} is computed as

$$I_{c6} = \frac{1}{2} D_L \frac{I_{Lmp}}{3n+1} - I_o. \tag{39}$$

Since I_{c6} is equal to zero under steady state, equations (24), (38), and I_{c6} = 0 can be substituted to (39). Thus, equations (39) can be rewritten as follows:

$$\frac{D^2 V_{in}^2 T_s}{2\left[V_o - (1+2n) V_{in}\right] L_m} = \frac{V_o}{R}. \tag{40}$$

Then, the normalized magnetizing-inductor time constant is defined as

$$\tau_{Lm} \equiv \frac{L_m}{RT_s} = \frac{L_m f_s}{R}, \tag{41}$$

where f_s is the switching frequency.
Substituting (41) into (40), the voltage gain is given by

$$M_{DCM} = \frac{V_o}{V_{in}} = \frac{1+2n}{2} + \sqrt{\frac{(1+2n)^2}{4} + \frac{D^2}{2\tau_{Lm}}}. \tag{42}$$

The curve of the voltage gain is showed in fig. 8 which illustrates the voltage-gain versus the duty-ratio under various τ_{Lm}.

(C) Boundary Operating Condition between CCM and DCM

If the proposed converter is operated in boundary condition mode, the voltage gain of CCM operation is equal to the voltage gain of DCM operation. The boundary normalized magnetizing-inductor time constant τ_{LmB} can be derived from (18) and (42) as

$$\tau_{LmB} = \frac{D(1-D)^2}{2(1+3n)(1+2n+nD)}. \tag{43}$$

Fig. 9 shows the curve of τ_{LmB}. If τ_{Lm} is larger than τ_{LmB}, the proposed converter is operated in CCM.

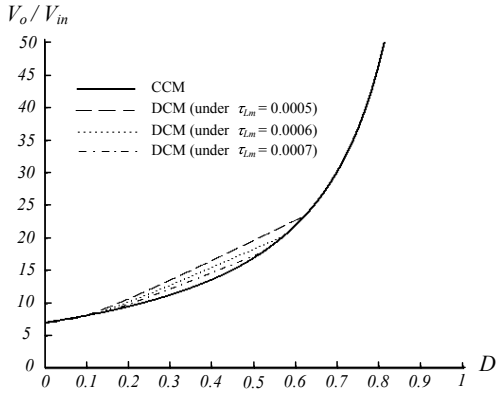


Fig. 8 Voltage-gain versus duty-ratio at DCM operation under various τ_{Lm} and at CCM operation under $n = 3$ and $k = 1$.

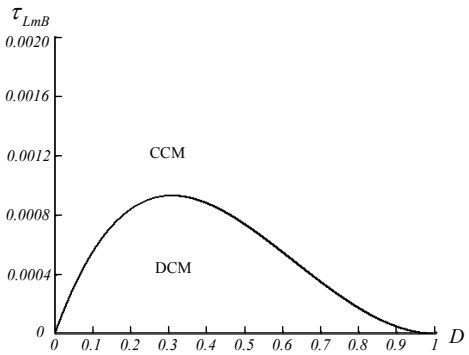


Fig. 9 Boundary condition of the proposed converter under $n = 3$.

IV. Experimental Results of the Proposed Converter

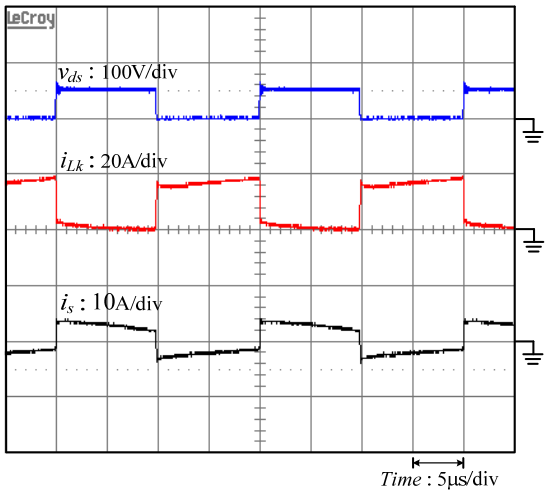
A prototype circuit is implemented in the laboratory to demonstrate the practicability of the proposed converter. The specifications are as follows:

1) input DC voltage V_{in} : 24 V
2) output DC voltage V_o: 400 V
3) maximum output power: 200 W
4) switching frequency: 50 kHz
5) MOSFET S: IRL83036
6) Diodes D_1: MBRF20200CT, $D_2/D_3/D_4/D_5/D_6$: DESP29
7) Coupled inductor: ETD-59, core pc40, $N_p : N_s = 1 : 3$ $L_m = 30$ μH; $L_k = 0.12$ μH
8) Capacitors $C_2/C_3/C_4/C_5$: 22 μF/ 200 V, C_1: 47μF/ 160 V, C_6 : 47 μF/ 400 V

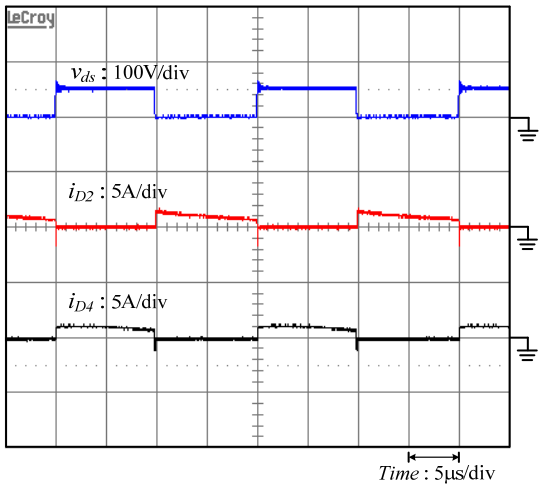
Fig. 10 shows the measured waveforms for full-load P_o = 200 W and V_{in} = 24 V. The proposed converter is operated in CCM under full-load condition. In the measured waveforms, the peak value of V_{ds} is 60.04 V. The duty cycle is 51% and the voltage stress is clamped at appropriately 49 V during the switch-off period. The waveforms demonstrate that the steady-state analysis is corresponded. Therefore, the low-voltage rated switch can be adopted to achieve high efficiency for the proposed converter.

The waveform of secondary-side current i_s in fig. 10(a) shows that the proposed converter is operated in CCM because the current is not equal to zero when the switch is turned on. In fig. 10(b), the waveforms of i_{D2} and i_{D4} show that capacitors C_2 and C_4 are charged in the different time durations. Fig. 10(c) shows that the energy of leakage inductor L_k is released to capacitor C_1 through diode D_1. Fig. 10(d) reveals that V_{c1}, V_{c2} and V_{c4} satisfy equations (33), (34) and (35). In addition, output voltage V_o is consistent with Equation (37). Fig. 10(e) shows the voltage stress of main switch and diodes, and demonstrates the consistency of Equations (19), (20) and (21). Fig. 11 shows the proposed converter under the output power variation between light-load 20 W and full-load 200 W.

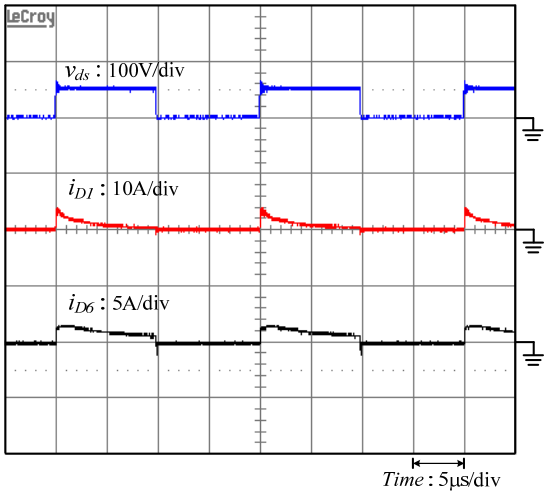
Fig. 12 shows the experimental conversion efficiency of the proposed converter. Maximum efficiency is around 95.31% at P_o= 80 W and V_{in} = 24 V. The full-load efficiency is appropriately 94.06 % at P_o= 200 W, V_{in} = 24 V, and V_{out} = 400 V. Compared to other converter, the efficiency is improved about 2%.



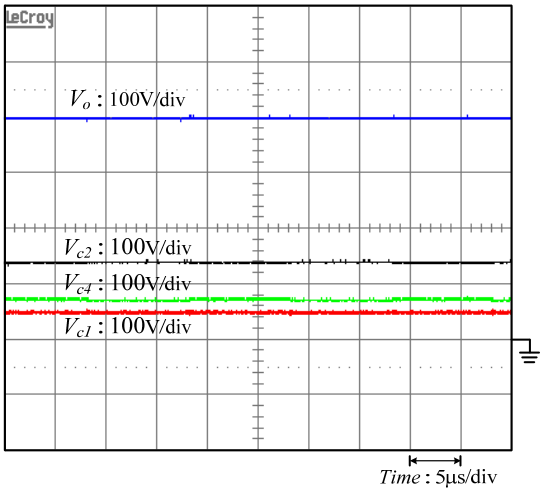
(a)



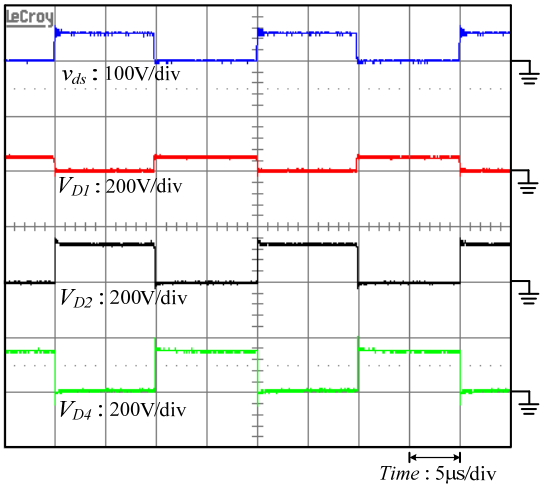
(b)



(c)



(d)



(e)

Fig. 10 Experiment results under full-load P_o = 200 W.

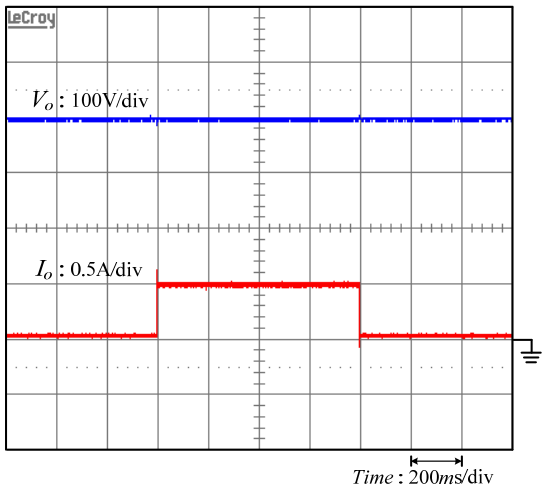


Fig. 11 Load variation between light-load P_o = 20 W and full-load P_o = 200 W.

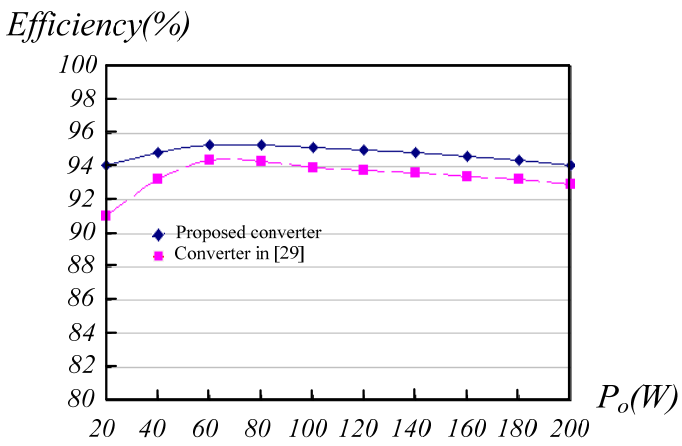


Fig. 12 Experimental conversion efficiency.

V. Conclusions

This paper has proposed a novel, high efficiency, and high step-up DC-DC converter with the coupled inductor and switched capacitors techniques. The proposed converter adds passive components without extra winding stage, and uses capacitors charged in parallel and discharged in series with a coupled-inductor to achieve high step-up voltage gain. The steady-state analyses of voltage gain and boundary operating condition are discussed. Finally, a prototype circuit of the proposed converter is implemented in the laboratory. Experimental results verify that high efficiency and high step-up voltage gain can be achieved. The efficiency is 95.31%. The voltage stress on the main switches is 60 V, thus low voltage ratings and low on-state resistance levels $R_{DS(ON)}$ switch can be selected.

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