Novel High Step-Up DC-DC Converter with Coupled-Inductor and Voltage-Doubler Circuits

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Abstract

In this paper, a novel high step-up DC-DC converter with coupled-inductor and voltage-doubler circuits is proposed. The converter achieves high step-up voltage gain with appropriate duty ratio and low voltage stress on the power switches. Also, the energy stored in the leakage inductor of the coupled inductor can be recycled to the output. The operating principles and the steady-state analyses of the proposed converter are discussed in detail. Finally, a prototype circuit of the proposed converter is implemented in the laboratory to verify the performance of the proposed converter.

***Index Terms* – Coupled-inductor, voltage-doubler, high step-up voltage gain.**

I. INTRODUCTION

The DC-DC converter with high step-up voltage gain is widely used for many applications, such as fuel-cell energy-conversion systems, solar-cell energy-conversion systems, and high-intensity-discharge lamp ballasts for automobile headlamps. Conventionally, the DC-DC boost converter is used for voltage step-up applications, and in

this case this converter will be operated at extremely high duty ratio to achieve high step-up voltage gain [1], [2]. However, the voltage gain and the efficiency are limited due to the constraining effect of power switches, diodes, and the equivalent series resistance (ESR) of inductors and capacitors. Moreover, the extremely high duty-ratio operation will result in a serious reverse-recovery problem. Some literatures have researched the high step-up DC-DC converters that do not incur an extremely high duty ratio [3]-[25]. The transformerless DC-DC converters, such as the cascade boost type [3], the quadratic boost type [4], the switched-inductor type [5], [6], the voltage-lift type [7], [8], the voltage doubler technique [9]-[11], the capacitor-diode voltage multiplier type [12], and the boost type that is integrated using a switched-capacitor technique [13]. These converters can provide higher voltage gain than the conventional DC-DC boost converter. However, the voltage gain of these converters is only moderately high. If higher voltage gain is required, these converters must cascade more power stages, which will result in low efficiency. The DC-DC flyback converter is adopted to achieve high step-up voltage gain by adjusting the turns ratio of the transformer. This converter has the merits of simple topology, easy control, and low cost, but the fact that the leakage-inductor energy of the transformer can not be recycled, it results in low efficiency and high voltage stress on the active switch. In order to reduce the voltage stress, an RCD snubber is used [14]. However, this decreases the efficiency. Some active-clamp techniques are adopted to recycle the leakage-inductor energy of the transformer and to minimize the

voltage stress on the active switch, but this approach requires an additional switch [15]-[17]. Some converters, which include the clamp-mode boost type, the integrated boost-flyback type, and the integrated boost-sepic type, are developed to achieve high step-up voltage gain by using the coupled-inductor technique [18]-[22]. The leakage-inductor energy of the coupled inductor can be recycled and the voltage stress on the active switch is reduced. Much higher voltage gain is achieved by using the coupled inductor and the voltage-multiplier or voltage-lift techniques [23]-[25]. However, the active switch will suffer high current stress during the switch-on period.

A conventional high step-up DC-DC converter with coupled-inductor technique is shown in Fig. 1 [21]. The structure of this converter is very simple and the leakage-inductor energy of the coupled inductor can be recycled to the output. However, the voltage stresses on switch S_1 and diode D_1, which are equal to the output voltage, are high. This paper presents a novel high step-up DC-DC converter, as shown in Fig. 2. The coupled-inductor and voltage-doubler techniques are integrated in the proposed converter to achieve high step-up voltage gain. The features of this converter are as follows: 1) The leakage-inductor energy of the coupled inductor can be recycled. 2) The voltage stresses on the switches are half the level of the output voltage. Thus, the switches with low voltage rating and low ON-state resistance $R_{DS(ON)}$ can be selected. 3) The voltage gain achieved by the proposed converter is double that of the conventional high step-up converter. Under the same voltage gain and duty ratio, the

turns ratio of the coupled inductor for the proposed converter can be designed to be less than the conventional high step-up converter. 4) The frequency of the magnetizing-inductor current for the proposed converter is double of the switching frequency. Thus, the magnetizing-inductance of the coupled-inductor for the proposed converter can be designed to be less than the conventional high step-up converter under same switching frequency.

II. Operating Principle of the Proposed Converter

Fig. 2 shows the circuit configuration of the proposed converter, which consists of two active switches S_1 and S_2, one coupled inductor, four diodes $D_1 - D_4$, and two output capacitors C_1 and C_2. The simplified circuit model of the proposed converter is shown in Fig. 3. The coupled inductor is modeled as a magnetizing inductor L_m, primary leakage inductor L_{k1}, secondary leakage inductor L_{k2}, and an ideal transformer. Capacitors C_{S1} and C_{S2} are the parasitic capacitor of S_1 and S_2. In order to simplify the circuit analysis of the proposed converter, some conditions are assumed as follows: 1) All components are ideal. ON-state resistance $R_{DS(ON)}$ of the active switches, the forward voltage drop of the diodes, and the ESR of the coupled-inductor and output capacitors are ignored. 2) Output capacitors C_1 and C_2 are sufficiently large, and the voltages across C_1 and C_2 are considered to be constant during one switching period.

Fig. 4 shows some typical waveforms during one switching period in continuous conduction mode (CCM) operation. The operating principle is described as follows.

1) Mode I [t_0, t_1]: At $t = t_0$, S_1 and S_2 are turned on. The current-flow path is shown in Fig. 5(a). The DC-source energy is transferred to L_m and L_{k1} through D_3, S_1, and S_2, so currents i_{Lm}, i_{Lk1}, and i_{D3} are increased. The energy stored in L_{k2} is released to L_m and L_{k1} through D_4, S_1, and S_2. Thus, i_{Lk2} is decreased. Meanwhile, the energy stored in L_{k2} is recycled. The energy stored in C_{S2} is rapidly and completely discharged. The energies stored in C_1 and C_2 are discharged to the load. This mode ends when i_{Lk2} is equal to zero at $t = t_1$.

2) Mode II [t_1, t_2]: In this mode, S_1 and S_2 are still turned on. The current-flow path is shown in Fig. 5(b). The DC-source energy is still transferred to L_m and L_{k1}. Thus, i_{Lm} and i_{Lk1} are still increased. The energies stored in C_1 and C_2 are still discharged to the load.

3) Mode III [t_2, t_3]: At $t = t_2$, S_1 is turned off and S_2 is still turned on. The current-flow path is shown in Fig. 5(c). The DC-source energy is still transferred to L_m, L_{k1}, and C_{S1}. Meanwhile, the voltage across S_1 is increased rapidly. The energies stored in C_1 and C_2 are still discharged to the load.

4) Mode IV [t_3, t_4]: During this time interval, S_1 is still turned off and S_2 is still turned on. The current-flow path is shown in Fig. 5(d). The DC source, L_m, and L_{k1} are series-connected to transfer their energies to L_{k2}, C_1, and the load. Thus, i_{Lm} and i_{Lk1} are decreased and i_{Lk2} is increased. Meanwhile, the energy stored in L_{k1} is recycled to C_1 and the load. The energy stored in C_2 is still discharged to the load. This mode ends when i_{Lk1}

is equal to i_{Lk2} at $t = t_4$.

5) Mode V [t_4, t_5]: During this period, S_1 is still turned off and S_2 is still turned on. The current-flow path is shown in Fig. 5(e). The DC source, L_m, L_{k1}, and L_{k2} are series-connected to transfer their energies to C_1 and the load. Thus, i_{Lm}, i_{Lk1}, and i_{Lk2} are decreased. The energy stored in C_2 is still discharged to the load.

6) Mode VI [t_5, t_6]: At $t = t_5$, S_1 and S_2 are turned on. The current-flow path is shown in Fig. 5(f). The DC-source energy is transferred to L_m and L_{k1} through D_3, S_1, and S_2. So currents i_{Lm}, i_{Lk1}, and i_{D3} are increased. The energy stored in L_{k2} is released to L_m and L_{k1} through D_4, S_1, and S_2. Thus, i_{Lk2} is decreased. Meanwhile, the energy stored in L_{k2} is recycled. The energy stored in C_{S1} is rapidly and completely discharged. The energies stored in C_1 and C_2 are discharged to the load. This mode ends when i_{Lk2} is equal to zero at $t = t_6$.

7) Mode VII [t_6, t_7]: During this time interval, S_1 and S_2 are still turned on. The current-flow path is shown in Fig. 5(g). The DC-source energy is still transferred to L_m and L_{k1}. Thus, i_{Lm} and i_{Lk1} are still increased. The energies stored in C_1 and C_2 are still discharged to the load.

8) Mode VIII [t_7, t_8]: At $t = t_7$, S_1 is still turned on and S_2 is turned off. The current-flow path is shown in Fig. 5(h). The DC-source is still transferred to L_m, L_{k1}, and C_{S2}. Meanwhile, the voltage across S_2 is increased rapidly. The energies stored in C_1 and C_2 are still

discharged to the load.

9) Mode IX [t_8, t_9]: During this period, S_1 is still turned on and S_2 is still turned off. The current-flow path is shown in Fig. 5(i). The DC source, L_m, and L_{k1} are series-connected to transfer their energies to L_{k2}, C_2, and the load. Thus, i_{Lm} and i_{Lk1} are decreased and i_{Lk2} is increased. Meanwhile, the energy stored in L_{k1} is recycled to C_2 and the load. The energy stored in C_1 is still discharged to the load. This mode ends when i_{Lk1} is equal to i_{Lk2} at $t = t_9$.

10) Mode X [t_9, t_{10}]: In this mode, S_1 is still turned on and S_2 is still turned off. The current-flow path is shown in Fig. 5(j). The DC source, L_m, L_{k1}, and L_{k2} are series-connected to transfer their energies to C_2 and the load. Thus, i_{Lm}, i_{Lk1}, and i_{Lk2} are decreased. The energy stored in C_1 is still discharged to the load. This mode ends when S_1 and S_2 are turned on at the beginning of the next switching period.

III. Steady-State Analysis of the Proposed Converter

(A) Voltage gain

At CCM operation, the time durations of modes I, III, IV, VI, VIII, and IX are very short as compared to one switching period. Thus, only modes II, V, VII, and X are considered. At modes II and VII, the following equations can be written from Figs. 5(b) and 5(g):

$$v_{L1}^{II} = v_{L1}^{VII} = kV_{in}, \tag{1}$$

$$\frac{di_{Lm}^{II}}{dt} = \frac{di_{Lm}^{VII}}{dt} = \frac{kV_{in}}{L_m}, \tag{2}$$

where coupling-coefficient k of the coupled-inductor is equal to $L_m/(L_m+L_{k1})$.

At mode V, the following equations are derived from Fig. 5(e):

$$i_{Lk1}^{V} = i_{Lk2}^{V}, \tag{3}$$

$$i_{Lm}^{V} = (1+n)i_{Lk1}^{V}, \tag{4}$$

$$V_{in} - V_{c1} = v_{L1}^{V} + v_{Lk1}^{V} + v_{L2}^{V} + v_{Lk2}^{V}, \tag{5}$$

where turns ratio n of the coupled-inductor is equal to N_2/N_1. Voltage v_{Lk2}^{V} is found to be

$$v_{Lk2}^{V} = L_{k2}\frac{di_{Lk2}^{V}}{dt} = L_{k2}\frac{di_{Lk1}^{V}}{dt} = n^2 L_{k1}\frac{di_{Lk1}^{V}}{dt} = n^2 v_{Lk1}^{V}. \tag{6}$$

Substituting (6) into (5) yields the following equation:

$$V_{in} - V_{c1} = (1+n)v_{L1}^{V} + (1+n^2)v_{Lk1}^{V}. \tag{7}$$

Voltage v_{L1}^{V} is written as

$$v_{L1}^{V} = L_m\frac{di_{Lm}^{V}}{dt} = (1+n)L_m\frac{di_{Lk1}^{V}}{dt}. \tag{8}$$

Thus,

$$v_{Lk1}^{V} = L_{k1}\frac{di_{Lk1}^{V}}{dt} = \frac{L_{k1}}{(1+n)L_m}v_{L1}^{V} = \frac{1-k}{(1+n)k}v_{L1}^{V}. \tag{9}$$

Substituting (9) into (7) yields the following equation:

$$v_{L1}^{V} = \frac{(1+n)k}{1+2nk+n^2}(V_{in} - V_{c1}), \tag{10}$$

$$\frac{di_{Lm}^{V}}{dt} = \frac{(1+n)k}{1+2nk+n^2} \times \frac{V_{in} - V_{c1}}{L_m}. \tag{11}$$

Similarly, at mode X, the voltage across L_m is derived from Fig. 5(j) as follows:

$$v_{L1}^{X} = \frac{(1+n)k}{1+2nk+n^2}(V_{in} - V_{c2}), \tag{12}$$

$$\frac{di_{Lm}^{X}}{dt} = \frac{(1+n)k}{1+2nk+n^2} \times \frac{V_{in} - V_{c2}}{L_m}. \tag{13}$$

Using the volt-second balance principle on L_m, the following equation is derived as

$$\int_0^{\frac{DT_s}{2}} v_{L1}^{II} dt + \int_0^{\frac{(1-D)T_s}{2}} v_{L1}^{V} dt + \int_0^{\frac{DT_s}{2}} v_{L1}^{VII} dt + \int_0^{\frac{(1-D)T_s}{2}} v_{L1}^{X} dt = 0. \tag{14}$$

Substituting (1), (10), and (12) into (14), the voltage gain is obtained as

$$M_{CCM} = \frac{V_o}{V_{in}} = \frac{2(1+n-nD+n^2D+2nDk)}{(1-D)(1+n)}. \tag{15}$$

Thus, the drawing of the voltage gain versus the duty ratio under various coupling coefficients of the coupled-inductor is shown in Fig. 6. It can be seen that the voltage gain is not very sensitive to the coupling coefficient. If the impact of the leakage inductor of the coupled inductor is neglected, then coupling coefficient k is equal to 1. Substituting $k = 1$ into (15), the voltage gain becomes

$$M_{CCM} = \frac{V_o}{V_{in}} = \frac{2(1+nD)}{1-D}. \tag{16}$$

(B) Boundary Operating Condition

Fig. 7 shows some waveforms of the proposed converter at boundary conduction mode (BCM). When the proposed converter is operated in BCM, the peak value of the magnetizing-inductor current is given as

$$I_{Lmp} = \frac{kDV_{in}T_s}{2L_m}. \tag{17}$$

Since the time duration [t_1, t_3] is very short as compared to one switching period, this time duration is not considered. The average value of i_{D1} is found to be

$$I_{D1} = \frac{\frac{1}{2} \times \frac{I_{Lmp}}{1+n} \times \frac{1-D}{2} T_s}{T_s} = \frac{(1-D) I_{Lmp}}{4(1+n)}. \tag{18}$$

At steady state, the average value of i_{D1} is equal to I_o. Thus,

$$\frac{(1-D) I_{Lmp}}{4(1+n)} = I_o = \frac{V_o}{R}. \tag{19}$$

Then, the normalized magnetizing-inductor time constant is defined as

$$\tau_{Lm} \equiv \frac{L_m}{R T_s} = \frac{L_m f_s}{R}, \tag{20}$$

where f_s is the switching frequency.

Substituting (15), (17), and (20) into (19), the boundary normalized magnetizing-inductor time constant τ_{LmB} can be derived as

$$\tau_{LmB} = \frac{kD(1-D)^2}{16(1+n-nD+n^2D+2nDk)}. \tag{21}$$

The curve of τ_{LmB} is plotted in Fig. 8. If τ_{Lm} is larger than τ_{LmB}, the proposed converter is operated in CCM.

(C) Efficiency Analysis

In order to simplify the efficiency analysis of the proposed converter, the leakage inductors of the coupled inductor are neglected. Thus, the operating principle is divided into four modes, the equivalent circuits for which are shown in Fig. 9. r_{L1} and r_{L2} represent the

ESR of the primary and secondary windings of the coupled inductor. V_{FD1}-V_{FD4} and r_{D1}-r_{D4} are the ON-state forward voltage drop and resistance of D_1-D_4. r_{S1} and r_{S2} denote the ON-state resistance of S_1 and S_2.

When S_1 and S_2 are turned on, the equivalent circuit is shown in Fig. 9(a). This time interval is $DT_s/2$. The average values of i_{c1} and v_{L1} are obtained as

$$I_{c1}^{I} = I_{c1}^{III} = -\frac{V_o}{R}, \tag{22}$$

$$V_{L1}^{I} = V_{L1}^{III} = V_{in} - V_{FD3} - I_{in(on)}(r_{L1} + r_{D3} + r_{S1} + r_{S2}), \tag{23}$$

where $I_{in(on)}$ is the average value of the input current in this time interval.

When S_1 is turned off and S_2 is turned on, the equivalent circuit is shown in Fig. 9(b). This time interval is $(1\text{-}D)T_s/2$. The average values of i_{c1} and v_{L1} are derived as

$$I_{c1}^{II} = I_{in(off)} - \frac{V_o}{R}, \tag{24}$$

$$V_{L1}^{II} = \frac{V_{in} - V_{FD4} - V_{FD1} - V_{c1} - I_{in(off)}(r_{L1} + r_{D4} + r_{L2} + r_{D1} + r_{S2})}{1+n}, \tag{25}$$

where $I_{in(off)}$ the average value of the input current in this time interval.

When S_1 is turned on and S_2 is turned off, the equivalent circuit is shown in Fig. 9(c). This time interval is $(1\text{-}D)T_s/2$. The average values of i_{c1} and v_{L1} are given as

$$I_{c1}^{IV} = -\frac{V_o}{R}, \tag{26}$$

$$V_{L1}^{IV} = \frac{V_{in} - V_{FD4} - V_{c2} - V_{FD2} - I_{in(off)}(r_{L1} + r_{D4} + r_{L2} + r_{S1} + r_{D2})}{1+n}. \tag{27}$$

By using the ampere-second balance principle on C_1, the following equations are obtained as

$$\int_0^{\frac{DT_s}{2}} I_{c1}^{I} dt + \int_0^{\frac{(1-D)T_s}{2}} I_{c1}^{II} dt + \int_0^{\frac{DT_s}{2}} I_{c1}^{III} dt + \int_0^{\frac{(1-D)T_s}{2}} I_{c1}^{IV} dt = 0. \tag{28}$$

Substituting (22), (24), and (26) into (28), $I_{in(off)}$ can be computed as

$$I_{in(off)} = \frac{2V_o}{(1-D)R}. \tag{29}$$

Also, $I_{in(on)}$ can be found to be

$$I_{in(on)} = (1+n)I_{in(off)} = \frac{2(1+n)V_o}{(1-D)R}. \tag{30}$$

Using the volt-second balance principle on L_m yields

$$\int_0^{\frac{DT_s}{2}} V_{L1}^{I} dt + \int_0^{\frac{(1-D)T_s}{2}} V_{L1}^{II} dt + \int_0^{\frac{DT_s}{2}} V_{L1}^{III} dt + \int_0^{\frac{(1-D)T_s}{2}} V_{L1}^{IV} dt = 0. \tag{31}$$

Substituting (23), (25), and (27) into (31), the actual voltage gain is derived as

$$\frac{V_o}{V_{in}} = \frac{2(1+nD)}{1-D} \times \frac{1-A_1}{1+\frac{4D(1+n)^2 A_2}{(1-D)^2 R} + \frac{2A_3}{(1-D)R}}, \tag{32}$$

where

$$A_1 = \frac{1-D}{2(1+nD)}\left(\frac{V_{FD1}}{V_{in}} + \frac{V_{FD2}}{V_{in}}\right) + \frac{(1+n)D}{1+nD} \times \frac{V_{FD3}}{V_{in}} + \frac{1-D}{1+nD} \times \frac{V_{FD4}}{V_{in}},$$

$$A_2 = r_{L1} + r_{D3} + r_{S1} + r_{S2},$$

$$A_3 = 2r_{L1} + 2r_{L2} + r_{D1} + r_{D2} + 2r_{D4} + r_{S1} + r_{S2}.$$

The input power and output power of the proposed converter are obtained as

$$P_{in} = V_{in} I_{in(on)}\left(\frac{D}{2} + \frac{D}{2}\right) + V_{in} I_{in(off)}\left(\frac{1-D}{2} + \frac{1-D}{2}\right), \tag{33}$$

$$P_o = \frac{V_o^2}{R}. \tag{34}$$

Substituting (29) and (30) into (33), the input power can be computed as

$$P_{in} = \frac{2(1+nD)}{(1-D)R} V_{in} V_o. \tag{35}$$

From (32), (34) and (35), the efficiency of the proposed converter is found to be

$$\eta = \frac{P_o}{P_{in}} = \frac{1-A_1}{1+\frac{4D(1+n)^2 A_2}{(1-D)^2 R}+\frac{2A_3}{(1-D)R}}. \tag{36}$$

(D) Voltage and Current Stresses on Power Devices

According to the operating principle, the voltage and current stresses on power devices are discussed as follows. If the impact of the leakage inductor of the coupled inductor is ignored, the voltage stresses on S_1, S_2, and $D_1 - D_4$ are given as

$$V_{S1} = V_{S2} = V_{D1} = V_{D2} = \frac{V_o}{2}, \tag{37}$$

$$V_{D3} = \frac{n}{1+n}\left(\frac{V_o}{2} - V_{in}\right), \tag{38}$$

$$V_{D4} = nV_{in}. \tag{39}$$

From (2), the ripple of i_{Lm} can be derived as

$$\Delta I_{Lm} = \frac{kDV_{in}T_s}{2L_m}. \tag{40}$$

From (29), (30), and (40), the current stresses flow through S_1, S_2, and $D_1 - D_4$ are found to be

$$I_{S1} = I_{S2} = I_{D1} = I_{D2} = I_{D3} = I_{in(on)} + \frac{\Delta I_{Lm}}{2} = \frac{2(1+n)V_o}{(1-D)R} + \frac{kDV_{in}T_s}{4L_m}. \tag{41}$$

$$I_{D4} = I_{in(off)} + \frac{\Delta I_{Lm}}{2(1+n)} = \frac{2V_o}{(1-D)R} + \frac{kDV_{in}T_s}{4(1+n)L_m}. \tag{42}$$

IV. Experimental Results

In order to verify the feasibility of the proposed converter, a 250-W prototype circuit is built in the laboratory. The circuit specifications and components are selected as V_{in} = 24 V, V_o = 200 V, f_s = 25 kHz, P_o = 250 W (R = 160 Ω), and C_1 = C_2 = 47 μF. Also, MOSFET IXFK140N20P (V_{DSS} = 200 V, $R_{DS(ON)}$ = 18 mΩ) is selected for S_1 and S_2, and diode MBR20150CT (V_{RRM} = 150 V, V_F = 0.92 V) is selected for D_1 and D_2. Substituting V_{in} = 24 V and V_o = 200 V into (38) and (39), the voltage stresses on D_3 and D_4 versus turns ratio n of the coupled inductor are plotted in Fig. 10. One can see that V_{D3} and V_{D4} are increased with an increase in n. For the voltage-gain and efficiency analysis, the ESR of the coupled inductor, the ON-state forward voltage drop and resistance of D_1-D_4, and the ON-state resistance of S_1 and S_2 are considered. Some parameters of three cases are assumed as follows:

1) Case 1: n = 1, r_{L1} = r_{L2} = r_{D1} = r_{D2} = r_{D3} = r_{D4} = 10 mΩ, r_{S1} = r_{S2} = 18 mΩ, V_{FD1} = V_{FD2} = 0.92 V, and V_{FD3} = V_{FD4} = 0.75 V.

2) Case 2: n = 2, r_{L1} = r_{D1} = r_{D2} = r_{D3} = r_{D4} = 10 mΩ, r_{L2} = 20 mΩ, r_{S1} = r_{S2} = 18 mΩ, V_{FD1} = V_{FD2} = 0.92 V, and V_{FD3} = V_{FD4} = 0.85 V.

3) Case 3: n = 3, r_{L1} = r_{D1} = r_{D2} = r_{D3} = r_{D4} = 10 mΩ, r_{L2} = 30 mΩ, r_{S1} = r_{S2} = 18 mΩ, V_{FD1} = V_{FD2} = 0.92 V, and V_{FD3} = V_{FD4} = 0.85 V.

Substituting the circuit specifications and parameters into (32) and (36), the calculated voltage gain and efficiency are plotted in Figs. 11 and 12. Fig. 12 shows that the calculated efficiency

in case 1 is better than in cases 2 and 3. Thus, turns ratio n of the coupled inductor is chosen as 1. Then, diode SBL2060CT (V_{RRM} = 60 V, V_F = 0.75 V) is selected for D_3 and D_4.

As can be seen from Fig. 11, duty ratio D is 0.634 for case 1. Substituting k = 1, n = 1, and D = 0.634 into (21), the boundary normalized magnetizing-inductor time constant τ_{LmB} is obtained as 0.00162. The proposed converter is operated in CCM from 25% of the full load, namely R = 640 Ω. When τ_{Lm} is larger than τ_{LmB}, the proposed converter is operated in CCM. Using (20), L_m is found by

$$\tau_{Lm} = \frac{L_m f_s}{R} = \frac{L_m \times 25\text{k}}{640} > 0.00162,$$

$$L_m > 41\ \mu\text{H},$$

L_m is selected to be 48 μH.

The circuit diagram of the proposed converter with control circuit is shown in Fig. 13. Under the operating conditions V_{in} = 24 V, V_o = 200 V, and P_o = 250 W, some experimental waveforms are shown in Figs. 14-16. Fig. 14 shows some experimental voltage waveforms. It is seen that v_{s1}, v_{s2}, v_{D1} and v_{D2} are equal to half of the output voltage during the steady-state period. However, the ringing phenomenon of v_{s1} and v_{s2} is caused by the line inductors and parasitic capacitors of S_1 and S_2 when S_1 and S_2 are turned off. Thus, the ringing phenomenon must be taken into consideration for choosing S_1 and S_2. Fig. 15 shows some experimental current waveforms, which agree with the operating principle and the steady-state analysis. However, the ringing phenomenon exists in i_{D4}. One must consider this phenomenon for

choosing D_4. As shown in Fig. 16, the voltages across C_1 and C_2 are equal, and they are also equal to half of the output voltage. Fig. 17 shows the measured efficiency of the proposed converter and the conventional converter in [21]. The circuit components of the conventional converter are chosen as the turns ratio n of the coupled inductor: 3.6, switch S_1: FDA59N30 (V_{DSS} = 300 V, $R_{DS(ON)}$ = 56 mΩ), diode D_1: DSEP30-03A (V_{RRM} = 300 V, V_F = 1.55 V), and D_2: DSEP30-06A (V_{RRM} = 600 V, V_F = 1.6 V). The $R_{DS(ON)}$ of the switch and V_F of diodes in the proposed converter are less than the conventional converter. When the output power is over 70 W, the proposed converter has higher efficiency than this conventional converter. Also, the measured efficiency of the proposed converter is 91.1% at the full-load condition and the maximum efficiency is 92.8% at the half-load condition.

V. CONCLUSIONS

A novel high step-up DC-DC converter is presented in this paper. The coupled-inductor and voltage-doubler circuits are integrated in the proposed converter to achieve high step-up voltage gain. The energy stored in the leakage inductor of the coupled inductor can be recycled. The voltages across the switches are half the level of the output voltage during the steady-state period. However, the voltages have the ringing phenomenon at the beginning when the switches are turned off. One must consider this phenomenon for choosing the switches. Similarly, since the ringing phenomenon is occurred in the current through diode D_4, this phenomenon is also considered for choosing diode D_4. Finally, a prototype circuit for the

proposed converter with 24-V input voltage, 200-V output voltage, and 250-W output power is built in the laboratory to verify the feasibility. The experimental results show that high step-up voltage gain is achieved. The measured efficiency is 91.1% at the full-load condition and the maximum efficiency is 92.8% at the half-load condition. Comparing to the proposed converter and the conventional converter in [21], one can see that the efficiency is improved. However, since more circuit components are used in the proposed converter, it results in higher cost.

ACKNOWLEDGMENTS

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Figure Captions

Fig. 1. Circuit configuration of the conventional high step-up DC-DC converter.

Fig. 2. Circuit configuration of the proposed converter.

Fig. 3. Simplified circuit model of the proposed converter.

Fig. 4. Some typical waveforms of the proposed converter at CCM operation.

Fig. 5. Current-flow path of operating modes during one switching period at CCM operation.

Fig. 6. Voltage gain versus duty ratio of the proposed converter at CCM operation with $n = 2$ and various values for k.

Fig. 7. Some typical waveforms of the proposed converter at BCM operation.

Fig. 8. Boundary condition of the proposed converter with $n = 2$ and $k = 1$.

Fig. 9. Equivalent circuit of the proposed converter, including ESR of the coupled inductor, the ON-state forward voltage drop and resistance of the diodes, and the ON-state resistance of the switches. (a) S_1 and S_2 ON. (b) S_1 OFF and S_2 ON. (c) S_1 ON and S_2 OFF.

Fig. 10. Voltage stresses on D_3 and D_4 versus the turns ratio of the coupled inductor.

Fig. 11. Calculated voltage gain versus duty ratio.

Fig. 12. Calculated efficiency versus output power.

Fig. 13. Circuit diagram of the proposed converter with control circuit.

Fig. 14. Experimental waveforms. (a) v_{gs1}, v_{gs2}, v_{S1}, and v_{S2}. (b) v_{D1}, v_{D2}, v_{D3}, and v_{D4}.

Fig. 15. Experimental waveforms. (a) i_{D4}, i_{in}, and i_{D3}. (d) i_{S1} and i_{D1}.

Fig. 16. Experimental waveforms for V_{c1}, V_{c2}, and V_o.

Fig. 17. Measured efficiency of the proposed converter and the conventional converter in [21] with various output power.

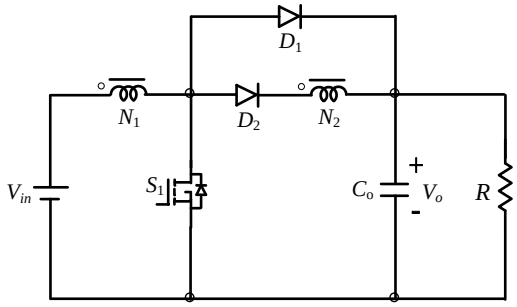


Fig. 1. Circuit configuration of the conventional high step-up DC-DC converter.

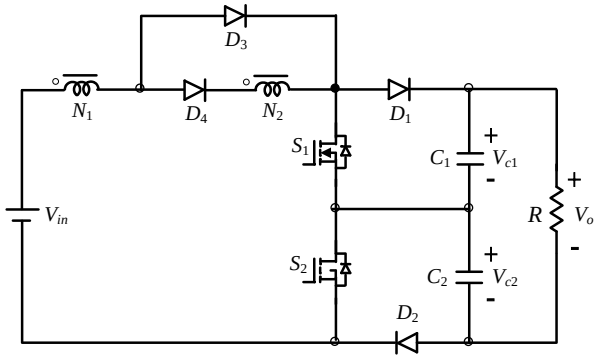


Fig. 2. Circuit configuration of the proposed converter.

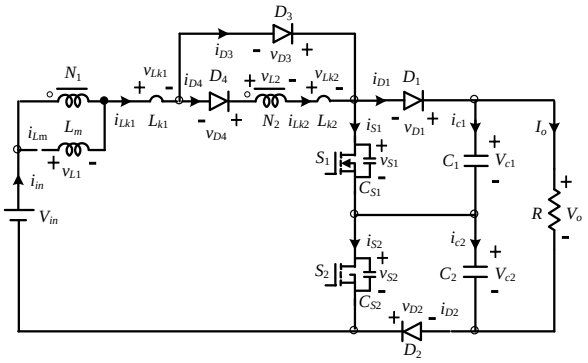


Fig. 3. Simplified circuit model of the proposed converter.

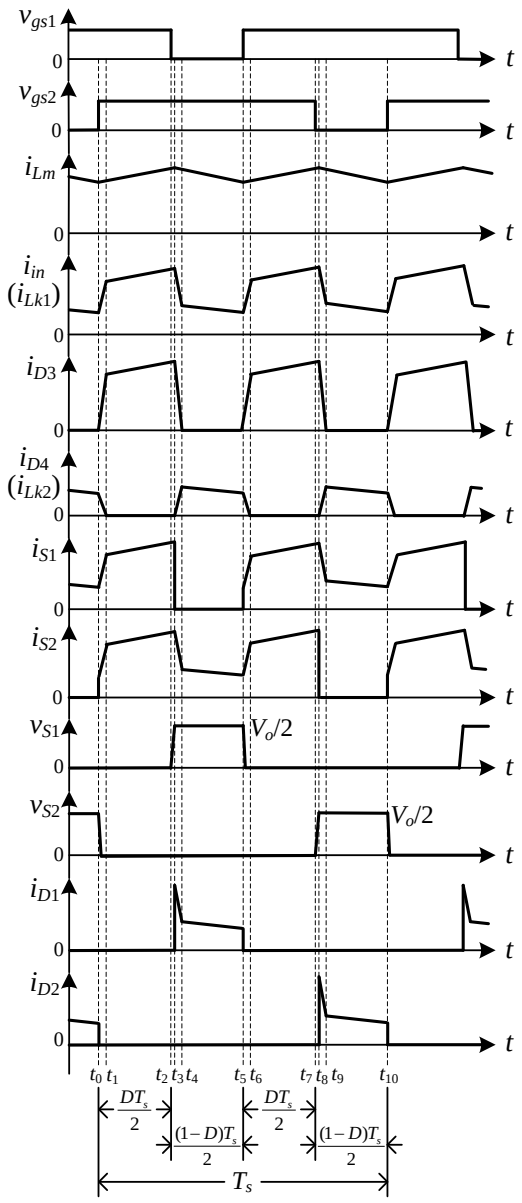
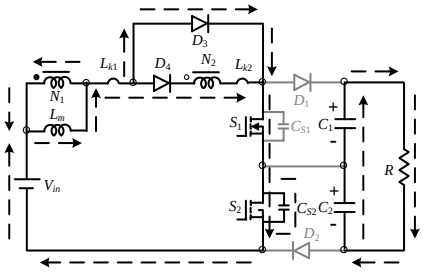
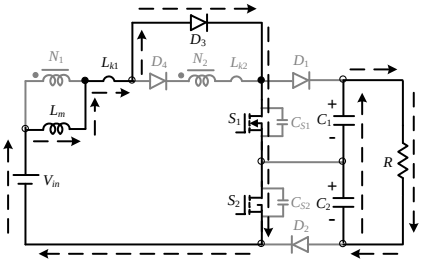


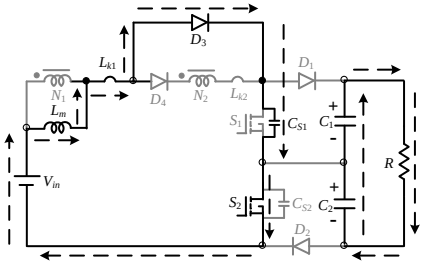
Fig. 4. Some typical waveforms of the proposed converter at CCM operation.



(a) Mode I



(b) Mode II



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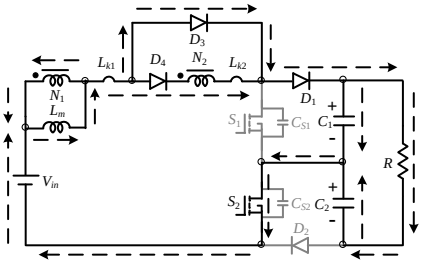
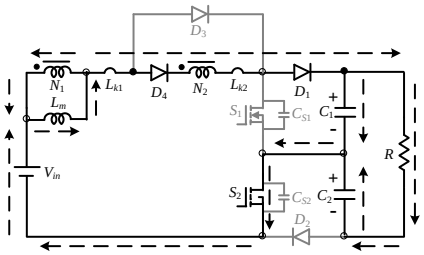


(d) Mode IV



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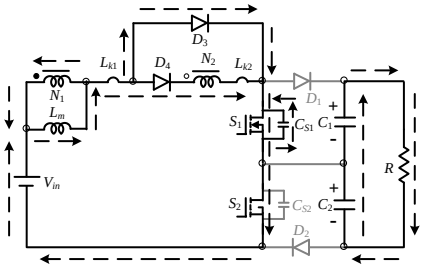

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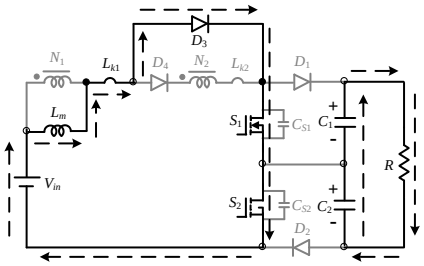

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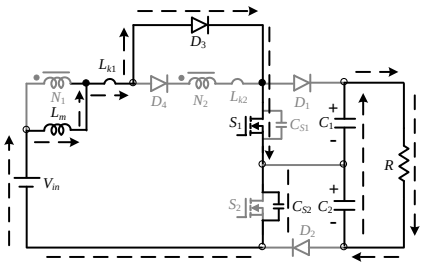

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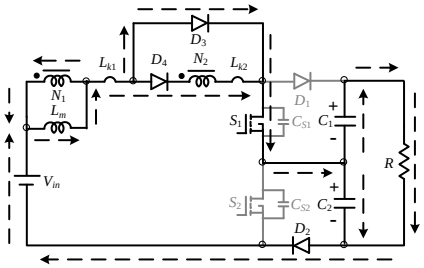
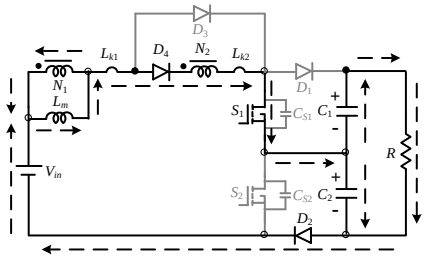


(i) Mode IX



(j) Mode X

Fig. 5. Current-flow path of operating modes during one switching period at CCM operation.

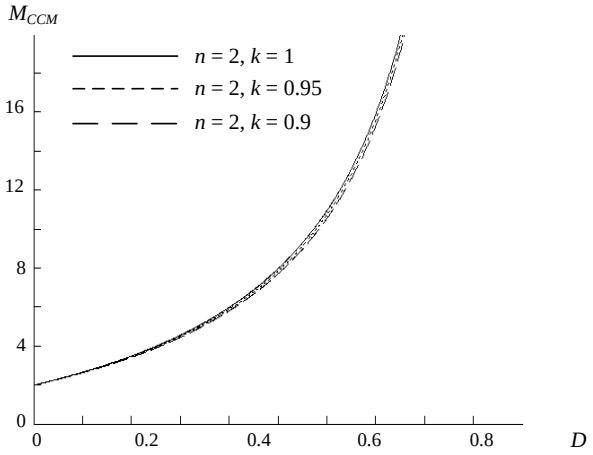


Fig. 6. Voltage gain versus duty ratio of the proposed converter at CCM operation with n = 2 and various values for k.

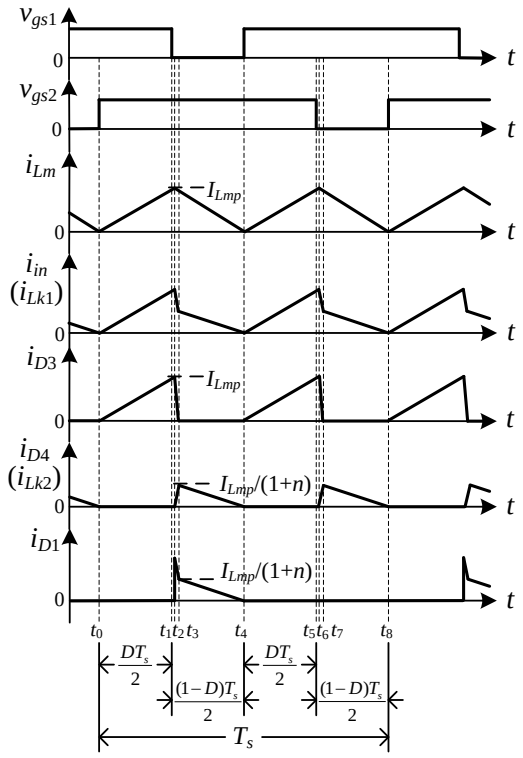


Fig. 7. Some typical waveforms of the proposed converter at BCM operation.

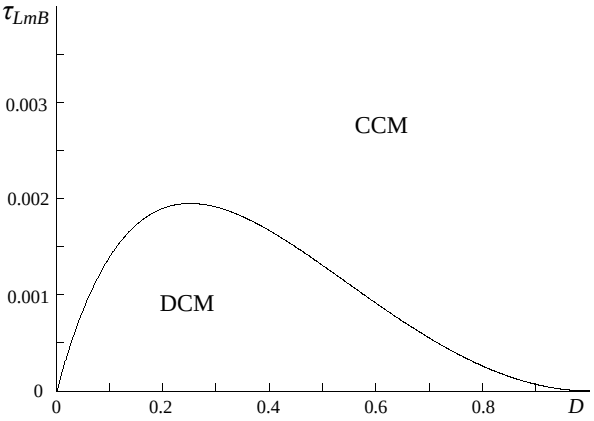
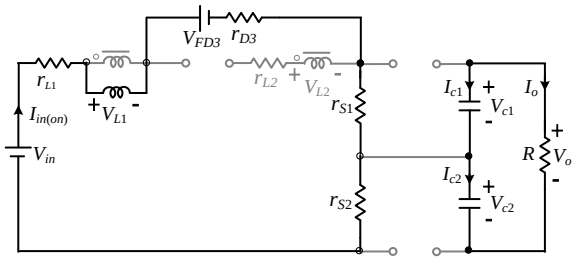
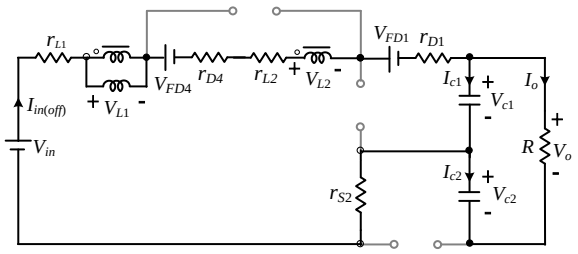


Fig. 8. Boundary condition of the proposed converter with $n = 2$ and $k = 1$.



(a)



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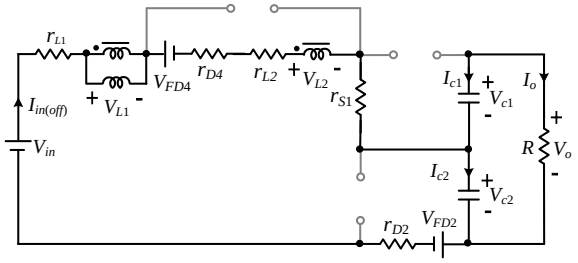


(c)

Fig. 9. Equivalent circuit of the proposed converter, including ESR of the coupled inductor, the ON-state forward voltage drop and resistance of the diodes, and the ON-state resistance of the switches. (a) S_1 and S_2 ON. (b) S_1 OFF and S_2 ON. (c) S_1 ON and S_2 OFF.

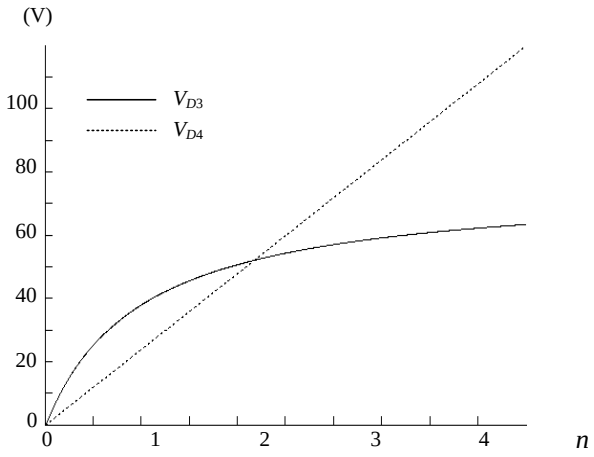


Fig. 10. Voltage stresses on D_3 and D_4 versus the turns ratio of the coupled inductor.

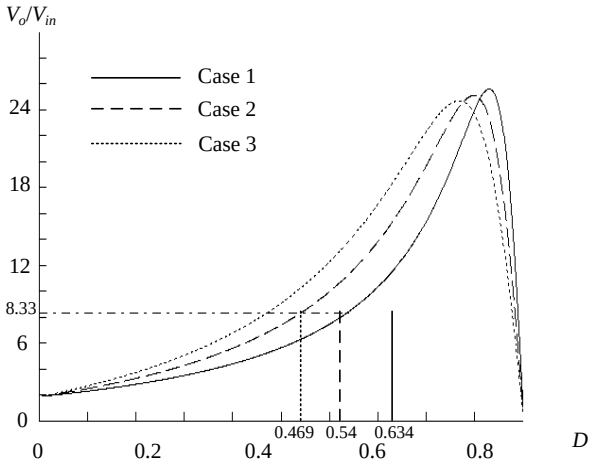


Fig. 11. Calculated voltage gain versus duty ratio.

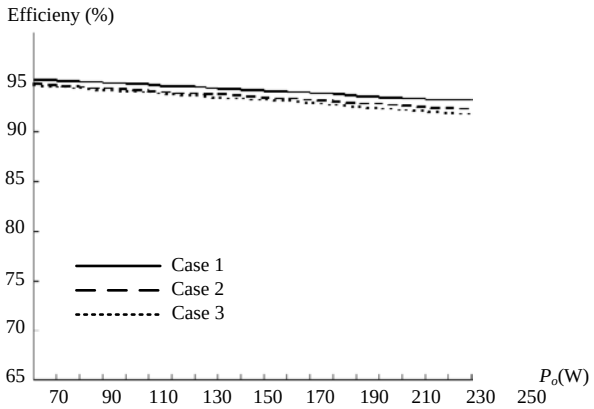
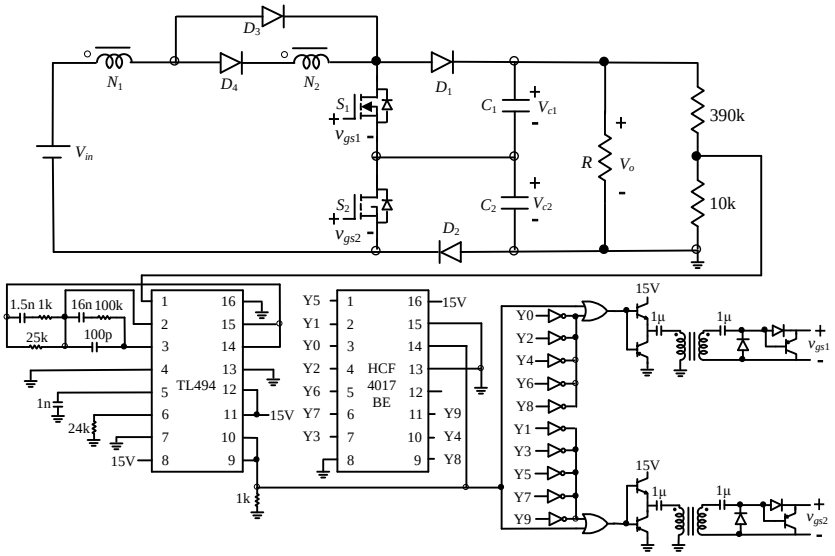


Fig. 12. Calculated efficiency versus output power.



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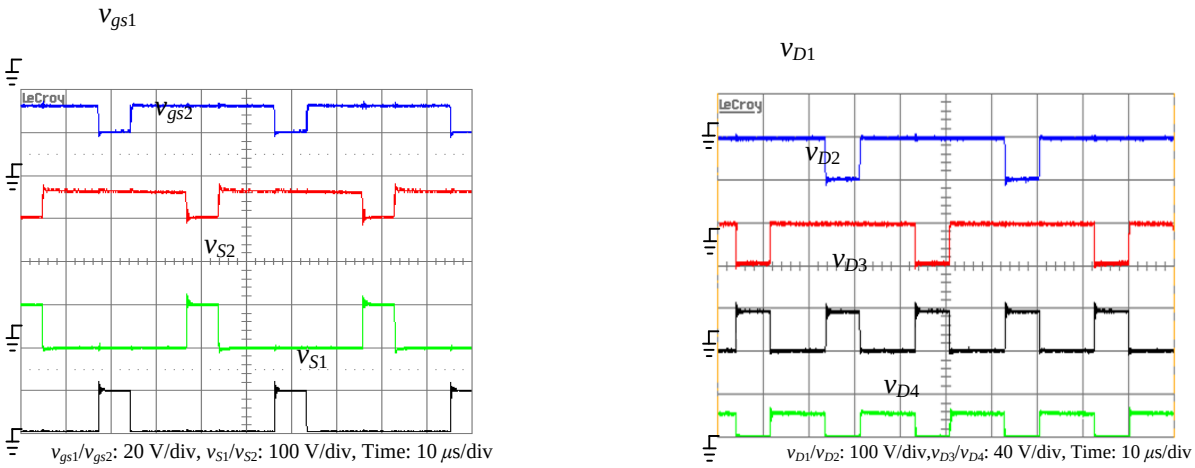
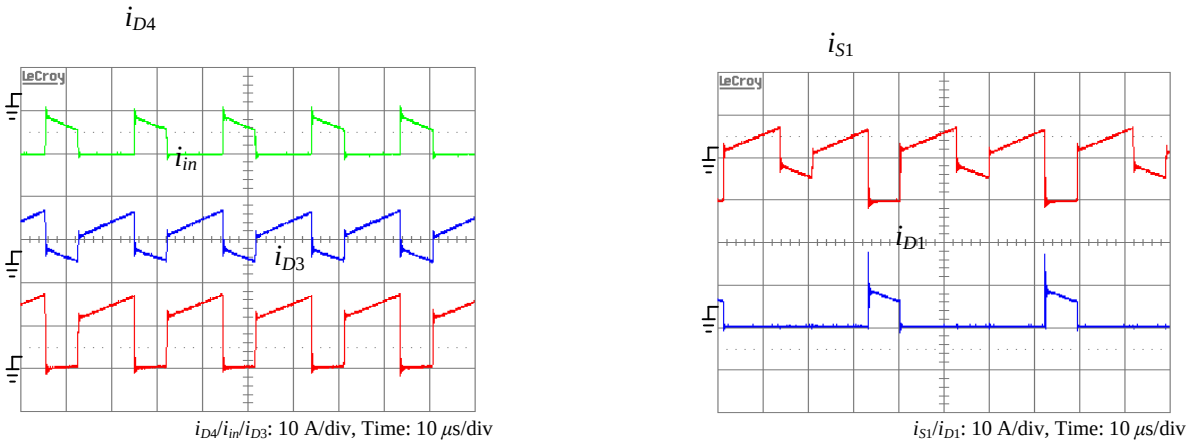


(a) (b)

Fig. 14. Experimental waveforms. (a) v_{gs1}, v_{gs2}, v_{S1}, and v_{S2}. (b) v_{D1}, v_{D2}, v_{D3}, and v_{D4}.



(a) (b)

Fig. 15. Experimental waveforms. (a) i_{D4}, i_{in}, and i_{D3}. (d) i_{S1} and i_{D1}.

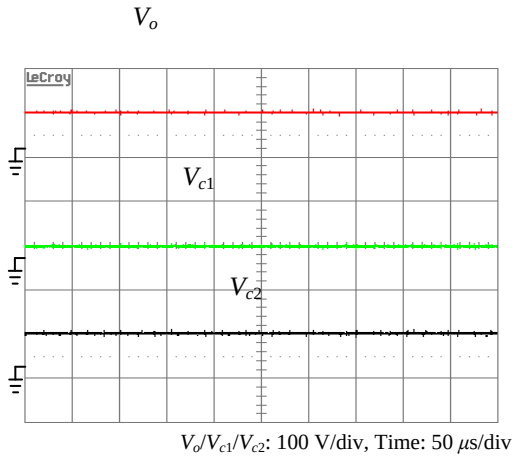
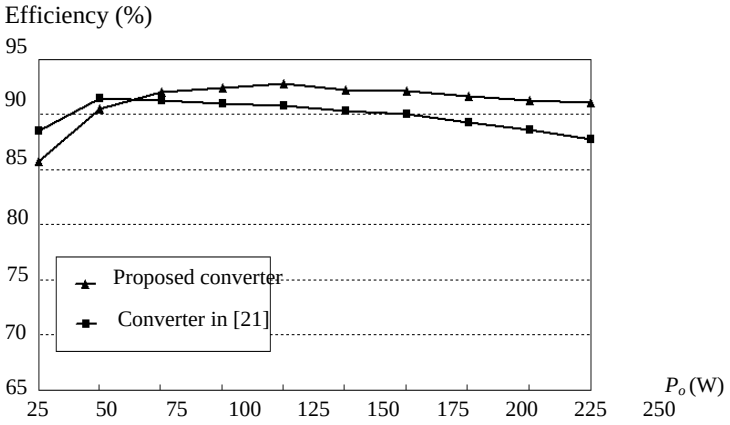


Fig. 16. Experimental waveforms for V_{c1}, V_{c2}, and V_o.



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