Novel Isolated High-step-up DC–DC Converter with Voltage Lift

Tsorng-Juu Liang, *Member*, *IEEE*, Jian-Hsieng Lee, Shih-Ming Chen, Jiann-Fuh Chen, *Member, IEEE,* and Lung-Sheng Yang

***Abstract* –A novel two-switch high-step-up isolated converter with voltage lift is proposed in this paper. The proposed isolated converter utilizes a transformer with low turn ratio to achieve high step-up gain. The secondary winding charges two boosting capacitors in parallel as switches during the switch-on period, and two boosting capacitors are discharged in series during switch-off period. Thus, the converter has high voltage gain with appropriate duty ratio. In addition, by using two clamping diodes and capacitor on the primary side, leakage energy is recycled and the voltage spikes of the two active switches are clamped, thereby improving conversion efficiency. Finally, experimental results based on a prototype implemented in the laboratory with input voltage 24 V, output voltage 200 V, and output power 200 W verify the performance of the proposed isolated converter; full-load efficiency is nearly 93%.**

***Index Terms* – High-step-up, two-switch isolated converter, voltage lift technique, high voltage gain**

I. Introduction

In 2011, the March 11 earthquake in Japan severely damaged several reactors at the Fukushima Nuclear Plant, thereby releasing a significant amount of radioactive material into the atmosphere. This event has led people to consider global abolishment of nuclear power plant operations. Furthermore, in recent years, massive amounts of petrochemical energy has been used, producing high levels of pollution that cause drastic climate change from the release of greenhouse gases. Thus, the development of clean and green renewable energy conversion systems, such as photovoltaic (PV), fuel cell, and tide energy conversion systems need to be accelerated. Front-end stage circuits of these applications need a high-step-up converters. These converter can be also applied in battery backup systems for uninterrupted power supplies (UPS) and high-intensity discharge (HID) lamp ballasts for motorcycle/automobile lighting also require high-step-up converters [1],[2].

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Conventional isolated converters such as flyback, forward, push–pull, and SEPIC converters can achieve high voltage gain by adjusting the turn ratio of the transformer. However, leakage of inductance energy in the transformer causes high voltage spikes in the switches, reducing system efficiency [3]–[5]. In order to reduce the voltage spike, snubber circuits can be used to reduce the voltage spike, such as resistor–capacitor–diode (RCD) snubber circuits, non-dissipative snubber circuits, and active clamp circuits [7]–[9].

Many non-isolated topologies have been presented to obtain high step-up voltage gain in the past decade [10]–[26]. These non-isolated converters can be used with the coupled-inductor [10]–[16], cascaded technique [17]–[22], and switched-inductor and switched-capacitor techniques [23]–[26] to obtain high voltage gain with the appropriate duty ratio. However, non-isolated converters cannot meet the safety standards needed in galvanic isolation. In order to meet the safety standards of galvanic isolation, some isolated converters for high-step-up applications have been proposed. These converters are secondary-series boost converters [27],[28], voltage-lift techniques [29],[30], and boost-type converters integrated with transformer [31],[32] to obtain high voltage gain. Active clamp circuits can be used to recycle energy leakage and also reduce voltage spike of switches. Since these circuits require two or more drive signals. This will increase the drive circuit and control complexity.

This paper proposes a novel high-efficiency high-step-up isolated DC–DC converter using one control gate driver signal and diodes D_1 and D_2 to recycle leakage energy of the transformer to the input side. According to the concept of charge in parallel and discharge in series, output capacitors C_1 and C_2 and diode D_3 and D_4 are utilized to form two voltage double circuits and obtain high voltage gain. The system configuration of the proposed isolated DC–DC topology is depicted in Fig. 1. The circuit includes DC input voltage V_{in}, input capacitor C_{in}, two clamping diodes D_1 and D_2, two active switches S_1 and S_2, transformer Tr, two boosting capacitors C_1 and C_2, two boosting diodes D_3 and D_4, output diode D_o, output capacitor C_o, output load R. Switches S_1 and S_2 are controlled simultaneously by one control signal. The transformer includes magnetizing inductance L_m and leakage inductance L_{kp} and L_{ks}. Compared with the flyback converter or other high-step up isolated converters [29],[30] in the same output voltage, the transformer only needs a small safety standard distance.

The features of proposed isolated converter are as follows: 1) meets the safety standards of galvanic isolation.

2) smaller safety standards distance of transformer.
3) high step-up voltage gain.
4) two diodes in the primary side is used to recycle the leakage inductance energy of the transformer and also clamp the voltage of active switches, Thus, system efficiency is improved.

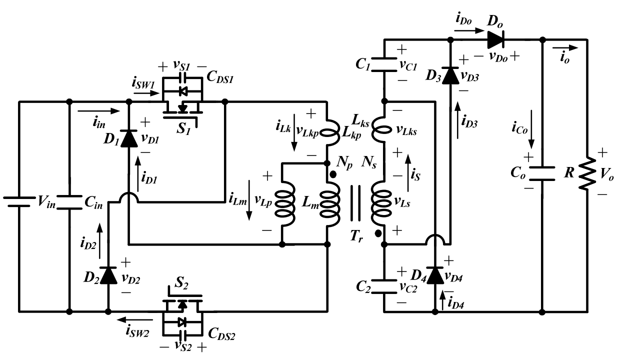


Fig. 1. Proposed isolated DC–DC converter circuit

II. OPERATING PRINCIPLE OF THE PROPOSED CONVERTER

In order to simplify the analysis of the proposed converter, the following are assumed over one switching period:
1) The capacitors C_{in}, C_1, C_2, and C_o are large enough; thus, V_{in}, V_{C1},V_{C2}, and V_o are regarded as constant values.
2) The active switches and all diodes are regarded as ideal.
3) The turn ratio of the transformer is defined as

$$n = \frac{N_S}{N_P} \tag{1}$$

where N_P and N_S are the winding turns in the primary and secondary side, respectively.
4) The parasitic inductors, capacitors, and resistors of circuit traces are ignored.

(A) CCM Operation

The key waveforms of the proposed converter at continuous condition mode (CCM) operation is depicted in Fig. 2 and discussed in detail below. In CCM operation, the operating mode of the proposed isolated converter can be divided into six operating modes over one switching period:

1) Mode I [t_0, t_1]: During this subinterval, active switches S_1 and S_2 are simultaneously on. Diodes D_1, D_2, D_3, and D_4 are reverse-biased, whereas D_o is forward-biased. The equivalent circuit of the isolated DC–DC converter is depicted in Fig. 3(a). The primary magnetizing inductance L_m stores energy from the DC input voltage V_{in}. The voltage across magnetizing inductance L_m and leakage inductance L_k in series is V_{in}. The primary current of i_{in}, i_{SW1}, i_{Lk} and i_{SW2} are equal. The current continually increases. However, the secondary winding current i_s decreases because the secondary leakage inductor L_{ks} limits the flow to the output. The secondary winding voltage v_{Ls} and boosting voltages V_{C1} and V_{C2} are linked in series to release energy to the output capacitor C_o and the output load R. When secondary winding current i_s drops to zero, boosting capacitors C_1 and C_2 begin to charge the DC input voltage V_{in}. The energy is delivered from the primary side N_p to secondary side N_s through D_3 and D_4. This operating mode ends when $i_{Lk} = i_{Lm}$ at $t = t_1$.
2) Mode II [t_1, t_2]: During this subinterval, switches S_1 and S_2 remain simultaneously on. Diodes D_1, D_2, and D_o are reverse-biased, whereas D_3 and D_4 are forward-biased. The equivalent circuit of the isolated DC–DC converter is depicted in Fig. 3(b). The primary magnetizing inductance L_m continues to store energy from the DC input voltage V_{in}. Portions of the energy from DC input voltage V_{in} is delivered to the secondary winding through D_3 and D_4 to charge the boosting capacitors C_1 and C_2, respectively. The voltages across C_1 and C_2 are nearly equal to nV_{in}, whereas the current i_{D3} is almost equal to i_{D4}. The output capacitor C_o is releases energy to output load R. This operating mode ends when active switches S_1 and S_2 are turned off simultaneously at $t = t_2$.
3) Mode III [t_2, t_3]: During this subinterval, active switches S_1 and S_2 are simultaneously off. Diodes D_1, D_2, and D_o are reverse-biased, whereas D_3 and D_4 are forward-biased. The equivalent circuit of the isolated DC-DC converter is depicted in Fig. 3(c). The leakage current i_{LK} charges the parasitic capacitor C_{DS1} and C_{DS2} of active switches S_1 and S_2. The voltages of V_{S1} and V_{S2} increase until t_3. Boosting capacitors C_1 and C_2 continue to charge the DC input voltage V_{in} through the secondary winding. D_3, D_4, and output capacitor C_o continue to release energy to output load R. This operating mode ends when the voltage V_{S1} and V_{S1} are equal to V_{in}; diodes D_1 and D_2 are forward-biased at $t = t_3$.
4) Mode IV [t_3, t_4]: During this subinterval, active witches S_1 and S_2 are simultaneously turned off. Diodes D_1, D_2, D_3, and D_4 are forward-biased, whereas D_o is reverse-biased. The equivalent circuit of the isolated DC–DC converter is depicted in Fig. 3(d). The leakage current i_{LK} flows through D_1 and D_2 to charge the input capacitor, clamping the maximum spike voltage of the two active switches so that the leakage energy can be recycled. The leakage current i_{LK} decreases quickly. Boosting capacitors C_1 and C_2 continue to produce energy in parallel mode. This operating mode ends when the clamping diode currents i_{D1} and i_{D2} equal zero at $t = t_4$.
5) Mode V [t_4, t_5]: During this sub-interval, active switches S_1 and S_2 are simultaneously off. Diode D_o is forward-biased, whereas diodes D_1, D_2, D_3, and D_4 are reverse-biased. The equivalent circuit of the isolated DC–DC converter is depicted in Fig. 3(e). The two capacitors C_{DS1} and C_{DS2} voltage decays are caused by resonant current through the leakage inductance L_k and the parasitic capacitor C_{DS1} and C_{DS2} of active switches S_1 and S_2. Boosting capacitors C_1 and C_2 still produce energy in parallel mode and output capacitor C_o continues to release energy to output load R. This operating mode ends when capacitors C_{DS1} and C_{DS2} are equal to $(V_o/n\text{-}V_{in})/2$ at $t = t_5$.
6) Mode VI [t_5, t_6]: During this subinterval, active switches S_1 and S_2 are simultaneously off. Diode D_o is forward-biased,

whereas diodes D_1, D_2, D_3, and D_4 are reverse-biased. The equivalent circuit of the isolated DC–DC converter is depicted in Fig. 3(f). The energy of magnetizing inductance L_m is delivered to the secondary winding N_p and N_s. Secondary-side voltage V_{Ls} is linked in series with V_{C1} and V_{C2} to release energy to output capacitor C_o and output load R. This operating mode ends when active switches S_1 and S_2 are turned on simultaneously at $t = t_6$.

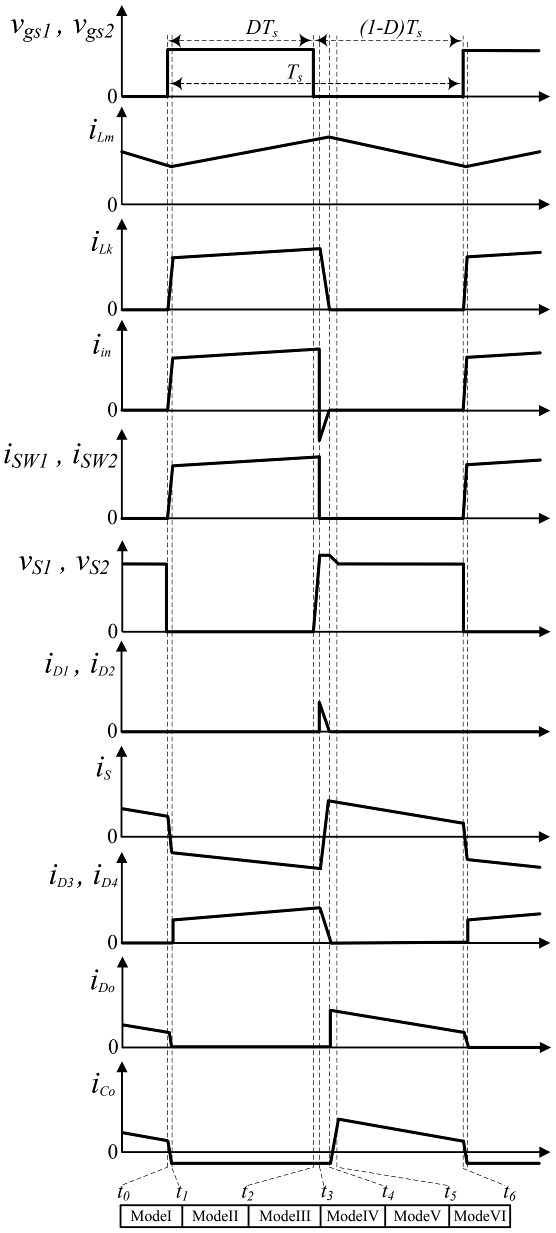
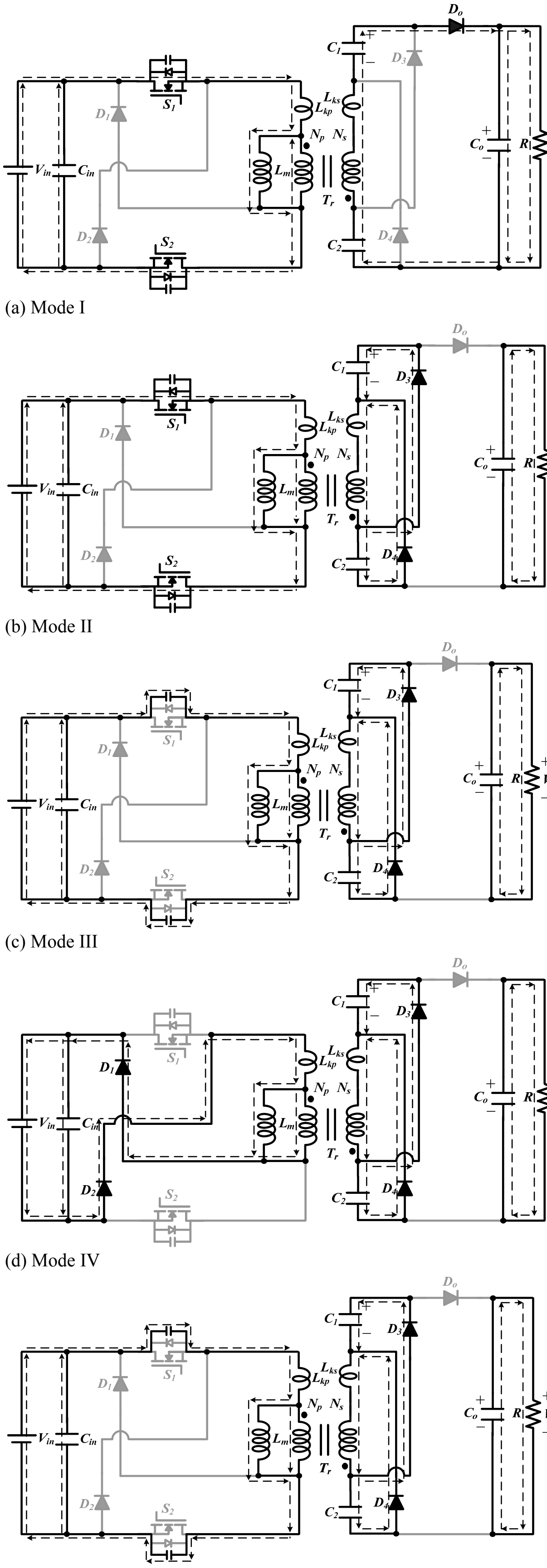


Fig. 2. Key waveforms of the proposed converter at CCM operation



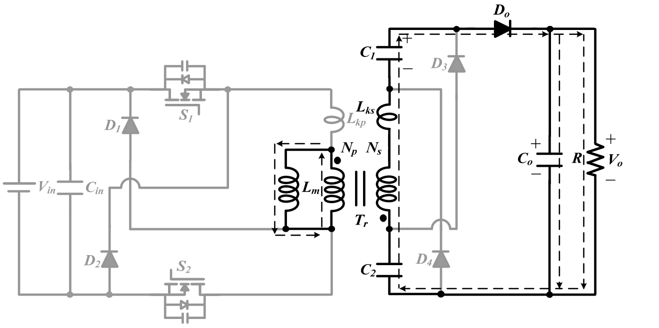
(a) Mode I

(b) Mode II

(c) Mode III

(d) Mode IV

(e) Mode V



(f) Mode VI

Fig. 3. Equivalent circuits of the isolated DC–DC converter over one switching period at CCM operation: (a) Mode I; (b) Mode II; (c) Mode III; (d) Mode IV; (e) Mode V; (f) Mode VI.

(B) DCM Operation

The key waveforms of the proposed converter at discontinuous condition mode (DCM) operation is depicted in Fig. 4. To simplify the analysis for DCM operation mode, the leakage inductances L_{kp} and L_{ks} of the transformer are neglected. Equivalent circuits of the isolated DC–DC converter over one switching period at DCM operation are depicted in Fig. 5. There are three operating modes in DCM:

1) Mode I [t_0, t_1]: During this sub-interval, active switches S_1 and S_2 are simultaneously on. Diodes D_1, D_2, and D_o are reverse-biased, whereas D_3 and D_4 are forward-biased. The equivalent circuit of the isolated DC–DC converter is depicted in Fig. 5(a). The primary magnetizing inductance L_m stores energy from the DC input voltage V_{in}. Portions of the energy by DC input voltage V_{in} is delivered to the secondary winding through D_3 and D_4 to charge capacitors C_1 and C_2. The voltages across C_1 and C_2 are nearly equal to nV_{in}, and current i_{D3} is nearly equal to i_{D4}. Output capacitor C_{o} releases energy to output load R. This operating mode ends when active switches S_1 and S_2 are turned off at $t = t_1$.
2) Mode II [t_1, t_2]: During this subinterval, active switches S_1 and S_2 are simultaneously off. Diode D_{o} is forward-biased, whereas diodes D_1, D_2, D_3 and D_4, are reverse-biased. The equivalent circuit of the isolated DC–DC converter is depicted in Fig. 6(b). The magnetic energy of L_m, C_1, and C_2 are released to output capacitor C_o and output load R. This mode ends when the energy stored in L_m is depleted at $t = t_2$.
3) Mode III [t_2, t_3]: During this subinterval, active switches S_1 and S_2 are simultaneously off. Diodes D_1, D_2, D_3, D_4, and D_{o} are reverse-biased. The equivalent circuit of the isolated DC-DC converter is depicted in Fig. 6(c). The energy stored in output capacitor C_{o} is discharged to load R. This mode ends when active switches S_1 and S_2 are turned on at $t = t_3$.

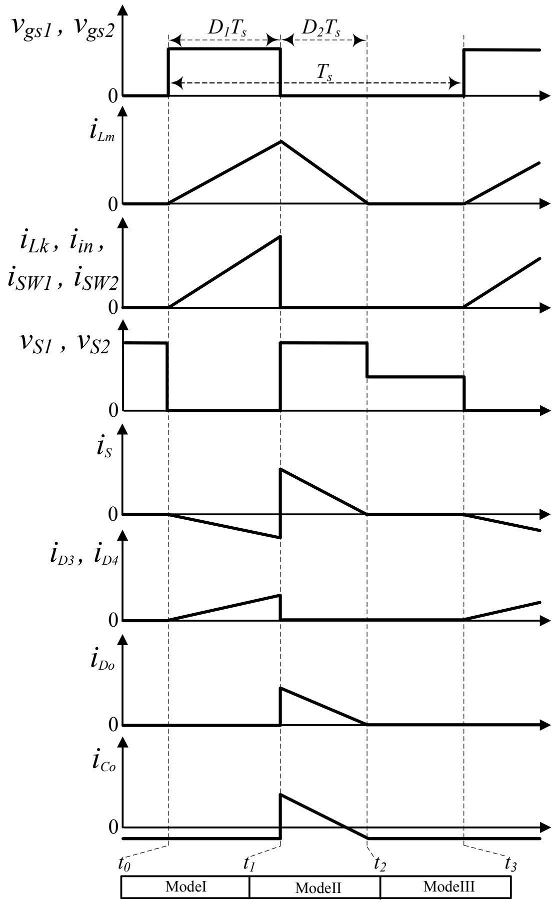
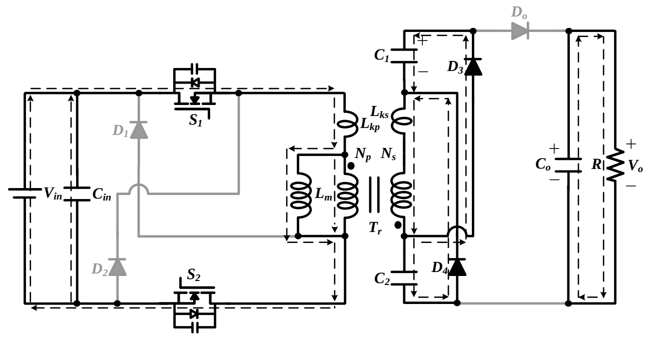
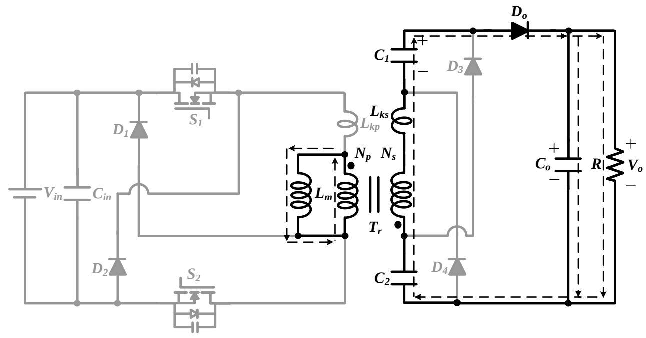


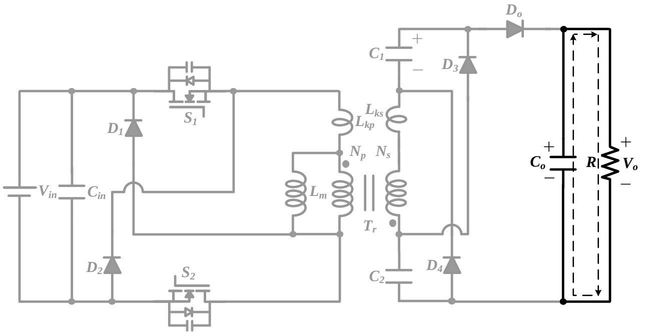
Fig. 4. Key waveforms of the proposed converter at DCM operation



(a) Mode I



(b) Mode II



(c) Mode III

Fig. 5. Equivalent circuits of the isolated DC–DC converter over one switching period at DCM operation: (a) Mode I; (b) Modes II; (c) Mode III.

III. Steady-state Analysis of the Proposed Converter

In steady-state condition analysis, total leakage inductance of the proposed isolated converter continues to be ignored.

(A) CCM Operation

While active switches S_1 and S_2 are simultaneously on, D_3 and D_4 are forward-biased. The primary magnetizing inductance voltage v_{Lp}, boosting capacitors voltage C_1 and C_2 are given by

$$v_{Lp} = V_{in} \tag{2}$$

$$v_{C1} = v_{C2} = nV_{in} \tag{3}$$

While active switches S_1 and S_2 are simultaneously off, the primary magnetizing-inductance voltage v_{Lp} for this interval is

$$v_{Lp} = 2V_{in} - \frac{V_O}{n} \tag{4}$$

Application of the principle of volt-second balance to primary-side magnetizing inductance L_m yields

$$\int_0^{DT_S} V_{in}dt + \int_{DT_S}^{T_S} (2V_{in} - \frac{V_O}{n})dt = 0 \tag{5}$$

Using (5), the voltage gain is

$$M_{CCM} = \frac{V_o}{V_{in}} = \frac{n(2-D)}{1-D} \tag{6}$$

Based on (6), the voltage gain compared of traditional flyback converter and proposed converter at CCM operation with turn ratio n=3 is depicted in Fig. 6. From Fig. 6, the voltage gain of the proposed converter becomes higher than the traditional flyback converters.

The active switches S_1 and S_2 ,diodes D_1– D_4, and diode D_o of voltage stresses are given by

$$v_{S1} = v_{S2} = \frac{\frac{v_o}{n} - v_{in}}{2} \tag{7}$$

$$v_{D1} = v_{D2} = v_{in} \tag{8}$$

$$v_{D3} = v_{D4} = v_o - nv_{in} \tag{9}$$

$$v_{Do} = v_o - nv_{in} \tag{10}$$

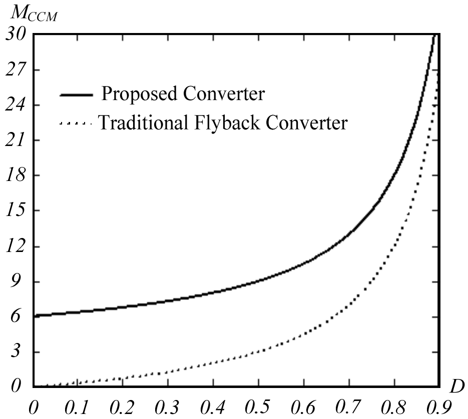


Fig. 6. Voltage gain compared of traditional flyback converter and proposed converter at CCM operation

(B) DCM Operation

In DCM operation, three modes are discussed. The key waveform is depicted in Fig. 4.

When active switches S_1 and S_2 are simultaneously on, D_3 and D_4 are forward-biased. The primary magnetizing- inductance voltage v_{Lp}, capacitors voltage C_1 and C_2 are given by

$$v_{Lp} = V_{in} \tag{11}$$

$$v_{C1} = v_{C2} = nV_{in} \tag{12}$$

The peak value of the magnetizing inductance current is given by

$$I_{Lmp} = \frac{V_{in}}{L_m} D_1 T_S \tag{13}$$

When active switches S_1 and S_2 are simultaneously off, the primary magnetizing inductance voltage v_{Lp} for this interval is

$$v_{Lp} = 2V_{in} - \frac{V_O}{n} \tag{14}$$

The peak value of the magnetizing inductance current is given by

$$I_{Lmp} = \frac{\frac{V_o}{n} - 2V_{in}}{L_m} D_2 T_S \tag{15}$$

When active switches S_1 and S_2 are simultaneously off, output diode D_o is reverse-biased. The primary magnetizing inductance voltage v_{Lp} for this interval is

$$v_{Lp} = 0 \tag{16}$$

Application of the principle of volt-second balance to primary-side magnetizing inductance L_m yields

$$\int_0^{D_1 T_s} V_{in}\,dt + \int_{D_1 T_s}^{(D_1+D_2)T_s} (2V_{in} - \frac{V_o}{n})dt + \int_{(D_1+D_2)T_s}^{T_s} 0\,dt = 0 \tag{17}$$

Using (17), the duty cycle D_2 is given by

$$D_2 = \frac{V_{in} D_1}{\frac{V_O}{n} - 2V_{in}} \tag{18}$$

Based on Fig. 4, the average current of i_{Co} is obtained as

$$I_{Co} = \frac{1}{2n} D_2 I_{Lmp} - I_O \tag{19}$$

Substituting (13), (18), and $I_{Co} = 0$ into Equation (19) yields

$$I_{Co} = \frac{1}{2nL_m}\left(\frac{V_{in}^2 D_1^2 T_S}{\frac{V_O}{n} - 2V_{in}}\right) - \frac{V_O}{R} \tag{20}$$

Because I_{Co} equals zero under steady state, (20) can be rewritten as

$$\frac{1}{2nL_m}\left(\frac{V_{in}^2 D_1^2 T_S}{\frac{V_O}{n} - 2V_{in}}\right) = \frac{V_O}{R} \tag{21}$$

The normalized magnetizing inductance time constant is defined as

$$\tau \equiv \frac{L_m}{RT_S} \tag{22}$$

where T_s is the switching period .

Substituting (22) into (21), the voltage gain is given by

$$M_{DCM} = \frac{V_o}{V_{in}} = n + \sqrt{n^2 + \frac{D_1^2}{2\tau}} \tag{23}$$

(i.e., voltage gain versus duty ratio at DCM operation with different τ and at CCM operation under $n = 3$).

Using (23), the voltage gain versus duty cycle at CCM and DCM with different τ is depicted in Fig. 7.

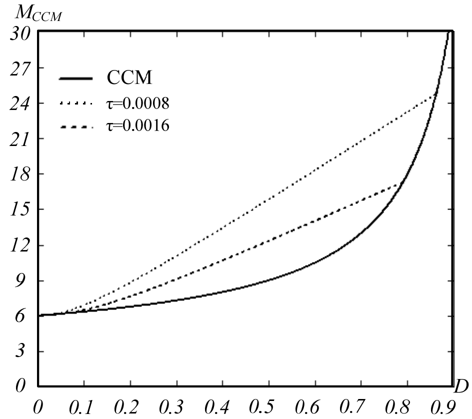


Fig. 7. Voltage gain versus duty ratio at CCM operation and at DCM operation with different τ with $n = 3$

(C) Boundary Operating Condition between CCM and DCM

If the proposed converter is operated in boundary-condition mode (BCM) (Figs. 2 and. 4), the output current of BCM I_{oB} is given by

$$I_{oB} = \frac{V_o}{R} = \frac{\frac{D}{2-D}V_o}{2L_m}\left(\frac{1}{n}\right)^2 (1-D)^2 T_s \tag{25}$$

The boundary normalized magnetizing inductance time constant defined as

$$\tau_{LB} \equiv \frac{L_m}{RT_S} \tag{26}$$

Using (25), τ_{LB} can be obtained as

$$\tau_{LB} = \frac{D(1-D)^2}{2n^2(2-D)} \tag{27}$$

The curve of τ is plotted in Fig. 8. If τ is smaller than τ_{LB}, the proposed isolated converter is operated in DCM; otherwise, the proposed isolated converter is operated in CCM

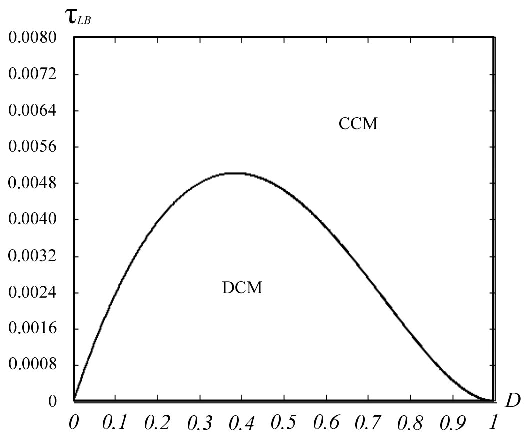


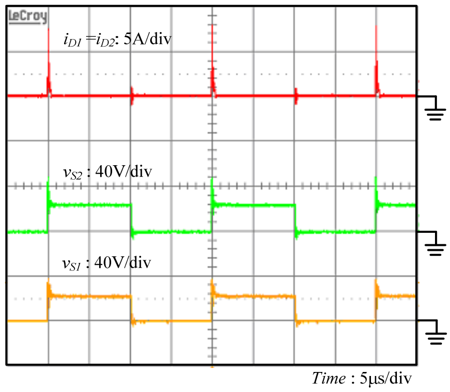
Fig. 8. Boundary condition of the proposed converter with $n = 3$

IV. Design and Experiment of the Proposed Converter

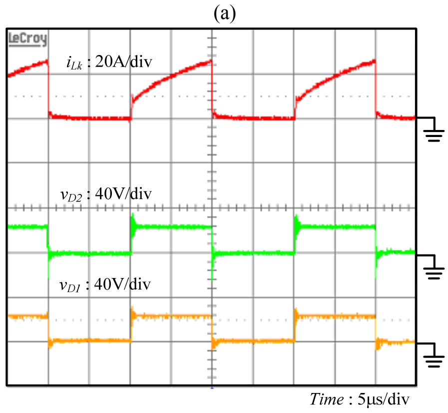
The laboratory prototype sample is implemented to demonstrate the practicability of the proposed isolated converter. The system specifications and components are as follows:

1) Input DC voltage V_{in}: 24 V
2) Output DC voltage V_o: 200 V
3) Maximum output power: 200 W
4) Operating frequency: 50 kHz
5) Input capacitor C_{in}: 3300 μF/35 V aluminum capacitor
6) Diodes D_1 and D_2: SBR20A60CTFP Schottky diode
7) Switches S_1 and S_2: IRLB3036
8) Transformer: ETD-59, core PC-40, N_p:N_s = 1:3, L_m = 43.5 μH; L_k = 0.27 μH
9) Boosting capacitors C_1 and C_2: 100 μF/ 250 V aluminum capacitor
10) Diodes D_3, D_4, and D_o: MBR20200CT Schottky diode
11) Output capacitor C_o: 220 μF/ 250 V aluminum capacitor

The experimental results at full load P_o = 200 W and V_{in} = 24 V are shown in Fig. 9. Figure 9(a) shows the waveforms v_{S1}, v_{S1}, i_{D1}, and i_{D2}. The current waveform i_{D1} equals i_{D2} because their current path is the same. In addition, i_{D1} and i_{D2} indicate that the leakage energy is recycled when S_1 and S_2 are turned off. The reduced loss is approximated 3.4 W. Figure 9(b) shows the waveforms of v_{D1}, v_{D1}, and i_{Lk}, and Figure 9(c) shows the waveforms of v_{C1}, v_{C2}, i_{D3}, and i_{D4}. Capacitors C_2 and C_3 are similar to forward converters charging energy in parallel when switches S_1 and S_2 are turned on, and the discharged energy in series is similar to a flyback converter when switches S_1 and S_2 are turned off. Current i_{D3} is approximately equal to i_{D4}. Figure 9(d) shows the waveforms of v_{D3}, v_{D4}, and i_S. The voltage stresses of D_3 and D_4 are approximately equal. The current of secondary winding i_S is equal to i_{D3} + i_{D4} when switches S_1 and S_2 are turned on. Figure 9(e) shows the voltage and current waveforms of v_{Do} and i_{Do}. The experimental results at P_o = 40 W and V_{in} = 24 V are shown in Fig. 10. The voltage waveforms of v_{S1}, v_{S2}, v_{D1}, v_{D2}, v_{D1}, and v_{Do} have some oscillations caused by the parasitic capacitor C_{DS1} and C_{DS2} of the active switches S_1 and S_2. The primary magnetizing inductance L_m and the leakage inductance L_k are formed in resonance when i_{Lm}=0. Figure 11 shows the experimental conversion efficiency of the proposed isolated converter. Maximum efficiency is 96.2%, and efficiency is 92.9% at full load. High current on primary side cause higher conduction loss and resistance R_T of transformer loss under high power condition. Thus, the efficiency is decreased at high power. Hence, the efficiency decays when the output power increases. The power loss analysis of the proposed converter at full load P_o = 200 W and V_{in}= 24 V are shown in Table 1 [33],[34]. The measured efficiency at 92.9 % and the calculated results at 95.52 % are slightly different, because the calculated results are losses of neglect switching, iron, and resistance of circuit traces.



(a)



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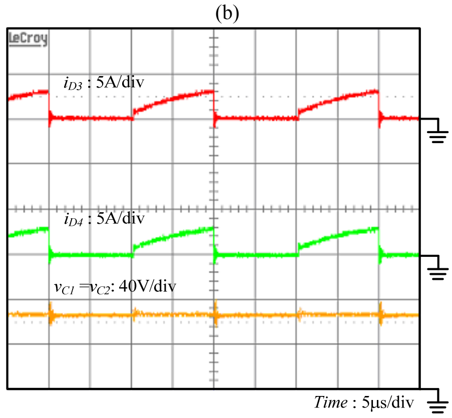
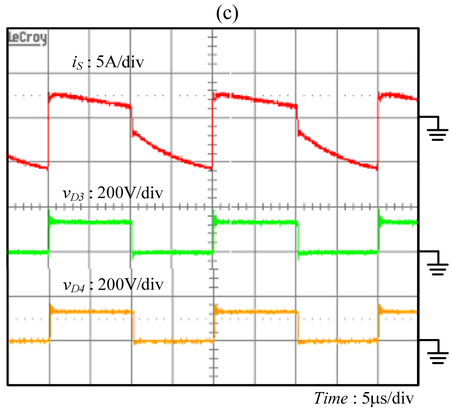
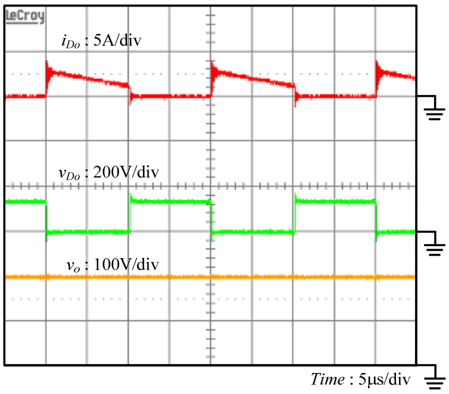


(c)

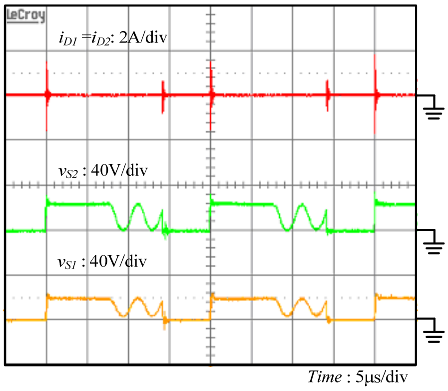


(d)

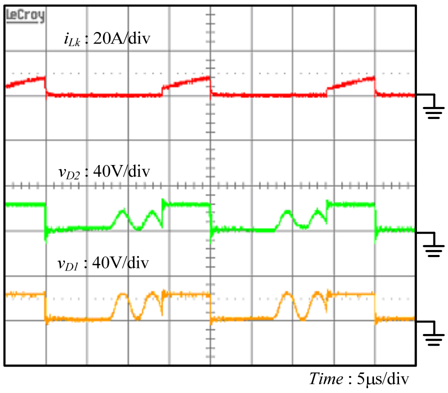


(e)

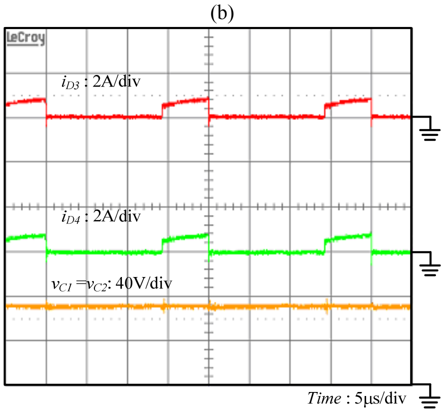
Fig. 9. Experimental waveforms at $P_o = 200$ W



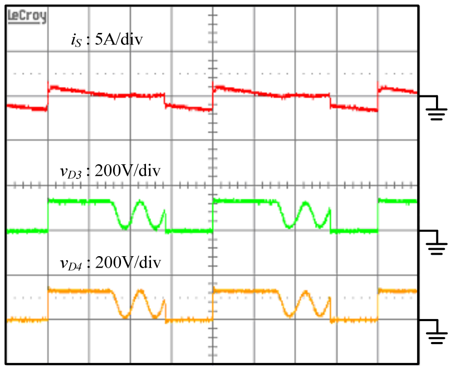
(a)



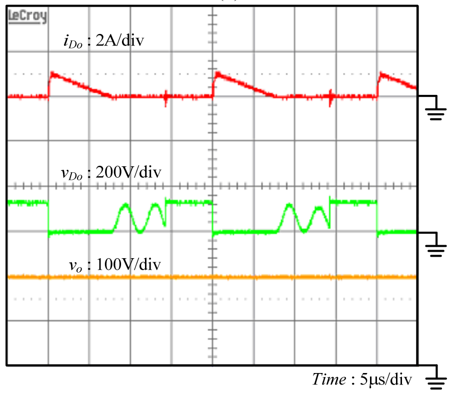
(b)



(c)



(d)



(e)

Fig. 10. Experimental waveforms at $P_o = 40$ W

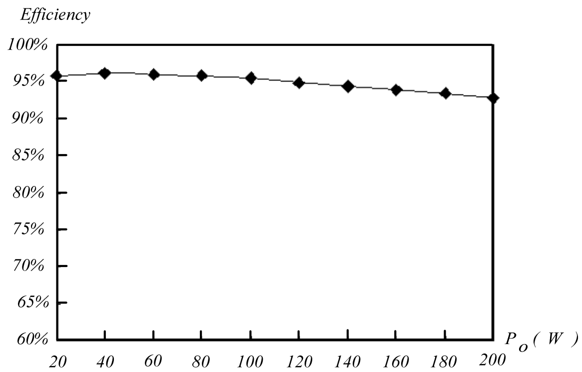


Fig. 11. Experimental conversion efficiency of proposed isolated converter

Table 1. Power loss analysis of the proposed converter at full load 200W

Components	Parameters	Loss (W)	%
Switches S_1 and S_2	1.9 mΩ	0.58	0.29
Clamping Diodes D_1 and D_2	0.7 V	0.2	0.1
Resistance R_T of transformer	28 mΩ	5.24	2.62
Boosting diode D_3 and D_4	0.7 V	2.8	1.4
Output diode D_0	0.7 V	0.7	0.35
Total loss		9.52	4.76

V. Conclusions

In this paper, forward and flyback converters are successfully integrated using voltage-lift technique to achieve high voltage gain. Energy stored in the primary leakage inductance during on-time is returned to v_{in} via clamping diodes D_1 and D_2. This not only improves converter efficiency, it also reduces voltage spike of active switches such that low-voltage stresses and low on-resistance R_{on} switches can be selected. The CCM and DCM operating principle and steady state of voltage gain are analyzed in detail. Finally, a prototype of the proposed converter with input voltage 24 V, output voltage 200 V, output power 200 W, maximum efficiency of 96.2%, and switch voltage spikes lower than 48 V is achieved in the laboratory.

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