Novel MTJ-Based Shift Register for Non-Volatile Logic Applications

Thomas Windbacher, Hiwa Mahmoudi, Viktor Sverdlov, and Siegfried Selberherr
Institute for Microelectronics, TU Wien, Gußhausstraße 27–29/E360, A–1040 Wien, Austria
Email: {windbacher | mahmoudi | sverdlov | selberherr}@iue.tuwien.ac.at

***Abstract*—The increasing costs and leakage losses have become the major concerns for CMOS technology scaling. A possible way to address in particular the standby power problem is to introduce non-volatility into the devices and circuit blocks so that unused devices or even entire circuit blocks do not waste energy, and power is only spent, when information is read or written. Recently, we proposed a non-volatile magnetic flip flop which moves the information storage and processing from the CMOS domain to the magnetic domain. Here, we propose a way to extend the functionality of the device to a shift register; computing via spin wave superposition and passing information by spin torque transfer (STT). The presented shift register and its operation allows an extremely dense layout, is CMOS compatible, and non-volatile.**

I. Introduction

The ever increasing demand for cheap and fast electronics drives the scaling efforts of semiconductor industry. However, with every technology generation of CMOS devices it becomes harder to control the leakage due to short channel effects and gate dielectrics thinning. Introducing non-volatility in the basic building blocks allows to bypass the leakage power issue by spending energy only when reading or writing as well as it enables instant-on applications, since initialization procedures can be considerably simplified or may even be skipped completely. Magnetic tunnel junctions (MTJs) have drawn recently much of attention due to the high endurance, infinite retention of stored information, low power consumption for writing and reading, fast switching and access, and little additional wear due to reading/writing cycles. Even though Zhao et al. [1] have shown non-volatile flip flops, they employ MTJs only as ancillary devices, while the actual computation takes place in the CMOS domain, which suffers under scaling. Recently, we proposed a non-volatile magnetic flip flop free of this problem by carrying out the logic operation in the magnetic domain via constructive or destructive spin wave superposition and storing the information as magnetization orientation and also checked for proper operation via extensive micromagnetic simulations [2]. The flip flop structure consists of three perpendicular MTJ stacks - two for input (A,B) and one for readout (Q) - sharing a common free layer (see Fig. 1). Applying a current to one input MTJ generates a spin wave which travels to the other end where it gets reflected, heads back, gets pushed again, and so on. During this oscillating motion the magnetization precession in the common layer starts to build up, until it eventually passes the energy barrier separating the two stable magnetization states and relaxes into the new magnetization state. By applying two synchronous voltage or current pulses two spin waves are generated, which either superimpose constructively for pulses with similar polarities (the same spin torque orientation) or destructively for pulses with opposing polarities. (cf. Tab. I).

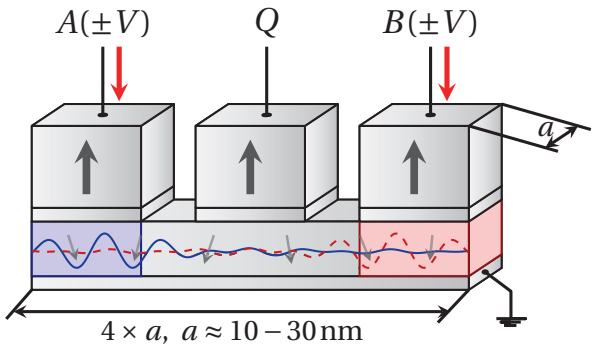

Fig. 1. Non-volatile magnetic flip flop exhibiting a shared free layer storing the information via magnetization orientation, two stacks A,B for input and one stack Q for output. The current (voltage) polarities and the magnetization orientation of the free layer are mapped to logic "0" and "1".

TABLE I. Logic table of non-volatile magnetic flip flop. The flip flop sets or resets its state for pulses with identical polarities (1,0) and keeps its state for opposing polarities ($Q(l-1)$, l denotes the time step).

A	B	$Q(l)$
0	0	0
0	1	$Q(l-1)$
1	0	$Q(l-1)$
1	1	1

II. Non-Volatile Shift Register

Using the proposed flip flop is beneficial, because, instead of eight CMOS transistors (non clocked) or twelve CMOS transistors (clocked) needed for a classic RS flip flop or seven transistors and two magnetic tunnel junction memory elements required for a flip flop with MTJs proposed in [1], only three MTJs are employed.

Even more, we propose a novel shift register topology which takes advantage of the peculiarities of the proposed non-volatile flip flops enabling an extremely dense layout. Arranging two rows of flip flops in two different levels (see Fig. 2) along a line or in a cross-like structure (cf. Fig. 3) and employing two shifted clock signals (Clk_1 and Clk_2, see Fig. 5), information stored in one flip flop can

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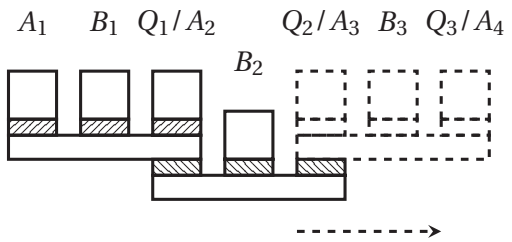

Fig. 2. Side view of a shift register topology enabling information transport via spin transfer torque. Either the first level (A_1,B_1,Q_2/A_3,B_3,$\cdots$, first clock signal Clk_1) is powered or the second level is active (Q_1/A_2,B_2,$\cdots$, second clock Clk_2) passing the information stored in the shared free layers between the subsequent flip flops.

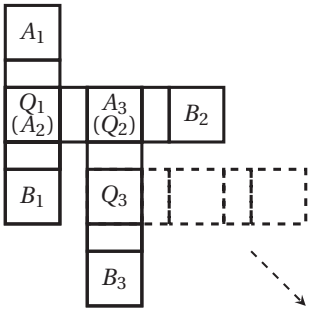

Fig. 3. Top view of an alternative cross topology for a two level shift register. Odd (even) flip flops are in the top (bottom) layer.

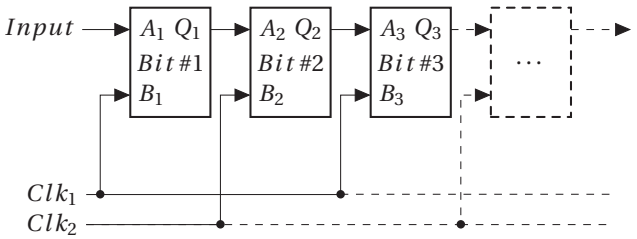

Fig. 4. Equivalent circuit diagram of the non-volatile shift register. Odd (even) flip flops are operated by clock signal Clk_1 (Clk_2).

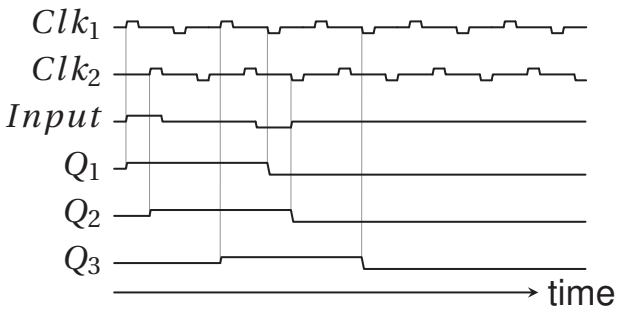

Fig. 5. Example signal sequence illustrating how information is written into the first flop Q_1 ($Input$ and Clk_1 exhibit same polarities), then passed to the second flip flop Q_2 (Q_1 and Clk_2 same polarity) and from there to the third flip flop Q_3 (Q_2 and Clk_1).

be successively passed to the next subsequent flip flop via the STT effect. Every flip flop is alternately operated in a writing and a reading mode. In the writing mode the inputs A_i and B_i are active, while Q_i is inactive. In this mode one input is fed with the information/signal while the other is fed by one of the two clock signals (depending on its level, cf. Fig. 4). In the reading mode A_i and B_i are inactive and Q_i is active. A safe decoupling between the two operation modes is achieved by the two phase shifted clock signals (see Fig. 5). Furthermore, unintentional flipping of the shared free layer magnetization is avoided by the mismatch in the required pulse duration for writing. In reading mode only region Q_i exerts a spin torque on the shared free layer, while in writing mode two regions A_i and B_i exert a spin torque on the shared free layer. Therefore, it takes about twice as long to change the magnetization orientation in reading mode than in writing mode.

We illustrate the working principel with an example (see Fig. 2, Fig. 4, and Fig. 5). Starting with the first flip flop in the first level (A_1,B_1, and Q_1); applying an input pulse to A_1 and a first clock signal Clk_1 to B_1 will set or reset the flip flop, if both pulses exhibit the same polarity. So when the input signal and the Clk_1 exhibit the same torque on the shared free layer, information is written into the first free layer and becomes available via Q_1. Next Clk_1 turns inactive and Clk_2 active. Now the first flip flop is in reading mode, where a current passes the first free layer and a tunnel barrier separating the free layers before it enters the second free layer and exerts a spin torque on the second free layer. At the same time Clk_2 also creates spin torque in the B_2 region and two synchronous spin waves are generated, which either superimpose constructively or destructively. Then Clk_2 becomes inactive again and Clk_1 active, so that the second flip flop is in reading mode and information is passed via the STT effect to the third free layer and so on.

One additionally must mention that the voltage or current signals passing the information at Q_i must be synchronous to the respective clock signals but are fed with constant polarities to compensate the additional degree of freedom introduced by the variable shared free layer magnetization. To guarantee that the information stored in one shared free layer will be successfully copied into the next subsequent flip flop the clock signals Clk_1 and Clk_2 require a positive and negative pulse within the signal period.

III. Conclusion

A novel non-volatile shift register based on three MTJs with a shared free layer has been proposed. It is compatible with CMOS technology and is characterized by an extremely dense layout opening new opportunities for implementing MTJ based non-volatile logic.

Acknowledgment

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References

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