

Novel Multilevel Inverter Carrier-Based PWM Method

Leon M. Tolbert, *Senior Member, IEEE*, and Thomas G. Habetler, *Senior Member, IEEE*

Abstract—The advent of the transformerless multilevel inverter topology has brought forth various pulse width modulation (PWM) schemes as a means to control the switching of the active devices in each of the multiple voltage levels in the inverter. An analysis of how existing multilevel carrier-based PWM affects switch utilization for the different levels of a diode-clamped inverter is conducted. Two novel carrier-based multi-level PWM schemes are presented which help to optimize or balance the switch utilization in multilevel inverters. A 10 kW prototype six-level diode-clamped inverter has been built and controlled with the novel PWM strategies proposed in this paper to act as a voltage source inverter.

Index Terms—Carrier-based pulsewidth modulation, diode-clamped inverter, multilevel converter, multilevel inverter, multilevel pulse width modulation.

I. INTRODUCTION

Multilevel pulse width modulation (PWM) inverters have been developed to overcome shortcomings in solid state switching device ratings so that large motors can be controlled by high-power adjustable frequency drives. The most popular structure proposed as a transformerless voltage source inverter is the diode clamped converter based on the neutral point converter proposed by Nabae [1]. A three-phase 6-level diode-clamped inverter is shown in Fig. 1.

The two multilevel PWM methods most discussed in the literature are multilevel carrier based PWM and multilevel space vector PWM; both are extensions of traditional two-level PWM strategies to several levels. Investigators have proposed carrier-based multilevel sine-triangle PWM schemes for control of a multilevel diode clamped inverter used as a motor drive or static var compensator [2]–[9]. Others have generalized space vector PWM theory for use with multilevel inverters [10]–[12]. A third PWM method used to control a multilevel diode clamped converter is with selective harmonic elimination [13]–[14].

While the multilevel PWM techniques developed thus far have been extensions of two-level PWM methods, the multiple levels in a diode-clamped inverter offer extra degrees of freedom and greater possibilities in terms of device

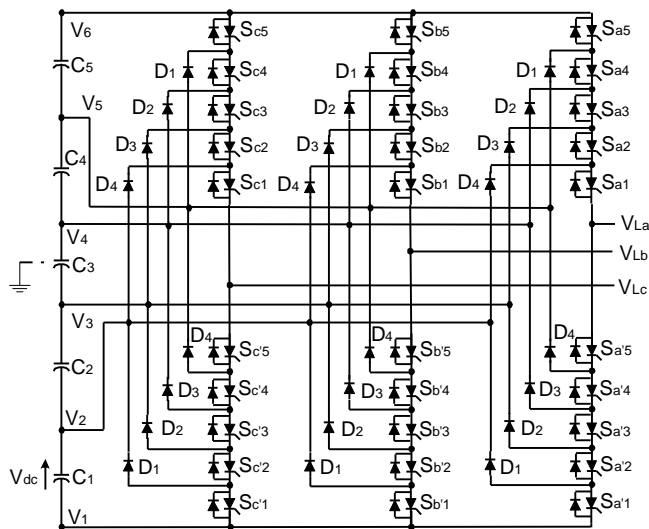


Fig. 1. Circuit diagram of a three-phase 6-level diode clamped inverter.

utilization, state redundancies, and effective switching frequency. In this paper, novel carrier-based multilevel PWM schemes are presented which take advantage of the special properties available in multilevel inverters to minimize switch utilization and/or balance the switching duty among its various levels.

II. EXISTING MULTILEVEL CARRIER-BASED METHODS

A. Subharmonic PWM Method

Other authors have extended two-level carrier based PWM techniques to multilevel inverters by making the use of several triangular carrier signals and one reference signal per phase. Carrara [3] developed multilevel subharmonic PWM (SH-PWM) as follows. For an m -level inverter, $m-1$ carriers with the same frequency f_c and same peak-to-peak amplitude A_c are disposed such that the bands they occupy are contiguous. The reference, or modulation, waveform has peak-to-peak amplitude A_m and frequency f_m , and it is centered in the middle of the carrier set. The reference is continuously compared with each of the carrier signals. If the reference is greater than a carrier signal, then the active device corresponding to that carrier is switched on; and if the reference is less than a carrier signal, then the active device corresponding to that carrier is switched off. In multilevel inverters, the amplitude modulation index, m_a , and the frequency ratio, m_f , are defined as

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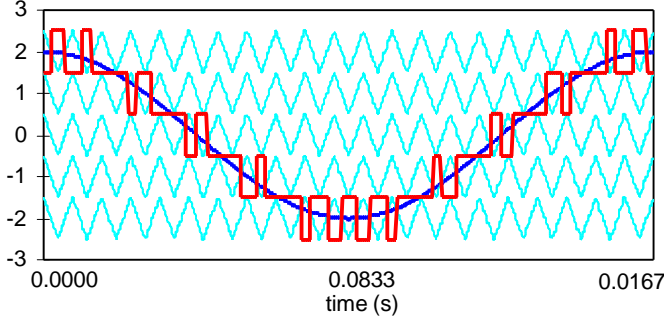


Fig. 2. Multilevel carrier-based SH-PWM showing carrier bands, modulation waveform, and inverter output waveform ($m = 6$, $m_f = 21$, $m_a = 0.8$).

$$m_a = \frac{A_m}{(m-1) \cdot A_c}, \quad (1)$$

$$m_f = \frac{f_c}{f_m}. \quad (2)$$

Carrara also considered different methods of disposing the many carrier bands required in multilevel PWM. The three cases he considered for an inverter with an odd number of levels were as follows:

- 1) alternative phase opposition disposition where each carrier band is shifted by 180° from the adjacent bands;
- 2) phase opposition disposition where the carriers above the zero reference are in phase but shifted by 180° from those carriers below the zero reference;
- 3) in-phase disposition where all the carriers are in phase (further examination of in phase disposition is given in this paper).

Fig. 2 shows a set of carriers ($m_f = 21$) with all of the carriers in phase for a six-level diode-clamped inverter and a sinusoidal reference voltage with $m_a = 0.8$. The resulting output voltage of the inverter is also shown in Fig. 2.

B. Switching Frequency Optimal PWM Method

Steinke [2] proposed a carrier-based method termed switching frequency optimal PWM (SFO-PWM) which was similar to Carrara's except that a zero sequence (triplen harmonic) voltage is added to each of the carrier waveforms. This method takes the instantaneous average of the maximum and minimum of the three reference voltages (V_a^* , V_b^* , V_c^*) and subtracts this value from each of the individual reference voltages to obtain the modulation waveforms, i.e.,

$$V_{offset} = \frac{\max(V_a^*, V_b^*, V_c^*) + \min(V_a^*, V_b^*, V_c^*)}{2}, \quad (3)$$

$$\begin{aligned} V_{a\ SFO}^* &= V_a^* - V_{offset}, \\ V_{b\ SFO}^* &= V_b^* - V_{offset}, \\ V_{c\ SFO}^* &= V_c^* - V_{offset}. \end{aligned} \quad (4)$$

SFO-PWM is illustrated in Fig. 3 for the same reference voltage waveform that was used in Fig. 2. The resulting output voltage of the inverter is also shown in Fig. 3. The

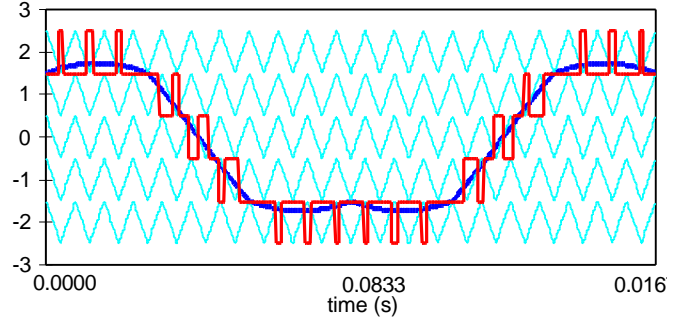


Fig. 3. Multilevel carrier-based SFO-PWM showing carrier bands, modulation waveform, and inverter output waveform ($m=6$, $m_f = 21$, $m_a = 0.8$).

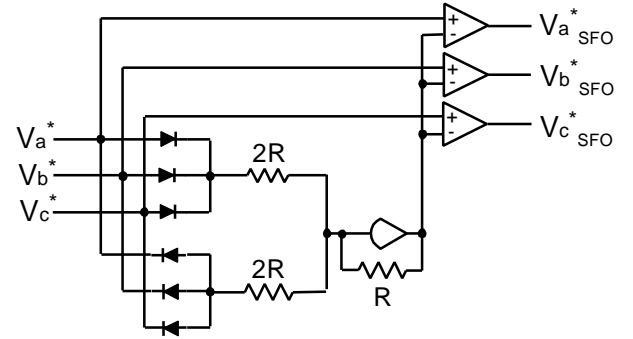


Fig. 4. Analog equivalent circuit for SFO-PWM zero sequence addition.

SFO-PWM technique can only be used for three-phase three-wire systems, and it enables the modulation index to be increased by 15% before overmodulation, or pulse dropping, occurs.

The addition of this triplen-offset voltage continuously centers all of the three reference waveforms in the carrier band, which Holmes [15] showed for carrier-based two-level PWM is similar to using space vector PWM with the zero voltage state divided evenly at the beginning and end of each half carrier interval. The analog equivalent of (3) and (4) is shown in Fig. 4 [16].

III. CARRIER PHASE ANGLE EFFECT ON SWITCHING

Previously, Menzies [5] considered two simple cases of what effect the displacement phase angle f , between the modulation waveform (sinusoidal reference) and the set of carrier waveforms, has on the switching of the active devices and the unfiltered inverter output waveform distortion where

$$V_a^* = |V| \cdot \cos(q - f). \quad (5)$$

The two cases considered were: 1) the carrier is a maximum when the reference is a maximum ($f = 0$), referred to as a W-type carrier set and 2) the case where the carrier is a minimum when the reference is a maximum, referred to as a M-type carrier set.

In this paper, all displacement phase angles were considered. The displacement phase angle between the reference and carrier set was varied incrementally by 0.01 radians from 0 to $2\pi/3$ radians (120 degrees) to see what effect this would have on the total switchings of the

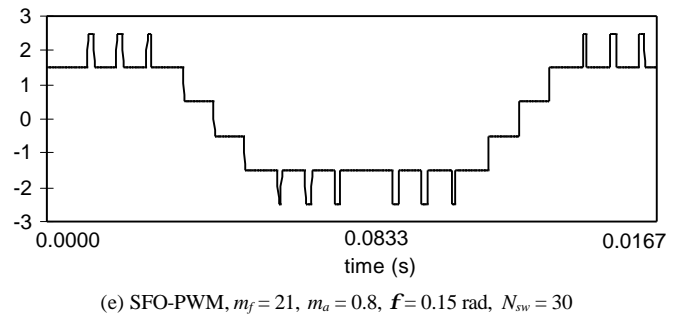
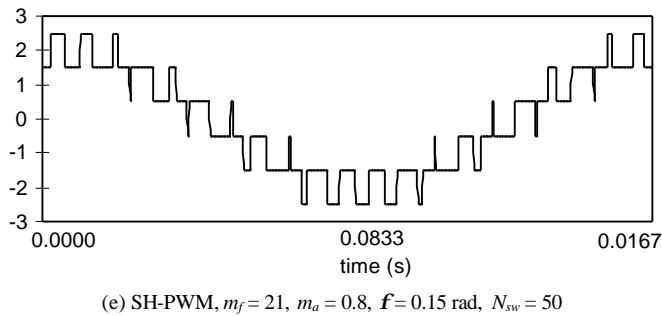
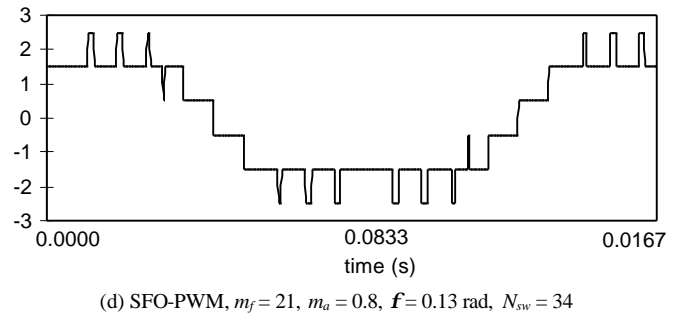
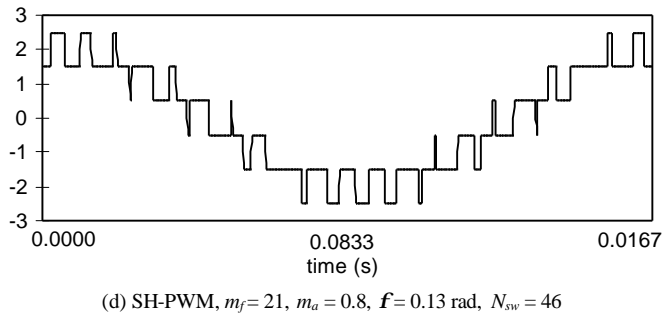
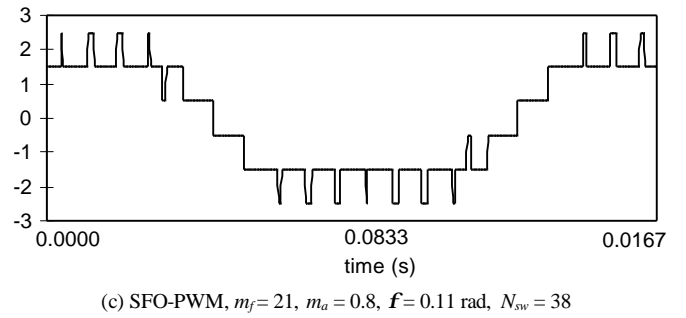
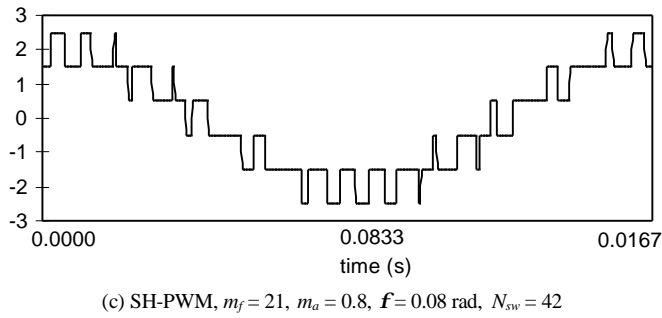
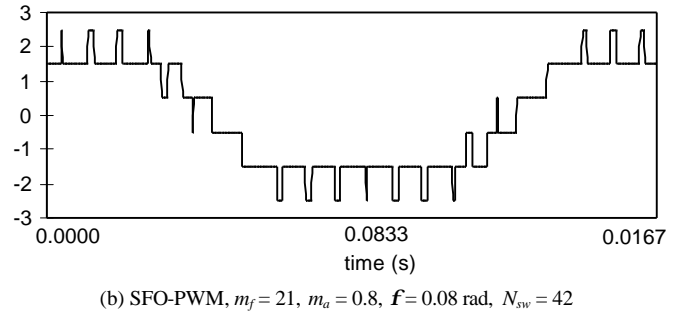
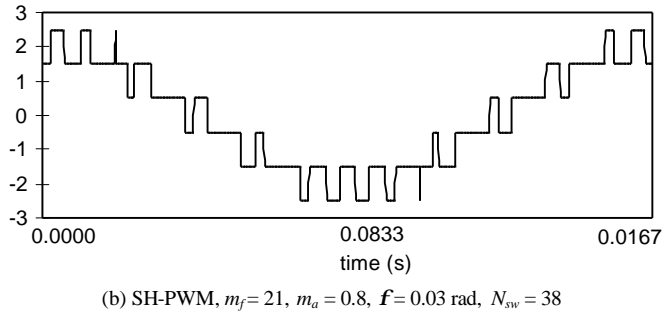
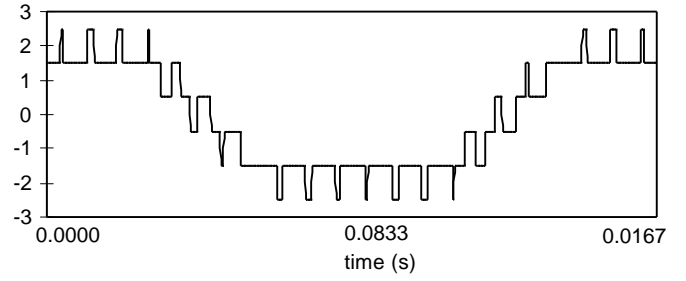
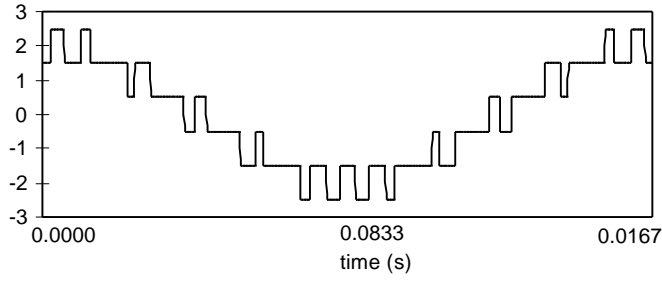


Fig. 5. Output voltage waveforms for a 6-level inverter controlled with SH-PWM for various phase angles f .

Fig. 6. Output voltage waveforms for a 6-level inverter controlled with SFO-PWM for various phase angles f .

TABLE I
NUMBER OF MAIN DEVICE SWITCHINGS IN EACH LEVEL FOR FIG. 5
AND LINE-LINE VOLTAGE THD FOR 3RD - 19TH HARMONICS

Phase Angle, f	Switches/Cycle (SH-PWM, $m = 6, m_f = 21, m_a = 0.8$)						% V_{ab} THD
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	N_{sw}	
0.00rad	8	6	6	6	8	34	5.37%
0.03rad	10	6	6	6	10	38	5.77%
0.08rad	10	8	6	8	10	42	5.34%
0.13rad	10	8	10	8	10	46	5.37%
0.15rad	10	10	10	10	10	50	5.27%

TABLE II
NUMBER OF MAIN DEVICE SWITCHINGS IN EACH LEVEL FOR FIG. 6
AND LINE-LINE VOLTAGE THD FOR 3RD - 19TH HARMONICS

Phase Angle, f	Switches/Cycle (SFO-PWM, $m = 6, m_f = 21, m_a = 0.8$)						% V_{ab} THD
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	N_{sw}	
0.03rad	14	6	6	6	14	46	4.05%
0.08rad	14	4	6	4	14	42	3.94%
0.11rad	14	4	2	4	14	38	3.70%
0.13rad	12	4	2	4	12	34	3.41%
0.15rad	12	2	2	2	12	30	2.92%

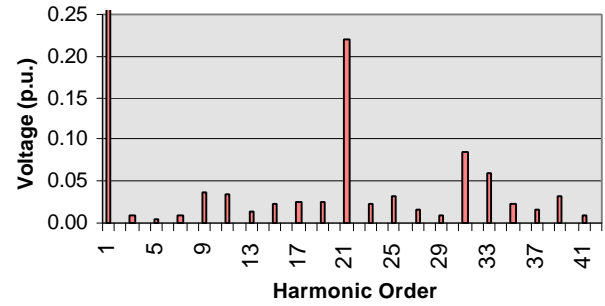
active devices and the output waveform distortion.

In Fig. 5, an example of controlling a 6-level inverter with the SH-PWM method, with $m_a = 0.8$ and $m_f = 21$, shows that the total number of switchings (active device transition from on-to-off or off-to-on), N_{sw} , during a modulation cycle, $1/f_m$, can vary between 34 and 50 depending on the phase angle of the reference. Although the waveforms are not quarter-wave symmetric for some values of f , the waveforms are always half-wave symmetric regardless of the displacement angle. Note that in a traditional two-level inverter with a single carrier wave, $N_{sw} = 42$ for $m_f = 21$ regardless of the displacement phase angle and for all values of $m_a < 1$.

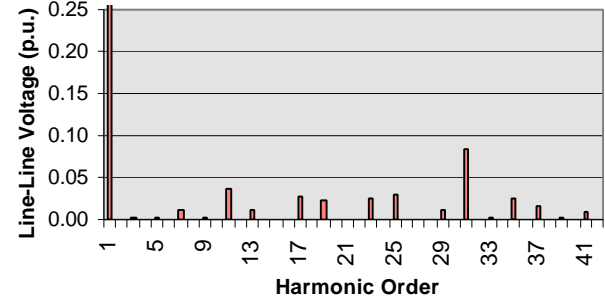
Table I shows the number of switchings at each level of the diode-clamped inverter for the examples shown in Fig. 5. The upper and lower main device pairs (S_{a1} - $S_{a'1}$, S_{a5} - $S_{a'5}$, in a 6-level inverter), in general, are switched more often than the intermediate switches for carrier-based control where each level has the same carrier frequency and all levels of the inverter are being used ($m_a > 0.6$ in a 6-level inverter). Table I also shows the line-line voltage total harmonic distortion (THD) for the 3rd through 19th harmonics for the examples shown in Fig. 5.

In Fig. 6, an example with a 6-level inverter with the SFO-PWM method and the same parameters as Fig. 5 shows that the total number of switchings can vary between 30 and 46. Table II shows the number of switchings at each level of the inverter for the examples represented in Fig. 6. Again, and even more dramatically, the upper and lower main device pairs are switched more often than the intermediate switches. Table II also shows the line-line voltage total harmonic distortion (THD) for the 3rd through 19th harmonics for the examples shown in Fig. 6.

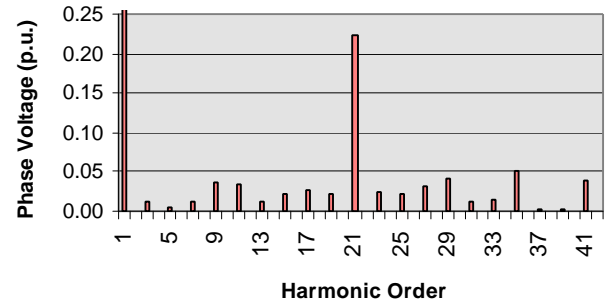
Fig. 7 shows the frequency spectrum for the unfiltered output phase voltage shown in Fig. 5(a) ($f=0.00$ rad, $N_{sw} = 34$) and Fig. 5(e) ($f=0.15$ rad, $N_{sw} = 50$). From these



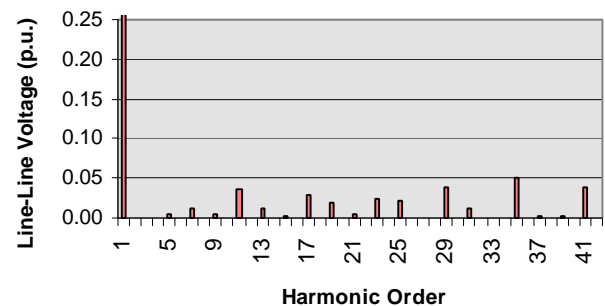
(a) V_{an} , SH-PWM, $m_f = 21, m_a = 0.8, f = 0.00$ rad, $N_{sw} = 34$



(b) V_{ab} , SH-PWM, $m_f = 21, m_a = 0.8, f = 0.00$ rad, $N_{sw} = 34$



(c) V_{an} , SH-PWM, $m_f = 21, m_a = 0.8, f = 0.15$ rad, $N_{sw} = 50$



(d) V_{ab} , SH-PWM, $m_f = 21, m_a = 0.8, f = 0.15$ rad, $N_{sw} = 50$

Fig. 7. Frequency spectrum of unfiltered output phase and line-line voltage waveforms. (a) from Fig. 5(a), (c) from Fig. 5(e).

frequency spectrums, one can see that the dominant harmonic in the phase voltage (21st) is the carrier ratio m_f . The frequency spectrums for line-line voltages are also shown in Fig. 7. One should note that no harmonic component exists at the carrier ratio in the line-line voltage.

One can also see that the only difference in the frequency spectrum for the two different displacement angles is in the magnitude of the harmonics whose order is above the carrier ratio ($m_f = 21$). The magnitude of the harmonics whose order is below the carrier ratio is nearly identical for the two cases.

An algorithm was written to count the total number of switchings during a modulation cycle with varying values of f for m_f from 9 to 39 for the SH-PWM and SFO-PWM cases for values of m_a between 0.05 and 1.35 and for $m = 6$. Some interesting observations have been gleaned from these simulations.

- 1) If the carrier ratio m_f is a multiple of 16, the phase angle between the carrier and reference generally has no effect on the total number of switchings, i.e., N_{sw} does not vary with f ($N_{sw} = 2m_f$ for this case).
- 2) If the carrier ratio m_f is even (multiple of 2), then the maximum number of switchings for a modulation cycle is $2m_f$ and $N_{sw} = 2m_f - 2j$ where $j = 0, 1, 2, 3$ (exact values for j depend on m_a and the carrier ratio m_f).
- 3) If the carrier ratio m_f is odd, then the maximum number of switchings for a modulation cycle is *greater* than $2m_f$ and $N_{sw} = 2m_f + 4j$ where $j = -2, -1, 0, 1, 2$ (exact values for j depend on m_a and the carrier ratio m_f).
- 4) The number of switchings per modulation cycle are a function of the amplitude modulation index, the carrier ratio, and the displacement phase angle. At lower amplitude modulation indices ($m_a < 0.6$ in a 6-level inverter with SH-PWM), some levels go unused [18].

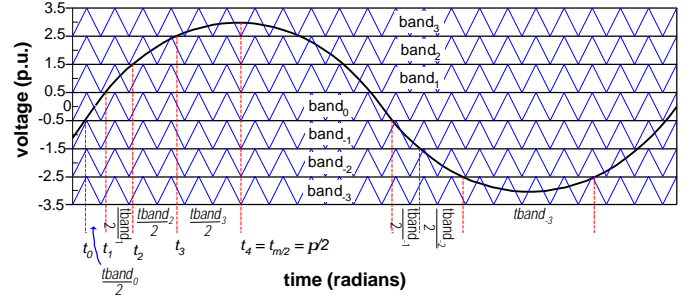
These points show a major difference between two-level PWM and multilevel PWM. In *two-level PWM*, the switching frequency is *always equal* to the carrier frequency for modulation indices less than unity. In *multilevel PWM*, the switching frequency can be *less than or greater than* the carrier frequency and is *a function of the displacement angle between the carrier set and the modulation waveform*. By choosing a phase displacement angle that minimizes the number of active device switchings for a particular m_a and m_f , switching losses can be reduced by as much as 35%, which increases the efficiency of the inverter considerably.

Another possible phase shifting method not yet explored is to shift each of the carrier bands relative to one another instead of shifting the whole carrier band set relative to the modulation waveform.

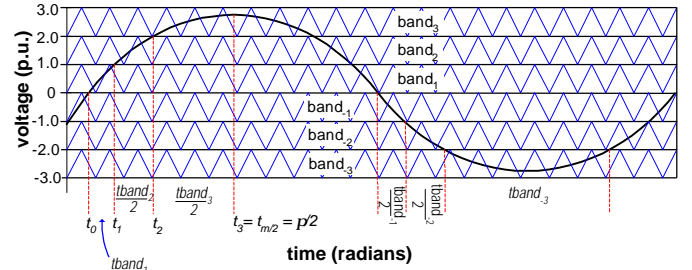
IV. VARIABLE FREQUENCY CARRIER BANDS

A method that could control or at least predict the number of switchings that occur at each level in a multilevel inverter would be advantageous. To accomplish this objective in a multilevel voltage source inverter that has a sine wave reference, knowledge of how long the reference dwells in each of the carrier time bands is required. The following section details how this information is obtained.

A. SH-PWM



(a) odd number of carrier time bands (m is even)



(b) even number of carrier time bands (m is odd)

Fig. 8. SH-PWM reference dwell times for individual carrier bands.

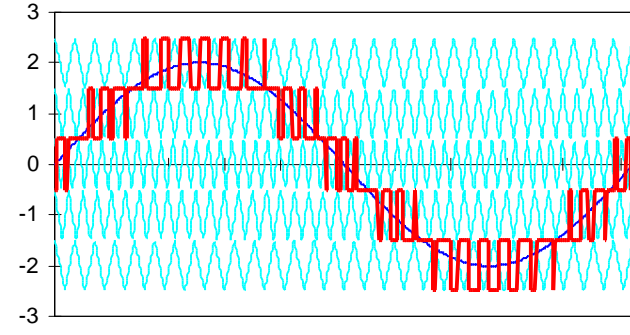
In carrier based multilevel PWM, the number of carrier bands is one less than the number of voltage levels m as shown in Fig. 8(a) for an inverter with an odd number of bands (even number of levels) and in Fig. 8(b) for an inverter with an even number of bands (odd number of levels). For a sine wave modulation (reference) waveform centered in the carrier bands (SH-PWM), the duration of time that the waveform exists during each of the bands occupied can be computed as follows. Using the amplitude symmetry of the sinewave about the time axis, the band crossing times t_n , where the reference waveform crosses from one band to an adjacent band, for bands above (or containing) the zero axis in the case that m is even) can be computed from (6).

$$t_n = \arcsin \left(\frac{2 \cdot n - \text{mod} \left(\frac{m-1}{2} \right)}{m_a \cdot (m-1)} \right), n = 0, 1, 2, \dots, \left\lfloor \frac{m}{2} - 1 \right\rfloor, \quad (6)$$

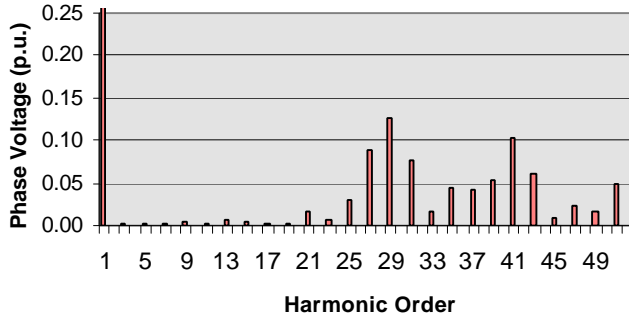
where $\text{mod}(x/y)$ is the modulus operator. Also noting that the sinewave has a maximum amplitude at $\pi/2$, this is set equal to $t_{\lfloor \frac{m}{2} \rfloor}$. From (6), the band dwell times in radians (starting at

the band adjacent to the zero axis in the case that m is odd or the band occupying the zero axis in the case that m is even) are then calculated:

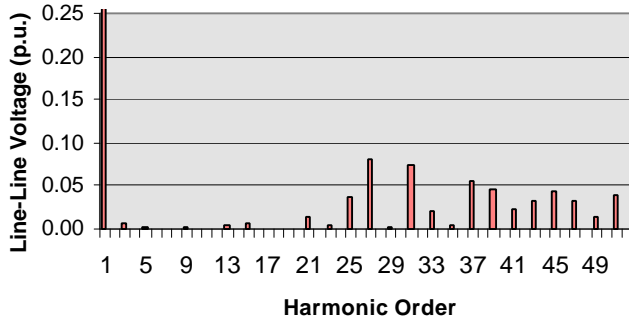
$$t_{band_n} = 2 \cdot (t_{n+1} - t_n), \text{ where } n = 0, 1, 2, \dots, \left\lfloor \frac{m}{2} - 1 \right\rfloor. \quad (7)$$



(a) carriers, reference, and inverter phase voltage waveform



(b) phase voltage harmonic spectrum



(c) line-line voltage harmonic spectrum

Fig. 9. SH-PWM where carriers have different frequencies ($m_f = 29$ for Band₂, Band₂; $m_f = 41$ for Band₁, Band₁; $m_f = 49$ for Band₀).

Because of the symmetry of the sinewave about the zero axis, the bands below the zero axis are simply

$$tband_{-n} = tband_n. \quad (8)$$

The number of switchings per modulation cycle at each level of the inverter is dependent on the carrier frequency for that level and the duration of time that the reference waveform dwells within the level's corresponding time band. If the carrier frequency for all of the levels is identical, the top and bottom levels will have many more switchings than the intermediate levels as shown in the previous section.

One method to balance the number of active switchings among the levels is to vary the carrier frequency of each band based on the time duration that the reference waveform dwells during the time band. The relationship between the

number of switchings per band, N_{sw_n} , and the frequency ratio, m_{f_n} , for each band n of an inverter is approximately given as follows:

$$m_{f_n} = \frac{p \cdot N_{sw_n}}{tband_n} = \frac{p \cdot N_{sw_n}}{2 \cdot (t_{n+1} - t_n)}. \quad (9)$$

From (9) and solutions to (7) and (8), the frequency ratio m_{f_n} for each band can be set such that each of the levels in the inverter has approximately the same number of active device switchings per cycle, i.e., N_{sw_n} is the same for all levels. Fig. 9 shows an example of the carrier waves and resulting output phase voltage from this control where N_{sw_n} has been set to 14. Harmonic spectra for the phase voltage and line-line voltage are also shown in Fig. 9.

B. SFO-PWM

To control the number of switchings in a multilevel inverter that is using SFO-PWM, different equations are needed to calculate the time duration that a sine wave reference waveform with zero sequence addition dwells in each band. Fig. 10(a) shows the carrier bands and reference waveform for multilevel SFO-PWM control. From this figure, one can see that the modulation waveform contains two segments that can be closely approximated as straight lines. Each of these line segments have a horizontal time duration of $\pi/3$ radians and a vertical amplitude of $0.75 \cdot m_a \cdot (m-1)$. Using the properties of proportional triangles from the enlarged area shown in Fig. 10(b), the following equations result:

$$\frac{t_{line}}{P/3} = \frac{\text{int}(0.75 \cdot m_a \cdot (m-1))}{0.75 \cdot m_a \cdot (m-1)}, \text{ and} \quad (10)$$

$$tband_n = tband_{-n} = \frac{t_{line}}{\text{int}(0.75 \cdot m_a \cdot (m-1))}, \quad (11)$$

$$\text{where } n = 0, 1, 2, \dots, \left\lfloor \frac{\text{int}(0.75 \cdot m_a \cdot (m-1))}{2} \right\rfloor.$$

The two "humps" at the top and bottom of the SFO-PWM modulation waveform each have a time duration of $2\pi/3$ radians. Considering the case where the two humps are wholly contained within a time band, the time duration that the modulation waveform dwells within these two bands can be given as

$$tband_{n+1} = tband_{-(n+1)} = \frac{2P}{3} + \frac{1}{2} \left(\frac{P}{3} - t_{line} \right), \quad (12)$$

where n is the maximum value used in (11).

Once the duration of dwell time for each of the carrier bands is known, (9) can be used to balance the number of switchings per modulation cycle among the levels of the inverter.

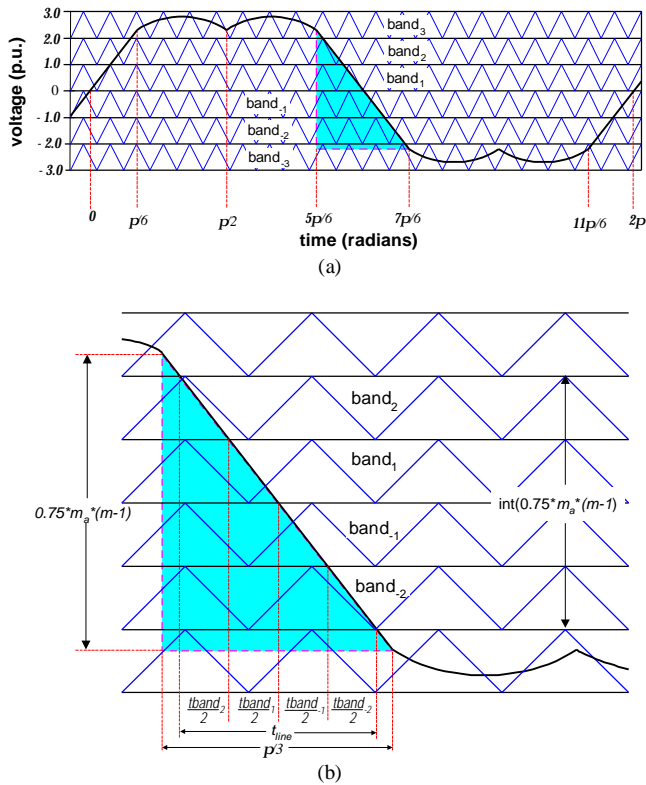


Fig. 10. Carrier bands for a 7-level inverter with SFO-PWM. (a) Modulation waveform and carrier bands. (b) Expanded view of straight segment.

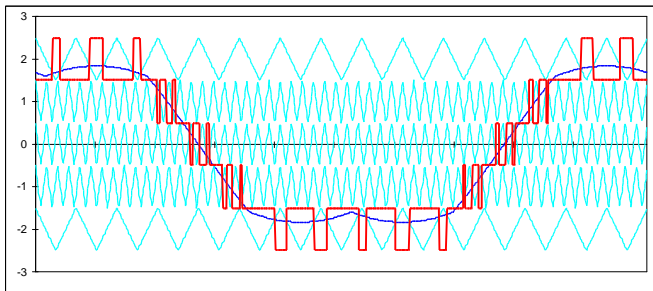


Fig. 11. SFO-PWM where carriers have different frequencies ($m_a = 0.85$, $m_f = 15$ for top and bottom bands, $m_f = 55$ for intermediate bands, $f = 0.10$).

Fig. 11 shows SFO-PWM where carriers have different frequencies for the intermediate bands ($m_f = 53$) and the top and bottom bands ($m_f = 11$) so that each level has 12 switchings per cycle. This example illustrates that balancing the switchings at each level of the inverter when using SFO-PWM requires a large difference between the frequency of the carrier bands that contain the two humps and the carrier bands that intercept only the straight line portion of the modulation waveform.

V. HARDWARE IMPLEMENTATION

A 6-level three-phase back-to-back 10 kW converter prototype, pictured in Fig. 12, has been built for operation at a line voltage of 208V for use as an adjustable speed drive for an induction motor [17-18]. The active switching devices used for the converter were 100 V, 100 A MOSFETs. Each

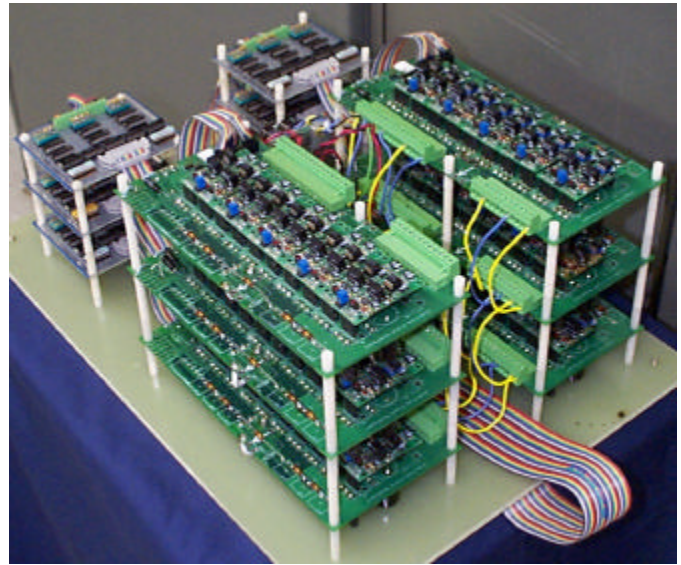


Fig. 12. Prototype 6-level, 10 kW back-to-back diode clamped converter.

internal dc level of the converter had a capacitance of 6.72 mF.

A table of switching patterns, which correspond to different amplitude modulation indices and can be optimized for the fewest switches per cycle by determining the phase displacement angle to use at each amplitude modulation index, was calculated off-line and stored in a digital signal processor controller as 1024 states per cycle. A constant voltage/frequency control technique was applied to the motor drive system. As a user interface, a potentiometer was adjusted to apply an external 0 – 3 V signal to the controller. The 0 – 3 V signal mapped directly to a 0 – 60 Hz fundamental frequency for the gate signals sent to the inverter. Also, the switching patterns corresponding to the various modulation indices were mapped from the 0 – 3V external control signal.

The inverter was used to drive a 3/4 hp induction motor and was first controlled with SH-PWM with the following parameters: $m_a = 0.95$, $m_f = 25$, and $f = 0.02$ rad. The inverter's output line-neutral voltage waveforms for all three phases are shown in Fig. 13(a), and the line-line voltage waveform V_{ab} and current waveform I_a are shown in Fig. 13(b). From the line-neutral waveforms, one can see that the top and bottom active devices in each phase switch 14 times per modulation cycle whereas the intermediate devices only switch 6 times per modulation cycle.

The prototype inverter was also controlled using carrier bands with different carrier frequencies as discussed in section IV of this paper. Specifically, the top and bottom bands had a frequency index of 17, while the next innermost bands had a frequency index of 37, and the center band had a frequency index of 43. The amplitude modulation index $m_a = 0.95$, and $f = 0.00$ for this example. Fig. 14 shows the inverter's output line-neutral and line-line voltage waveforms and current waveform when using this type of control method. All of the active devices in the inverter switch states either 8 or 10 times per modulation cycle.

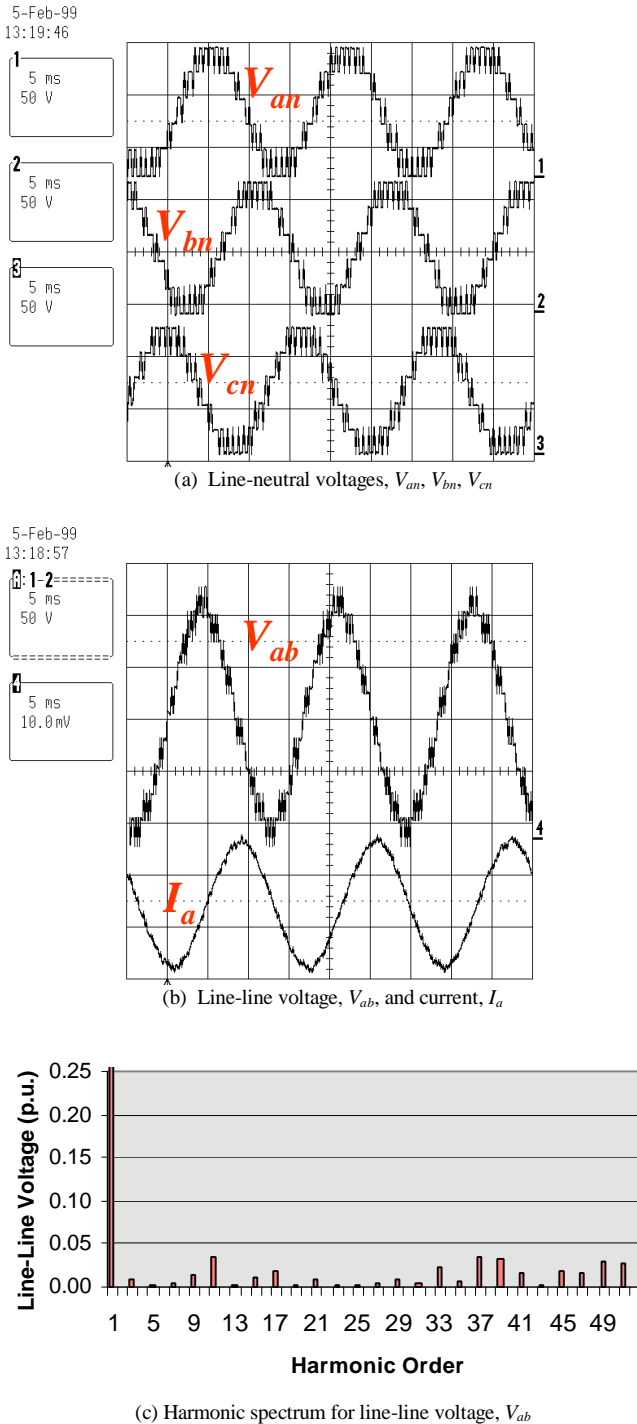


Fig. 13. Experimental voltage and current waveforms for multilevel converter controlled with same frequency carrier-bands. (SH-PWM, $m_a = 0.95$, $f = 0.02$ rad, $m_f = 25$ for all bands).

The total harmonic distortion of the line-line voltage waveform in Fig. 13(b) is 4.6%, and no individual harmonic component has a magnitude greater than 3.4% of the fundamental. The THD for the 3rd through 29th harmonic of the line-line voltage waveform in Fig. 14(b) is 8.8%. From the harmonic spectrum shown in Fig. 14(c), the dominant harmonics (15th at 5.2% and 19th at 5.4%) are adjacent to the frequency index of 17.

For this particular example, the control scheme balanced the number of device switchings but slightly increased the distortion in the inverter's output voltage. However, because a sinusoidal line-line voltage is the desired waveform for most motor drives, an algorithm can be written to determine a priori the minimum harmonic distortion for a given amplitude modulation index and desired switch utilization by combining the procedures outlined previously in sections III and IV.

VI. CONCLUSION

Multilevel carrier-based PWM offers many more degrees of freedom than traditional two-level PWM. In multilevel PWM, the switching frequency can be less than or greater than the carrier frequency and is a function of the displacement phase angle between the carrier set and the modulation waveform. By adjusting the displacement phase angle in multilevel PWM switching strategies, switching losses can be minimized for a more efficient multilevel inverter.

In traditional subharmonic PWM and switching frequency optimal PWM, the top and bottom switches are switched much more often than the intermediate devices. A novel method to balance device switchings for all of the levels in a diode clamped inverter has been demonstrated for SH-PWM and SFO-PWM by varying the frequency for the different triangle wave carrier bands.

A 6-level back-to-back diode clamped converter prototype has established that these novel carrier-based switching strategies can be used to enable better switch utilization. The need for an algorithm to combine the two procedures studied (changing the phase displacement angle and varying the frequency of the carrier bands) has been identified.

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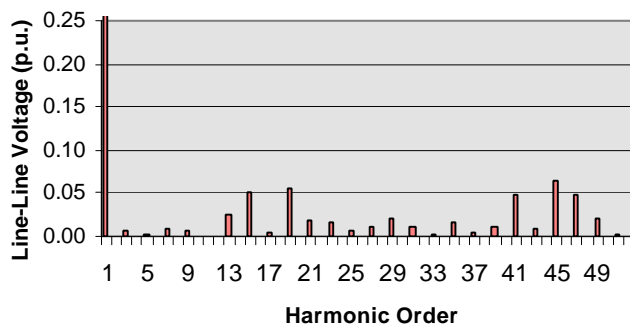
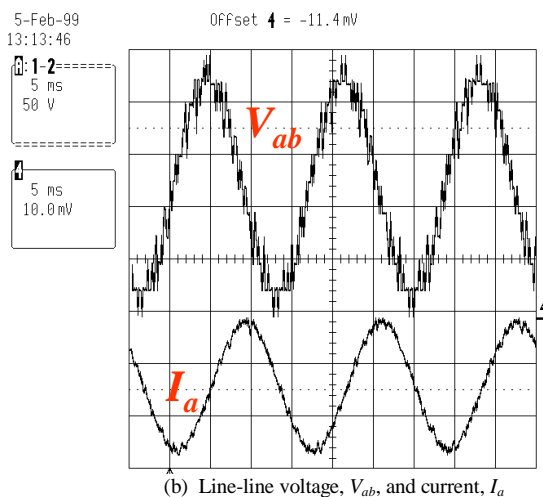
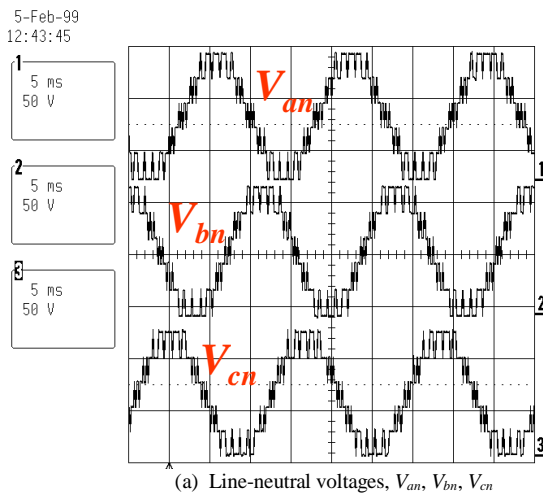


Fig. 14. Experimental voltage and current waveforms for multilevel converter controlled with variable frequency carrier-bands. (SH-PWM, $m_a = 0.95$, $f = 0.00$ rad, $m_f = 17$ for top and bottom bands, $m_f = 37$ for intermediate bands, $m_f = 43$ for center band).

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