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Novel Offline Software-in-the-Loop Simulation Technique for Modular Single-Phase Flyback Current Source Grid-Tie Inverter System

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ABSTRACT This paper proposes a novel approach in the offline Software-in-the-Loop (SIL) simulation technique to speed up the firmware development cycle of power electronics and enhance the firmware maintenance of commercial products. In the conventional SIL simulation process, Model-in-the-Loop (MIL) is always performed prior to the execution of SIL because it allows users to automatically generate C code for testing in the subsequent SIL. Furthermore, the target device can be programmed with the compiled files only if the simulation tools support specific models of control chips. In light of this, the goal to use SIL to validate firmware in early power electronics product development becomes more complex and limited due to the limited selection of simulation tools. In this paper, non-preemptive scheduling (NPS) and common firmware architecture (CFA) are explored to illustrate the integration of the application layer for implementing the proposed offline SIL. Users can directly use circuit simulation software that supports Dynamic-Link Library (DLL) to simultaneously develop source codes and verify the offline SIL process of the product. To further illustrate the practical application of the power electronics product in the microcontroller (MCU) mock model and the power stage circuit model, a single 300W power module composed of three single-phase quasi-resonant (QR) flyback current source converters connected in parallel and cascaded with an H-bridge unfolder is used as an example to execute offline SIL in the SIMULINK. Finally, a system-level experiment was conducted to validate the firmware of 16 power modules assembled in a 4.8 kW fuel cell (FC) grid-tie inverter system, which was modulated through the power management unit (PMU) and the monitoring graphical user interface (GUI).

INDEX TERMS Offline software-in-the-loop, non-preemptive scheduling (NPS), common firmware architecture (CFA), modular single-phase flyback current source inverter system.

I. INTRODUCTION

A. CONCEPT OF NOVEL OFFLINE SIL

The controller of power electronics products has evolved from analog control to microprocessor-based digital control to fulfill the advancements in function specifications, especially in the development of grid-tie inverters [1]–[4], where the programming of the digital control chips plays an important role.

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The Waterfall Model is a methodology widely used in product engineering to ensure success in product development that entails requirement evaluation, system analysis, design, implementation, testing, deployment, and maintenance.

Like a relay race, the Waterfall Model often results in insufficient time for power electronics firmware engineers to verify and debug the software embedded in the new hardware. Therefore, for power electronics software to be developed effectively or to allow testing in the early stages of product development, the SIL [7]–[13] simulation technique was extensively utilized.

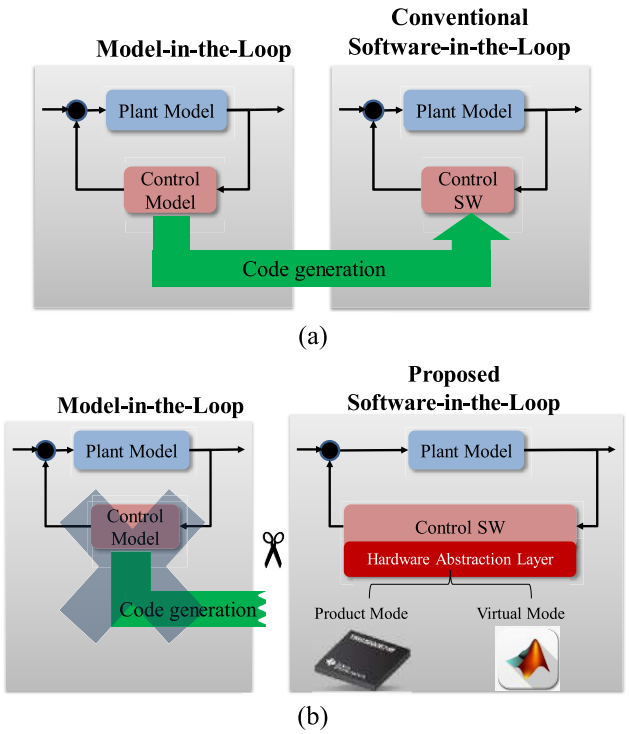

FIGURE 1. The development process of offline SIL: (a) conventional technique; (b) proposed technique.

The conventional SIL technique can be classified into two types: real-time (RT) and offline simulations.

The advantage of RT SIL simulation is that the system should sense the actual signals. Still, it requires a high-speed communication interface or specific hardware, and the cost is relatively high [7], [8].

In Fig. 1(a), the conventional offline SIL is highly dependent on MIL. The control model is established with a circuit simulation software prior to SIL implementation, then the corresponding codes for SIL are automatically generated [9], [10]. However, because the circuit simulation software does not support all MCUs in the market, the selected control chip may not generate the requirement C code during product development. This paper proposes a novel offline SIL simulation technique combined with the firmware development of power electronics without a circuit simulation software's restrictions on needing specific control chip models. Two core technologies: NPS and CFA are constructed for the proposed SIL technique, as shown in Fig. 1(b).

The NPS is a tiny scheduler, which can only be activated during the execution of SIL. Its function is to dispatch software subroutines in the firmware designed by the user based on priority level. The purpose is to mitigate the defects in behavior from the CPU in which the MCU cannot complete simulations in offline SIL due to the interrupt service routine (ISR). The CFA provides a software development platform that includes a hardware abstraction layer (HAL) to prevent the application layer from being doped with the machine codes of the MCU's peripheral modules, such as

TABLE 1. Comparisons of the SIL simulation techniques.

	RT SIL [7]-[8]	Offline SIL [11]	Proposed offline SIL
Origin of Control Software	Code generation based on the control model		Firmware design based on CFA
Development Complexity	High	Medium	Low
Development Cost	High	Medium	Low
Software Portability	Low	Low	High
Circuit Simulation Software Supporting	A specific control chip		DLL
Version Control	Low	Low	High

the pulse width modulation (PWM) and analog-to-digital converter (ADC) functions. Therefore, HAL of CFA manages all the machine codes related to the MCU peripherals. In addition, the application layer focuses on customizing codes for power electronics product applications in digital control, state machine control, protection, etc.

CFA has sufficient design flexibility to swap the implementation code and header files required by the HAL based on SIL requirements. At the same time, the offline SIL, which uses DLL, can be implemented on the circuit simulation software. Finally, the complete code based on the CFA and NPS can run on actual power electronics products or offline SIL simulation through the parameters in the application layer.

When users change different circuit simulation software or replace the control chip, the proposed CFA can still retain the application layer from the original design and keep the features of offline SIL. However, to adapt to the specifications and methods of the altered MCU peripherals, the HAL of CFA may need further expansion. The product development process often requires reconfirmation; thus, the code in the MCU is frequently modified. It is essential to evaluate the version control capabilities of each product development based on different SIL technologies. In the proposed approach, the critical assets are codes in plain text format; thus, we can efficiently execute the version control. In contrast to the conventional SIL, which runs on automatic code generation, the circuit simulation software uses visual graphic design to construct its control model, and it is hard to clarify modifications of the control model in non-text format.

B. CASE STUDY: A MODULAR INVERTER SYSTEM

A modular inverter system has been previously published in [14], as shown in Fig. 2; nevertheless, the literature did not further explore SIL technology for such a system.

The novel SIL simulation technology can be applied to firmware programming and the execution of offline SIL, which can ensure sufficient time for the embedded software to be verified and debugged.

In Fig. 2(a), a single 300W power module used in FC power generation is discussed, and it is established in the SIMULINK development environment to validate the proposed SIL simulation technique. Subsequently, an experiment was conducted in which 16 power modules assembled to be

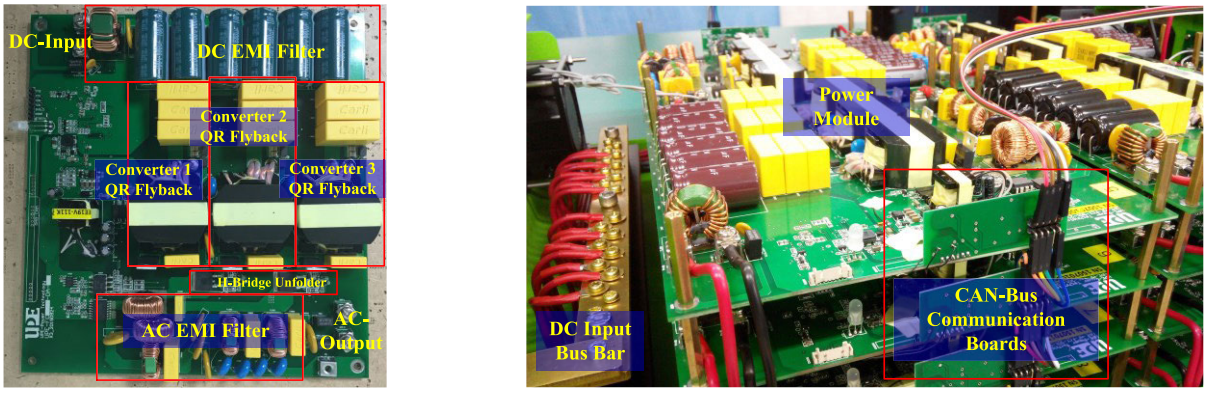

FIGURE 2. Proposed FC grid-tie inverter system: (a) single power module; (b) modular assemblage.

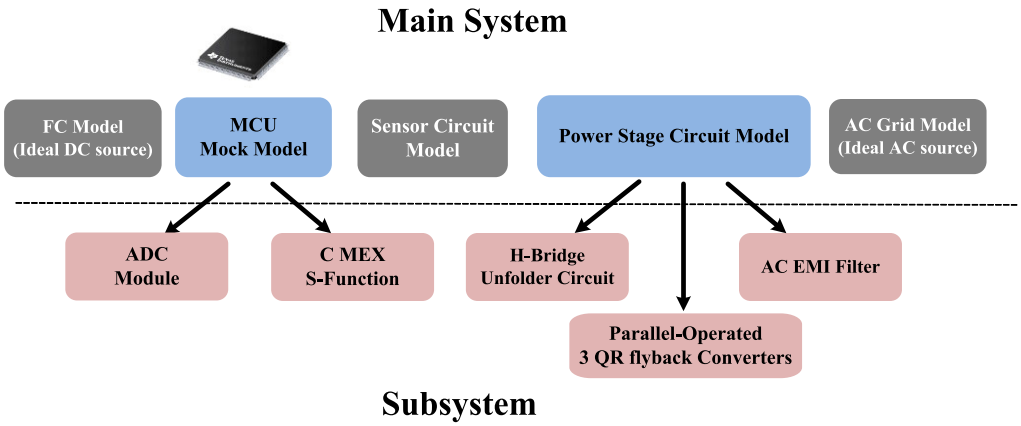

FIGURE 3. The correlation diagram of the simulation model in SIL.

a 4.8 kW grid-tie FC inverter system, as shown in Fig. 2(b), controlled through the PMU and GUI. Fig. 3 shows a complete model of the 300W power module, including the FC model, MCU mock model, sensor circuit model, power stage circuit model, and grid model.

II. PROPOSED NOVEL OFFLINE SIL SIMULATION

Two core technologies: the non-preemptive scheduling (NPS) and the common firmware architecture (CFA) are discussed in this section. After importing the proposed offline SIL simulation technology, it set two compilation modes through the application layer: product mode (PM) and virtual mode (VM).

In PM, the complete source code based on the CFA is compiled by the compiler using a specific control chip, then written to the target chip. A scenario similar to the feedback control system is described in Fig. 4(a). The PWM signal of the control chip drives the power switch to initiate the power stage circuit for energy conversion. The feedback signal, voltage, or current measured by the sensor circuit, are scaled to an acceptable range on the ADC pin. Finally, feedback control is executed through the digitalized compensator. For example, it can also apply a similar control strategy to the speed control of an electric fan.

As shown in Fig. 4(b), the purpose of VM is to verify the feasibility of the customized codes of the application layer and check for overall design flaws during offline SIL simulations. Therefore, products that involve power stage circuits, sensor circuits, and other plants should be modeled first with the circuit simulation software. Then, the MCU mock model is represented by DLL, which is compiled from the complete source code with NPS of the application layer of the CFA.

A. NON-PREEMPTIVE SCHEDULING (NPS)

In PM, it classifies the codes into ISR ($Periodic\_\_ISR_y$, $NonPeriodic\_\_ISR_z$) and non-ISR ($Non\_\_ISR_x$) that are associated with specific interrupt conditions. Then, the CPU completes the non-ISR software process and polling as the hardware device sends out an ISR request to interrupt the active process. When ISR is complete, the previously interrupted process is resumed. The flow chart is shown in Fig. 5(a).

When switching to the VM in circuit simulation software, the frequent execution of the DLL to simulate the behavior of the CPU may lead to a longer simulation time. Therefore,

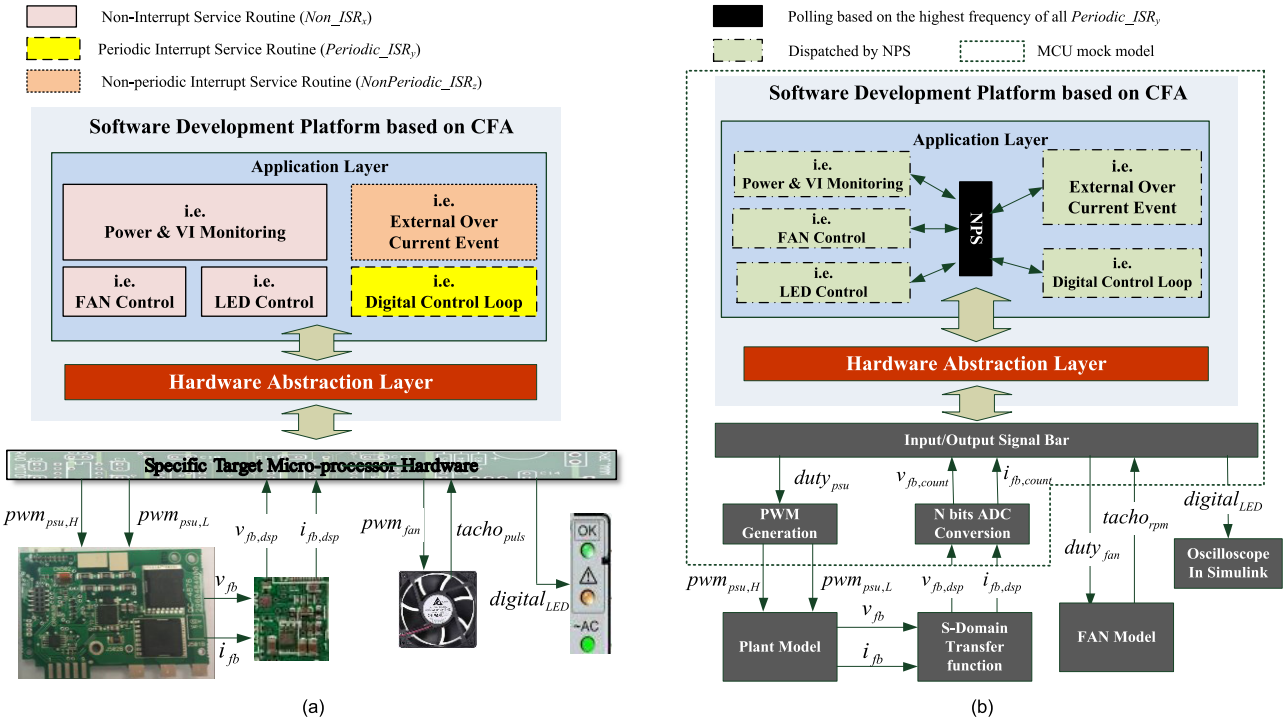

FIGURE 4. The block diagram of the proposed software development platform based on CFA and NPS: (a) PM; (b) VM.

the NPS is designed to be active in the VM to handle the activities of the ISR. Its polling speed is based on the highest design frequency of all the periodic ISRs in the PM. The scheduler can dispatch all the software routines in periodic ISRs, non-periodic ISRs, and non-ISRs, as shown in Fig. 5. Fig. 5(b) is draw based on two assumptions: (1) the polling frequency of NPS divided by the design frequency of all periodic interrupts are integer; (2) NPS execution time is within $T_{SIL}(T_{SIL} = 1/f_{SIL})$.

As can be seen that from Table 2, the execution timing of non-periodic ISR and non-ISR is different under PM and VM. For non-periodic ISRs, if the timing requirement is not extremely sensitive to the practical application case, the behavior of the control chip can still be simulated effectively. Whereas non-ISRs often have lower time accuracy requirements, as seen in the control of light-emitting diode (LED) or fan speed with lower control bandwidth.

B. COMMON FIRMWARE ARCHITECTURE (CFA)

The proposed CFA created a HAL that is suitable for the embedded system and offline SIL simulations, as well as an application layer that possesses reusability and portability to achieve the following: (1) same software development platform that can be used in both PM and VM; (2) increase in the flexibility of product software development to cope with the potential replacement of the target device. In order to achieve such functionality, the required

TABLE 2. Execution timing of periodic ISR, non-periodic ISR, and Non-ISR under PM and VM.

	EXECUTION TIMING	
	PM	VM
PERIODIC ISRs (Non_ISR_x)	Consistent due to the same execution frequency	Based on the highest design frequency of all the periodic ISRs
Non-periodic ISRs ($Periodic\_ISR_y$)	Dependent on event driven	
Non-ISRs ($NonPeriodic\_ISR_z$)	Infinite loop to poll it if CPU is not busy on dealing interrupt service routine	

HAL needs to cover the peripherals of the control chip that may be used in power electronics applications as shown in Figure 6.

The parameters in the header file required configurations include: (1) the current operating mode; (2) the manufacturer, compiler, and model of the control chip used in the PM; (3) the circuit simulation software and compiler used in the VM. As shown in Fig. 7, it set the operating mode to PM, the control chip is a TI TMS320F28035, and the compiler is a C2000. When the operating mode is switched to VM, the offline SIL simulation is executed in the S-function of the SIMULINK, and the compiler is a MinGW-w64.

To understand how to use the HAL module, ADC peripheral is used as an example; its structure is shown in Fig. 8. The specific implementation of the CFA's application layer will include the header cfa_hal_config.h, which allows the CFA to import cfa_adc_28035.c and cfa_adc_28035.h

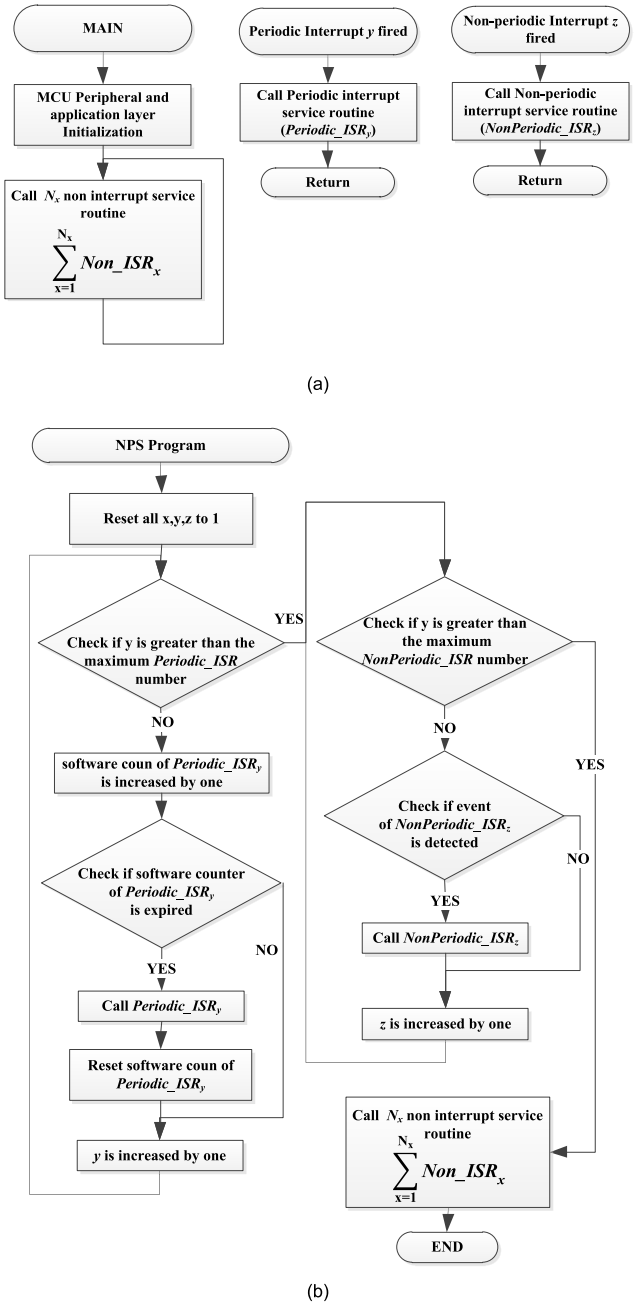

FIGURE 5. Flow chart of the application layer: (a) PM; (b) VM.

under PM. Furthermore, when users execute offline SIL simulation, operation mode should be switched to VM, which allows the CFA to import the cfa_adc_simulink.c and cfa_adc_simulink.h that are compatible with the SIMULINK. The application layer must first declare the variable as "ADC output handle" to initialize the adc_handle_t structure as shown in Fig. 9. Then, the application layer can access the ADC peripherals of the control chip through the "ADC output handle".

Based on the same concept, when the application layer uses other peripheral modules of HAL, data access must also pass through the designated "xx handle". Using control

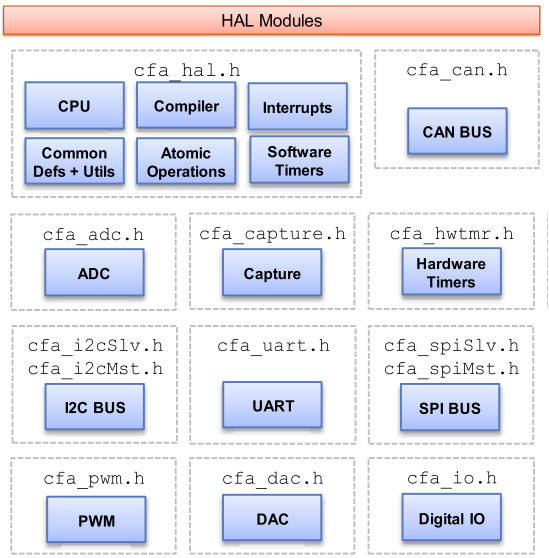

FIGURE 6. The peripheral module of the HAL.

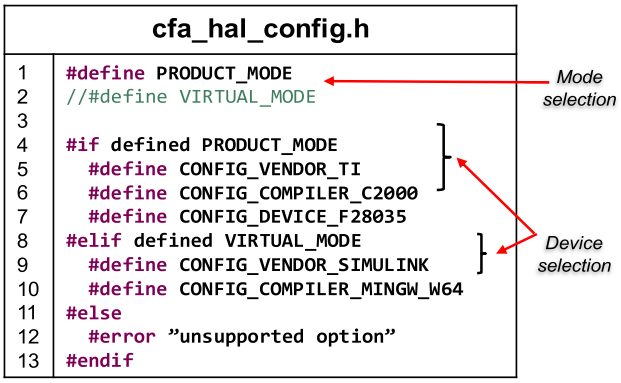

FIGURE 7. The setting of CFA parameters.

chips from different manufacturers can alternate the utilization strategy. Therefore, the components and design methods corresponding to "xx handle" might be slightly adjusted. For example, the adc_handle_t structure is defined, as shown in Fig. 9, which references the ADC chapter of the DSP TMS320F28035 technical reference manual [15].

During the operating process, the application layer will call the subroutine of the peripheral modules of the HAL to obtain the ADC channel value through adc_GetValue When comparing PM and VM, the adc_GetValue() subroutine designs are different, as shown in Fig. 10. In the PM, the adc_GetValue() subroutine refers to the register of the control chip; in the VM, the adc_GetValue() subroutine refers to the C MEX S-Function.

III. 4.8 kW GRID-TIE FC INVERTER SYSTEM

Fig. 11 shows the block diagram of the modular inverter system comprised of three units as follows [14]:

(1) Energy generation unit (EGU): A low-voltage, FC powered DC source.

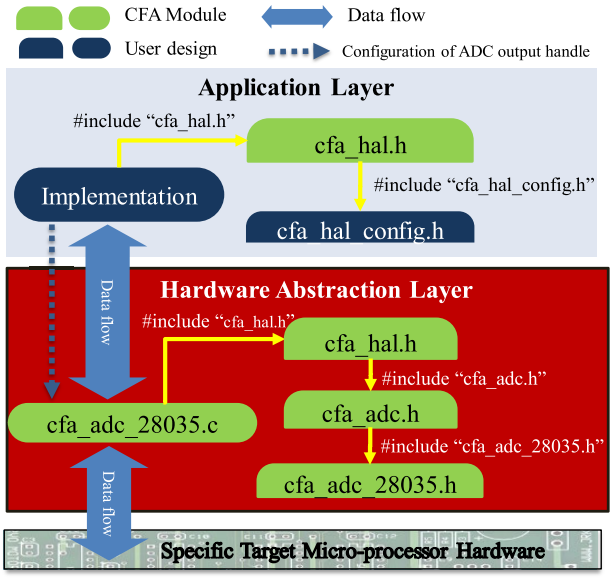

FIGURE 8. Internal block diagram of CFA.

cfa_adc_28035.h

```
1  /**
2   * ADC output handle.
3   */
4  typedef struct
5  {
6      /**< ADC converter. */
7      adc_converter_t *adc_converter;
8
9      /**< ADC SOC mask. SOC/ADC channel that will be scanned.
10      * Used to start conversion.
11      * Initialize using masks defined by `adc_soc_mask_t` */
12     uint16_t        soc_mask;
13
14     /**< ADC interrupt source mask.
15      * Interrupt sources to enable on interrupt enable.
16      * Initialize using masks defined by `adc_int_mask_t` */
17     uint16_t        int_mask;
18
19     /**< ADC interrupt 1 and 2 enable.
20      * Interrupt sources to enable on interrupt enable.
21      * Initialize using masks defined by `adc_int_1n2_en_mask_t` */
22     uint16_t        int_1n2_en_mask;
23
24      /**< ADC interrupt 3 and 4 enable.
25       * Interrupt sources to enable on interrupt enable.
26       * Initialize using masks defined by `adc_int_3n4_en_mask_t` */
27     uint16_t        int_3n4_en_mask;
28
29 }adc_handle_t;
```

FIGURE 9. Structure of ADC output handle.

(2) Power management unit (PMU): It uses an MCU MK64FN1M0VLL12 as the core for the power distribution of the inverter system, system monitoring, failure detection as well as communication between the inverter system and the monitoring GUI.

(3) Power conversion unit (PCU): This unit converts the DC power of the FC device to the AC grid. To increase power scalability, hardware utilization, and reliability, the designed PCU connects multiple power modules in parallel, allowing users to select the required number of power modules based on various power requirements.

A. OPERATING PRINCIPLES OF THE POWER MODULE

The single grid-tie inverter module of the PCU is shown in Fig. 12(a), which consists of three single-phase QR flyback current source converters connected in parallel and cascaded with an H-bridge unfolder [14]. In Fig. 12(a) and (b), it can see that the primary-side switch of the flyback current source converter is regulated by variable frequency PWM signals to control the magnetizing current of the transformer directly. As to the waveforms of the primary-side current, it follows a rectified sine signal. The basic operating concepts of the flyback converter are as follows: when the primary-side switch is turned off, the secondary-side output diode is turned on, and energy is transferred to the output through an H-bridge unfolder and the electromagnetic interference (EMI) filter.

The full-bridge circuit (S_{H1}, S_{H2}, S_{L1}, and S_{L2}) is an H-bridge unfolder for the rectified output voltage of the flyback that controls the direction of power flow to the AC grid. S_{H1} and S_{L2} are turned on during the positive half-wave period of the AC grid; switches S_{H2} and S_{L1} are turned on during the negative half-wave period of the AC grid. Due to the H-bridge unfolder is only operated at AC line frequency; therefore, it eliminates the switching loss, and the overall inverter architecture can be regarded as a single-stage topology [16]–[19].

Fig. 12(b) shows the typical waveforms of the QR flyback converter. The primary-side power switch conduction is always initiated by sensing a zero current signal to execute the boundary conduction mode (BCM). With BCM, the converter can achieve the natural ZCS feature of the secondary-side output diodes, thereby reducing EMI noise [16]–[18].

B. DIGITAL CONTROL ARCHITECTURE

As shown in Fig. 11, the digital control loop implemented in the control chip includes the following three parts:

1) Averaged current controller of the FC current

Using Eq. (1) and Eq. (2) as following, we can identify the averaged current loop of the FC power source (i.e., DC side input current).

$$u(t) = K_P e(t) + K_I \int_0^t e(t)dt \tag{1}$$

$$e(t) = I^*_{dc,M_x}(t) - I_{dc,M_x}(t) \tag{2}$$

According to Eq. (2), the erro $re(t)$ is the difference between $I^*_{dc,M_x}(t)$ and $I_{dc,M_x}(t)$. The averaged value I_{dc,M_x} of FC current feedback $i_{fc,M_x}(t)$ is obtained through two cascaded filters, a second-order notch filter and a first-order low-pass filter.

Besides, the FC current command I^*_{dc,M_x} is provided by the PMU and limited by the internal upper limit I_{dc_limit,M_x}, as Eq. (3).

$$I_{dc\_limit,M_x}(t) = \min(I_{dc,max}, \frac{P_{dcmax}}{V_{dc,M_x}(t)}) \tag{3}$$

2) Command of the primary-side magnetizing current

cfa_adc_28035.c

```
/** Get the value of a specific ADC channel
 *
 * @input:  Channel specific adc channel where conversion came from
 * @output: ADC value
 *
 **/
static inline adc_value_t adc_GetValue(adc_handle_t *h, adc_channel_t channel)
{
    /* 12 bit resolution, shift left by 4 bits to fully left justified */
    return ((&(h->adc_converter->adc_result_regs->ADCRESULT0))[channel] << 4);
}
```

(a)

cfa_adc_simulink.c

```
/** Get the value of a specific mock ADC channel
 *
 * @input:  Channel specific adc channel where conversion came from
 * @output: mock ADC value
 *
 **/
static inline adc_value_t adc_GetValue(adc_handle_t *h, adc_channel_t channel)
{
    /* Get mock ADC data of 12 bit resolution from S-function subroutine call */
    return (adc_value_t)sil_GetAdcValue(channel);
}
```

(b)

FIGURE 10. Coding under different modes: (a) PM; (b) VM.

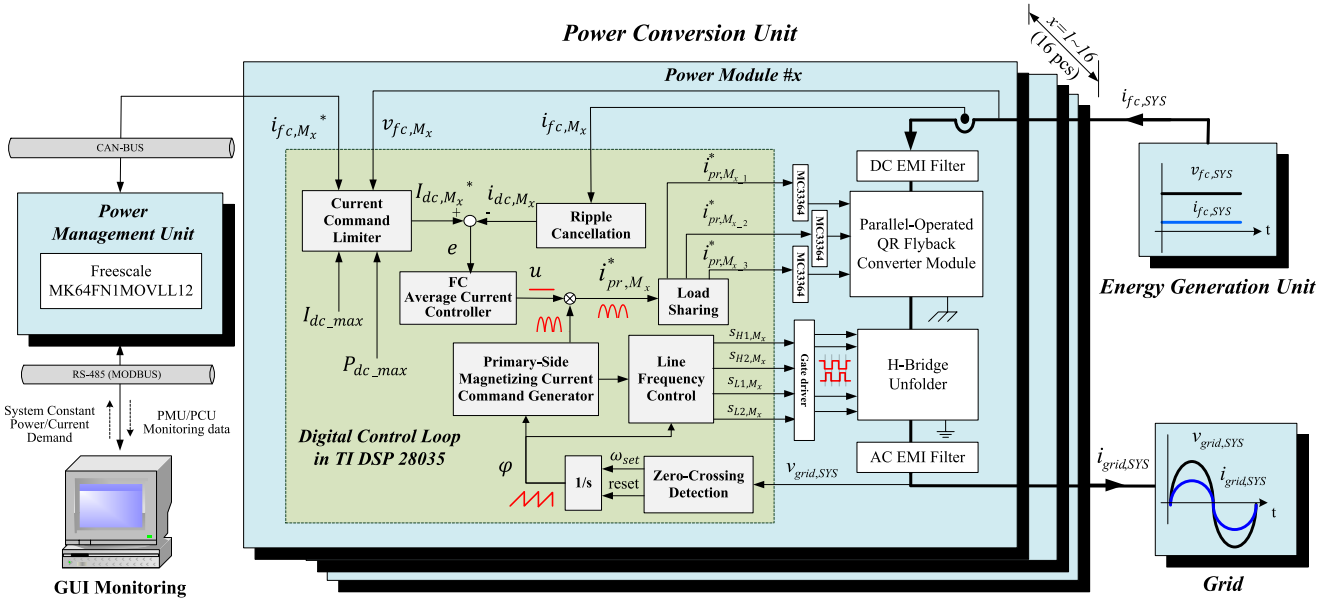

FIGURE 11. Block diagram of a digitally controlled modular FC grid-tie inverter system.

The command of the primary-side magnetizing current can be obtained from Eq. (4) [14].

$$i^*_{pr,M_x}(t) = 2i^*_{grid,M_x}(t)\left(\frac{v_{grid,SYS}(t)}{V_{fc}} + N\right) \tag{4}$$

where, N is turn ratio of flyback transformer.

Furthermore, based on the assuming conditions: (1) grid voltage $v_{grid,SYS}$ and current i^*_{grid,M_x} are in phase and ideal sinusoidal waveforms; (2) the FC voltage V_{fc} and the grid voltage $v_{grid,SYS}$ are set to be the nominal value. Therefore, Eq. (4) can be simplified and established as a lookup table $LUT_{QR,i_{pk}}(\varphi)$ for quick queries.

$$i^*_{pr,M_x}(t) = u(t)\, LUT_{QR,i_{pk}}(\varphi) \tag{5}$$

The phase signal φ is obtained by zero-cross detection of grid voltage $v_{grid,SYS}$ and its range is 0 to 2π. Since a

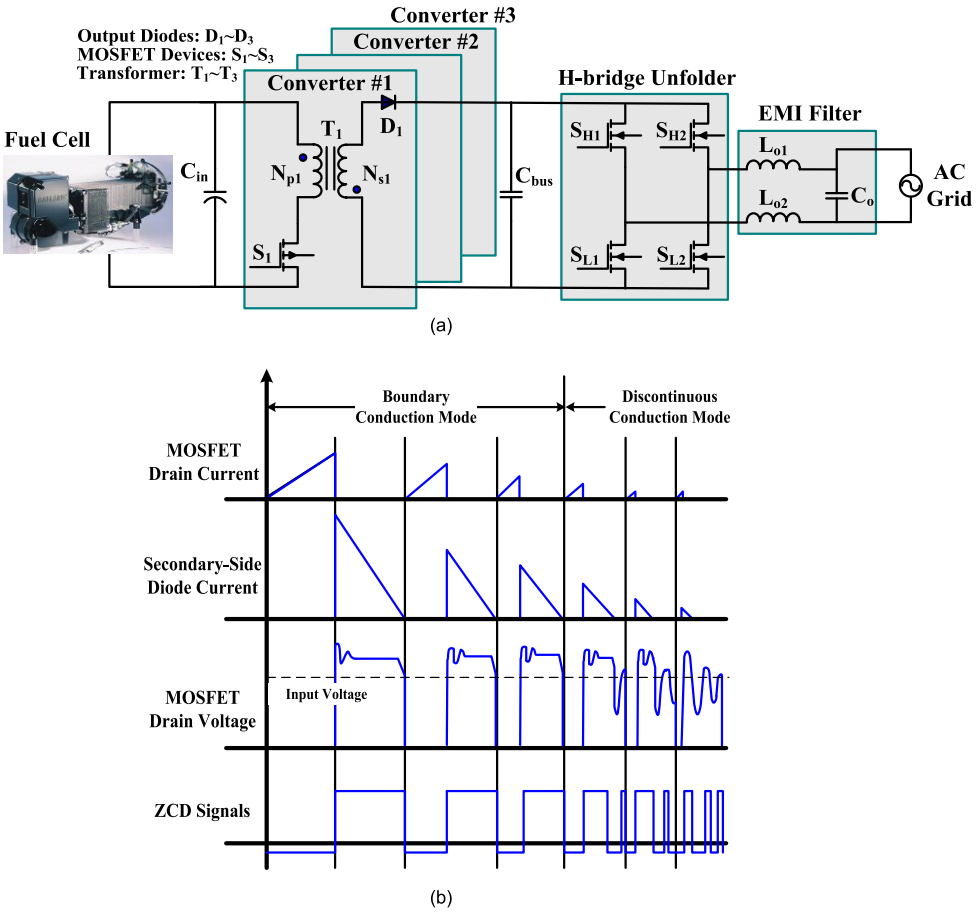

FIGURE 12. Single-phase power module: (a) circuit architecture; (b) typical waveforms.

single power module is composed of three QR flyback current source converters connected in parallel, the final primary current command ($i^*_{pr,M_{x\_1}}$, $i^*_{pr,M_{x\_2}}$, $i^*_{pr,M_{x\_3}}$) can be obtained when divided by 3.

$$i^*_{pr,M_{xy}}(t) = \frac{i^*_{pr,M_x}(t)}{3} \tag{6}$$

3) Switching signal generator of H-Bridge unfolder

Based on the phase signal φ of the grid voltage, while considering the dead time, the switching signal generator can produce the driving signals to drive the H-Bridge unfolder (S_{H1,M_x}, S_{H2,M_x}, S_{L1,M_x}, S_{L1,M_x}) at the AC side to achieve line frequency switching.

IV. SIMULATION MODEL DESIGN OF A SINGLE POWER MODULE

Fig. 13 shows the simulation block diagram of a single power module of the modular grid-tie inverter system based on offline SIL, which includes MCU mock model, power stage circuit model, FC model, grid model, and sensor circuit model. The FC model and the grid model are represented by the ideal DC voltage source and AC voltage source.

In addition, the multiple feedback signals of the power stage circuit model, such as FC current and grid voltage, are connected to the MCU mock model through the sensor circuit model and the sensor circuit model is based on the s-domain transfer function of the actual sensor circuit.

A. MCU MOCK MODEL

The MCU mock model includes a 12-bit ADC model and C MEX S-function. The C MEX S-function aims to generate a MEX file compiled by the MinGW-w64 compiler in MATLAB. In addition, the compiler links to the complete source code based on the proposed SIL under VM.

B. POWER STAGE CIRCUIT MODEL

As shown in Fig. 12(a), the power stage circuit model can be divided into three subsystems as shown in Fig. 14: (1) three QR flyback converter circuit models connected in parallel; (2) H-Bridge unfolder; (3) AC EMI filter. In practical applications, the flyback converter utilizes a variable frequency controller (MC33364D2) to make the converter operated in BCM. The function of MC33364D2 can be simplified and realized by the RS flip-flop, a current comparator, and multiple logic gates. Therefore, the model of the flyback converter with BCM control can be made, as shown in Fig. 15.

The RS flip-flop statues and the corresponding gate drive signals are shown in Table 3. As shown in Fig. 16(a), three waveforms are presented during the grid cycle: the

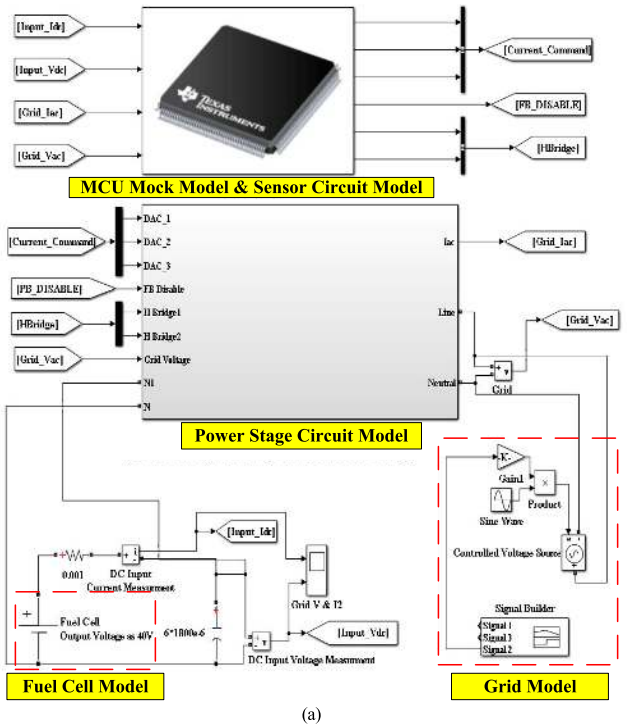

FIGURE 13. Simulation block diagram of the single power module based on offline SIL.

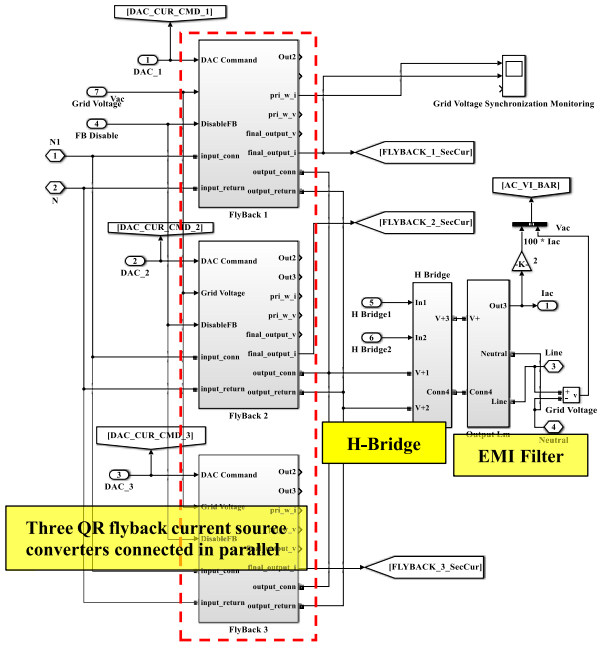

FIGURE 14. Power stage circuit model.

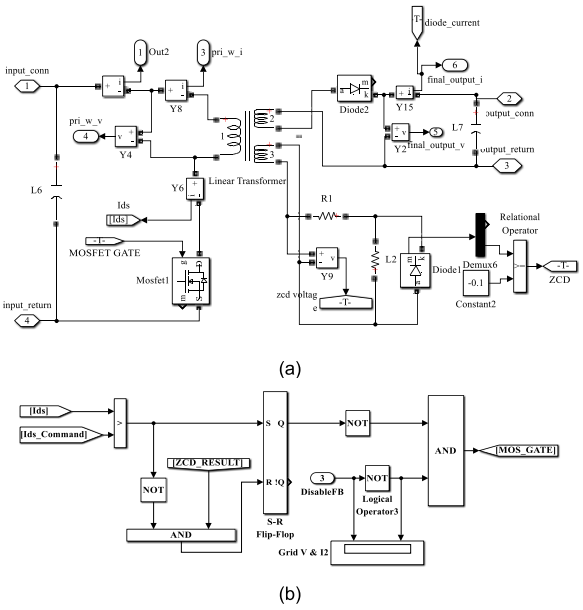

FIGURE 15. Subsystem model of the QR flyback converter: (a) circuit model; (b) BCM control block diagram.

TABLE 3. RS statues and gate drive signals in BCM.

State	S	R	Q_{next}	MOS_GATE $_{next}$
1	0	0	Q	MOS_GATE
2	0	1	0	1
3	1	0	1	0

primary-side magnetizing current command, the primary-side magnetizing current feedback, and the secondary-side diode output current. To show the relationship between the RS flip-flop statuses and the current waveform more clearly, Fig. 16(b) is the zoom-in view in the switching cycle, and the RS flip-flop value is also observed.

According to Table 3, the converter operations of each state can describe as below.

State 1: The primary-side switch remains constant, and the stored energy of magnetizing inductor is transferred to the secondary side. As the magnetizing current produces a negative slope change, the auxiliary winding voltage of the flyback transformer is negative, where the ZCD output is 0.

State 2: The energy of magnetizing inductance is completely released. The induced voltage of the auxiliary winding is 0, where the ZCD output is 1. The primary-side switch is turn on and the magnetizing current produces a positive slope change, which recharges the magnetizing inductance.

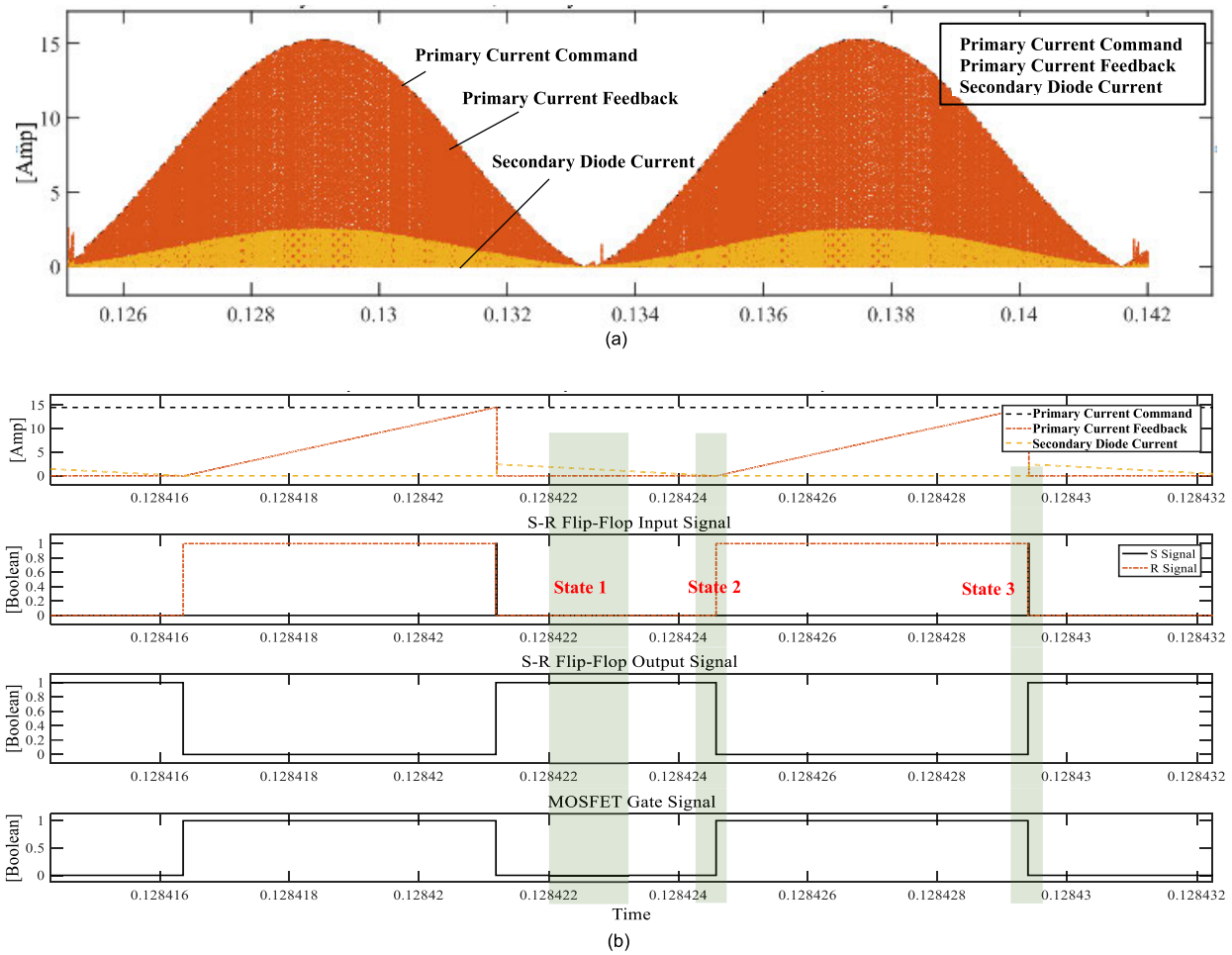

FIGURE 16. Simulation waveforms of the single-phase inverter module: (a) current waveforms during the time span of the grid cycle; (b) current waveforms and control signal during the time span of the switching cycle.

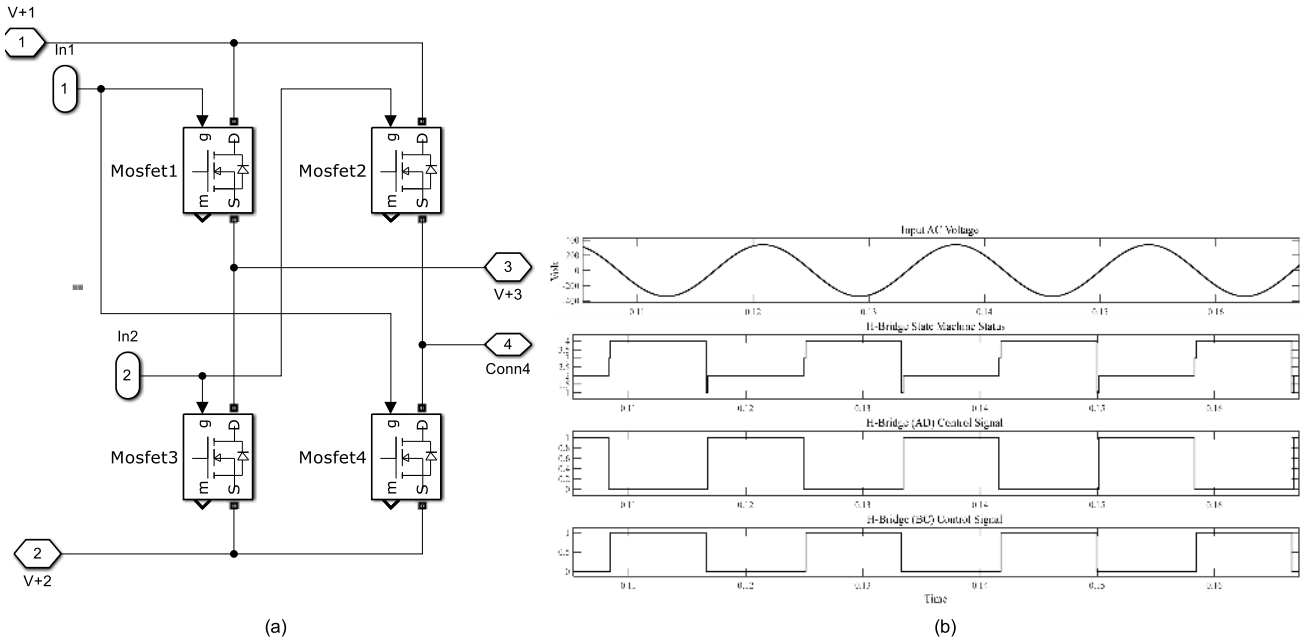

FIGURE 17. Simulation waveforms of the H-bridge unfolder: (a) circuit model; (b) grid voltage feedback and control signals.

TABLE 4. Comparisons of the operating sequences of the h-bridge switch.

State Variable	In1	In2	Power Flow
1	Off		Dead time
2	On	Off	Positive half-cycle
3	Off		Dead time
4	Off	On	Negative half-cycle

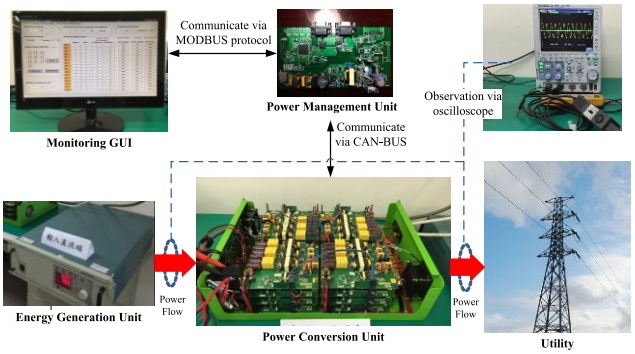

FIGURE 18. Experiment setup of the modular FC grid-tie inverter system.

State 3: The primary-side magnetizing current reaches the primary current command value, which leads the output of the current comparator from 0 to 1 and then turns off the primary-side gate signal. As the current comparator output returns to 0, an output pulse signal is formed.

Fig. 17(a) shows that the H-bridge unfolder model consists of four power switches, namely Mosfet1∼ Mosfet4. There are two gate driver signals for switching the H-bridge unfolder. The gate driver signal In1 is connected to Mosfet1 and Mosfet4; the gate driver signal In2 is connected to Mosfet2 and Mosfet3. The grid voltage, the internal state variables, and both of the gate driver signals are shown in Fig. 17(b). The purpose of the internal state variables is to control the gate signal of the H-bridge unfolder with dead time control.

V. EXPERIMENTAL RESULTS IN PRODUCT MODE

The purposed offline SIL can not only perform simulation, but also be used for firmware development of practice power electronics products. The required setting step is to set the operating mode in the cfa_hal_config.h header to PM, and then reprogram the MCUs of all power modules in the PCU.

Fig. 18 illustrates the experiment setup of the developed modular FC grid-tie power generation system, and Table 5 presents the specifications of the system. In the experiment, 16 grid-tie power modules with 300W power rating based on three QR flyback current source converters were assembled to form the modular single-phase inverter system that provided 4.8 kW of grid-tie power. The PMU collected RT power data of all the modules through the controller area network bus (CAN-Bus). The developed monitoring GUI was used to issue commands to the PMU, regulate the DC current command, and thereby generate power fed to the AC side.

Fig. 19(a) and Fig. 19(b) respectively illustrate the DC current commands (52A and 104A) issued through the monitoring GUI and the corresponding waveforms of the grid voltage and grid current.

TABLE 5. Specifications of the proposed grid-tie inverter system.

Parameter	Specification	
DC Side		
Input Rated Power	4800W	
Input Adjustable Power	0~4800W	
Input Voltage Range	25~65V	
AC Side		
Maximum Output Power	4300W	
Output Nominal Voltage	240V	
Output Voltage Brown-In	221V~254V	
Output Nominal Frequency	50Hz/60Hz	
Output Frequency Brown-In	**50Hz Range**	**60Hz Range**
	49.4Hz~50.4Hz	59.5Hz ~ 60.5Hz
Power Factor	>0.95	
THD	<5%	
Peak efficiency	>91% for the overall system	

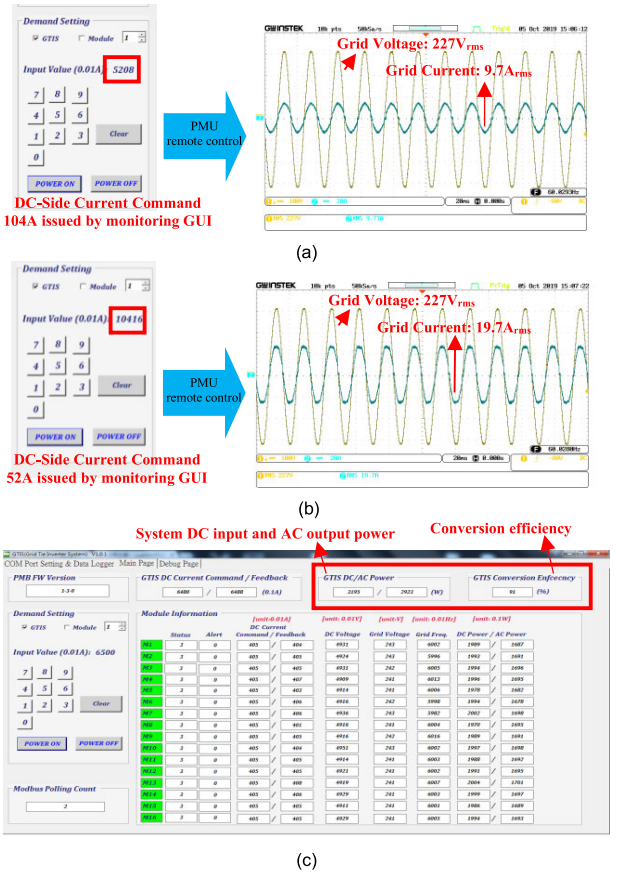

FIGURE 19. GUI displays of the implemented system performance: (a) grid-side waveforms corresponding to DC current command of 52A; (b) grid-side waveforms corresponding to DC current command of 104A; (c) The monitoring GUI under the command of DC current of 65A.

The results verified that system users could regulate the current transmitted to the AC grid through the demand setting panel, a monitoring GUI. As shown in **Fig. 19(c)**, the GUI of the proposed system collected the power data of overall power modules in the grid-tie power generation system.

According to the measuring in Fig. 19, the testing conditions and the experiment performance of the proposed

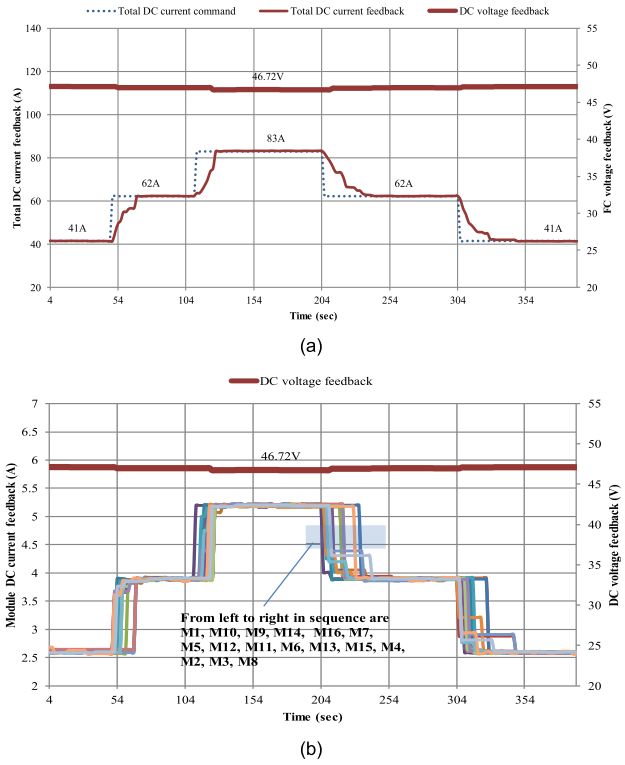

FIGURE 20. Power data recorded by the data logger of the monitoring GUI: (a) total DC current; (b) DC current of power module.

modular FC grid-tie inverter system implementation are described as follows:

(1) The voltage and frequency of the mains electricity (AC grid) are 235Vrms and 60Hz, respectively; and

(2) The voltage of the DC power supply is 50 Vdc, approximately 3 kW of AC power can be injected into the grid to achieve a system conversion efficiency of 91% under the DC current command of 65 A.

In addition, the monitoring GUI has the feature of the data logger, as shown in the Fig. 20. As shown in Fig. 20(a), when the user increases the DC current command of 21 A, the GUI issue a current sharing command to each power module through the PMU, and the data collection process is asynchronous and takes time.

According to the experimental results in Fig. 20(a) and Fig. 20(b), the functionality of the DC control loop of the 4.8kW system has been verified, and the firmware design of each module in the PM mode has also been confirmed to work normally.

VI. CONCLUSION

In the conventional SIL simulation technique, the control code is automatically generated from a pre-built controller model, and the selected simulation environment must support a specific control chip. In view of this, this paper proposes a software development platform based on CFA and NPS, which can be used in: (1) PM, the firmware design framework used to control the chip during product development; (2) VM, a novel offline SIL simulation technique that can bypass the limitations that the traditional process entails. The NPS proposed in this paper enables the firmware code to execute ISR in a non RT system simulation software environment through specific scheduling. In addition, the designed HAL of CFA can retain software of application layer portability even with different control chips. Overall, the research results of this paper can be applied to most of the circuit simulation software that supports DLL, at the same time, eliminate the need to use specific high-cost hardware circuits. It serves as a platform that allows corporations to save costs on research and development or educational programs. As a case study, the proposed concept is used in a modular 4.8kW grid-tie FC inverter system to design a power stage circuit model and a control chip model. The grid-tie power module is based on the three QR flyback current source converters in parallel and cascaded with an H-bridge unfolder. In addition, the PMU and monitoring GUI are used to verify the controllability of the average current of the DC side and the grid connection performance of the AC side.

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