Novel Robust Methodology for Controller Design Aiming to Ensure DC Microgrid Stability Under CPL Power Variation

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ABSTRACT In recent years, dc microgrid (MG) is increasing rapidly in electric power grids and other isolated systems, integrating more efficiency and suite better some of the renewable energy sources, storage units, and dc loads. However, dc MG stability analysis becomes a challenge when constant power loads (CPLs) are applied to dc bus, which introduces destabilizing effects in the system due to its negative impedance characteristics. This paper presents a novel robust controller, based on linear programming based on the Chebyshev theorem as a robust control technique considering the Kharitonov's theorem that ensures the minimization of the total deviation from the desired performance in a closed-loop system, specified by a family of characteristic polynomials. The purpose of the proposed controller is to tightly regulate the dc bus voltage, ensuring MG stability due to the effects of power variation on CPLs. The simulation and experimental tests are performed by using a MATLAB/Simulink simulator and a developed prototype of the DC MG system, respectively, to ratify the robustness and effectiveness of the proposed method of robust controller design.

INDEX TERMS Constant power load (CPL), Chebyshev theorem, DC microgrid (MG), Kharitonov stability theorem, microgrid stability, robust control design.

NOMENCLATURE

$G(s, p)$	Uncertain plant of order n
$P(s, p)$	Uncertain characteristic polynomial
$C(s, x)$	Controller of order r
p	Vector of real parameters that represent the plant
X	Vector of real parameters representing the controller
p^o	The nominal value of plant parameters
$d(s)$	Closed-loop characteristic polynomial
$d_i(x, p)$	closed-loop performance vector
Δ_d	Desired dynamic of closed-loop system
ϕ_i	Parameters of the closed-loop desired polynomial
Φ	Pesired performance region
x_c	Chebyshev Center
B	largest ball of radius R
R	Maximum radius of the largest ball B
A	Parameters Matrix of the plant
$B(\phi)$	Vector that contains ϕ and plant parameters
$B(\phi^+)$	Upper limit of ϕ
$B(\phi^-)$	Lower limit of ϕ
A_i	Matrix A of order i
$\|a_i\|_2$	The euclidian norm of coefficients of A_i
A'_{upper}	Upper limit of A'
A'_{lower}	Lower limit of A'
φ	Parameters of $d_i(x, p)$

φ^o	Nominal values of the parameters of φ
Δ	Uncertainty box region
P_{cl}	closed-loop interval polynomial
$f(.)$	Arbitrary linear function in (.)

I. INTRODUCTION

Nowadays the integration of renewable energy sources, such as solar and wind energy, into the current AC power grid have become a big concern for the research community around the world due to their spatially distributed and fluctuating nature [1], [2]. In the last years, the penetration of these renewable energy sources into the conventional utility grid system is rising every time because of increasing load demand, crisis of conventional energy and the environmental issues [3]–[5].

Microgrids (MGs) have been identified an efficient and attractive option of modern electrical systems to integrate various renewable energy sources [2], [6], where power electronic converters are the main power processing units for interfacing these sources, which facilitates connection to the conventional power system [4]. In contrast with AC MG, the DC MG has many advantages such as robustness, higher efficiency, simple control, an absence of reactive power and harmonics, and natural interface for renewable source [7], [8], which makes DC distribution an option to build more efficient systems [9]. In addition, DC MGs have other advantages over conventional AC systems, such as better current capability of DC power lines, better short circuit protection, and transformer-less conversion of voltage levels [1]. Moreover, MG can disconnect from the main distribution grid, operating as ''islanded mode'' for some cases, such as fault in the main distribution grid, blackout, and continue to supply a portion of their local loads [3].

DC MG usually consists of multiple converters in parallel, cascading, stacking, load splitting, and source splitting configurations in order to achieve proper system operation [4], [10]. Such systems are known as multiconverter power electronic systems or distributed power systems (DPS) [4]. Cascaded power electronic converters are a common feature of almost every converter dominated power system ensuring the desired point-of-load regulation. However, when a power electronic converter tightly regulates its output, it behaves as a Constant Power Load (CPL) if their control performance and bandwidth are sufficiently high to make the consumed power independent to the bus voltage variations [11], [12]. CPL introduces a destabilizing effect in the system, which may cause significant oscillations in the DC bus voltage leading to instability or voltage collapse [3], [11], [13], [14].

The main concern is to ensure DC bus voltage stability, therefore, several methods have been proposed to cope the destabilizing effect of CPL in a DC MG. From the literature, methods to overcome the CPL negative incremental impedance instability problem are categorized into two main categories: hardware modification methods (passive methods) and control techniques (active methods). Using passive approach researchers add a physical element (resistor or mostly capacitor) to the load side converter

to overcome the negative incremental impedance problem [10], [13]. An passive damping method based on the insertion of a transistor as an ac resistor to compensate for the negative incremental impedance of the CPL is successfully employed in [15]. An LC filter and a CPL is used in [16] to stabilize the system without requiring the modification of the source or the load control. The problem with passive techniques is their effect on systems size, weight, cost and efficiency. Other methods are active techniques, which can be applied on the load side and on the generation side. A finite control set model predictive control (FCS-MPC) is reported in [17] as an active damping method realized by introducing a stabilization term in the cost function of the FCS-MPC algorithm that is used for regulation of the point-of-load (POL) converter. Feedback linearization, which aims to cancel the nonlinearity introduced by CPL [18], is reported [19]. Sliding-mode control (SMC) is a large-signal time-domain analytical technique for controlling the dynamic behavior of switching systems that has been applied in the power electronics field in the last years [18], [20]. The model predictive controller (MPC) has been introduced by researchers as a solution to mitigate the instability caused by CPL. MPC controls the variation of the DC bus voltage and modifies of the load impedance which is seen at the point of common coupling [17], [21]. The work developed in [22] reported the application of adaptive back-stepping to deal with the voltage stability of the DC microgrid. In [23], a novel adaptive controller is proposed to mitigate the destructive effect of time-varying uncertain CPLs. The fuzzy model-based controller design procedure for TS fuzzy model is as simple as linear one; meanwhile, the performance of the fuzzy model-based controllers is significantly better. Therefore, numerous fuzzy control methods have been investigated in the literature [24]–[26]. To improve the stability scenario of DC MG system, Kalman filtration method has been introduced by researchers [22], [27], [28]. Robust control techniques has been considered for the elementary power electronics switching converters with a CPL to cope with the mentioned CPL instability [11], [26], [29]. All these statements are well discussed in the literature. However, there are other problems apart from the CPL that are usually not taken into account in the controller design, e.g., uncertainties present in the system parameters, uncertainties associated with renewable power sources, which may lead to performance degradation [30].

To the best of the authors' knowledge, it seems that most papers published so far focus on mitigating the destabilizing effect of CPL without considering the uncertainties present in the system parameters.

Therefore, studies reporting robust parametric methodologies to mitigate oscillations effects caused by CPL in a DC microgrid are still scarce in literature. Although, in [11] an interval robust controller based on Robust Parametric Control (RPC) theory is proposed, aiming to minimize oscillations effects caused by a CPL in a DC Multi-Converter Buck-Buck System. Moreover, in literature can be found control strategies applied to DC power converters that deal with parametric

uncertainties, in [31] a novel multivariable robust parametric technique was used for minimizing coupling effect in single inductor multiple output DC-DC converter operating in continuous conduction mode.

Furthermore, in [32] and [33], the use of RPC techniques is proposed to stabilize oscillations at the output of a buck converter caused by parametric uncertainties. Recently, the study developed in [34] addressed an outstanding contribution for the current state-of-the-art on the study of parametric uncertainties in DC-DC converters, its approach is focused only on a posterior analysis of system stability. However, the important subject of robust controller synthesis has been not addressed. In contrast, the problem of robust controller synthesis is addressed in [11], solving the Linear Matrix Inequality (LMI) optimization problem by using Linear Programming (LP) and Kharitonov's Theorem. Therefore, the RPC method justifiably takes into account all possible uncertainties in the system. However, the application of the RPC method to power electronic systems with CPL and parametric uncertainties is not widely discussed in the literature.

In this context, this paper proposes a novel robust controller based on convex optimization combining the LP approach [35] with Chebyshev Theorem [36], to solve the LMI optimization problem adjusting the parameters of an interval robust controller, in order to mitigate destabilizing effect of CPL in a DC microgrid, ensuring robust performance and stability, and providing a better control performance. The proposed controller is applied to DC power buck converter, which regulates the DC bus voltage, aiming to suppress oscillations effects caused by a CPL power variation. The main paper contributions are briefly summarized as follows:

1) The proposed novel methodology of controller design, based on convex optimization using the Chebyshev Theorem, provides a practical robust controller design algorithm with sufficient level of the detail in order to be easily implemented, aiming to minimize the oscillation effect which occurs in DC microgrid caused by CPL power variation.

2) By using the proposed novel methodology, structured uncertainties of the type hyperbox, considering interval parametric type, are taking into account from the outset in the controller design process, incorporating available information about components (resistors, inductors, capacitors, and CPL power variation) tolerances defined by designer.

3) The proposed method for controller design ensures the performance of controller and MG stability when the DC microgrid is submitted a parametric variation caused by CPL power variation.

The remainder of this paper is organized as follows. Section II presents the studied DC microgrid with its instability problem. Section III presents a brief review about parametric robust control background. Section IV proposes a mathematical model for the DC microgrid system. Section V presents the proposed design methodologies for interval

robust controller. Section VI describes the experiments to be performed in this paper. Section VII presents an assessment of the simulation results and experimental data. Finally, Section VIII presents the main conclusions.

II. STUDIED DC MICROGRID AND PROBLEM FORMULATION

Fig. 1 shows the considered DC MG used in this paper to illustrate the proposed method. The buck converter controls the DC voltage level on the DC bus maintaining the stability of the DC microgrid.
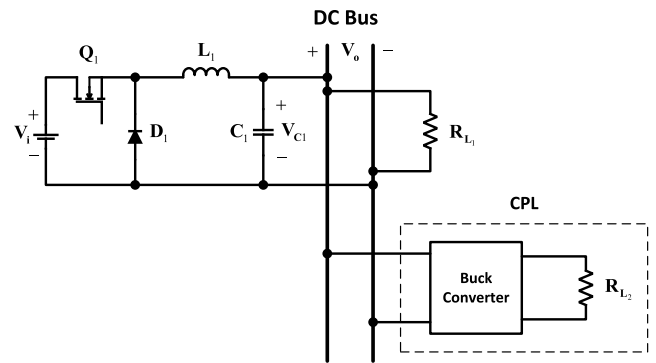

FIGURE 1. The structure of the DC microgrid developed.

DC-DC converters can be used to achieve different DC voltage levels suitable for a range of loads such as electronic devices, lighting, adjustable speed drive applications that require DC voltage, and resistive loads, hence it is more efficient to connect that loads in a DC distribution system [3], [29]. However, a tightly-regulated power electronic converter behaves as a CPL [11], [29].

A CPL behaves as a negative incremental resistance, which tends to destabilize its feeder system. The V-I characteristics of a typical CPL is shown in Fig. 2.

A simple example of CPL in a DC system is tightly-regulated DC-DC converter with resistive load (cf. Fig. 2).

In order to maintain a constant power level, in a DC-DC converter when it acts as a CPL, input current increases when
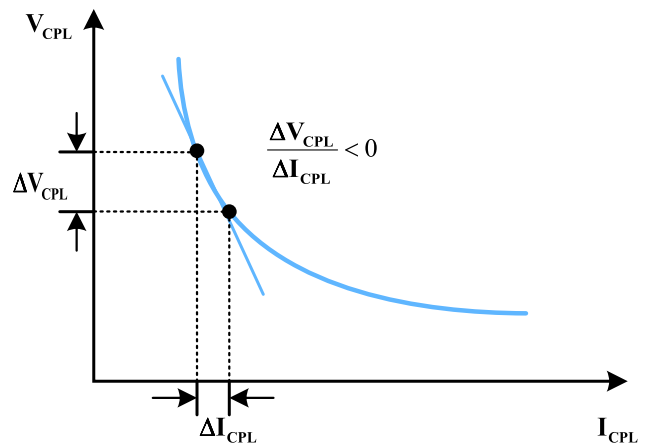

FIGURE 2. V-I characteristics of a typical CPL.

input voltage decreases, and vice versa, thus, the product of the input current and input voltage of the load converter, (i.e., $P_{CPL} = I_{CPL}V_{CPL}$) is a constant [11], [13].

The instantaneous value of the load impedance is positive (i.e., $V_{CPL}/I_{CPL} > 0$). However, the incremental impedance is always negative (i.e., $\Delta V_{CPL}/\Delta I_{CPL} < 0$) due to the appearance of any disturbance, thus its operating point will change and never settling back to its original value again. This negative incremental impedance has a negative impact on the power quality and stability of the DC MG.

The system is analyzed by a phase-plane analysis, solving (plotting) the system differential equations giving an insight about how the system dynamics evolve with time [11], [13].

The phase-portrait of feeder system, which is shown in Fig. 3), is simulated with the following parameters: $V_i = 15\ V$, $L_1 = 2mH$, $C_1 = 2000\ mF$, $P_o = 10\ W$, and $d_1 = 0.744$.

The phase-portrait (Fig. 3(a)) shows the state plane divided into two regions with distinct characteristics [11], [13]:
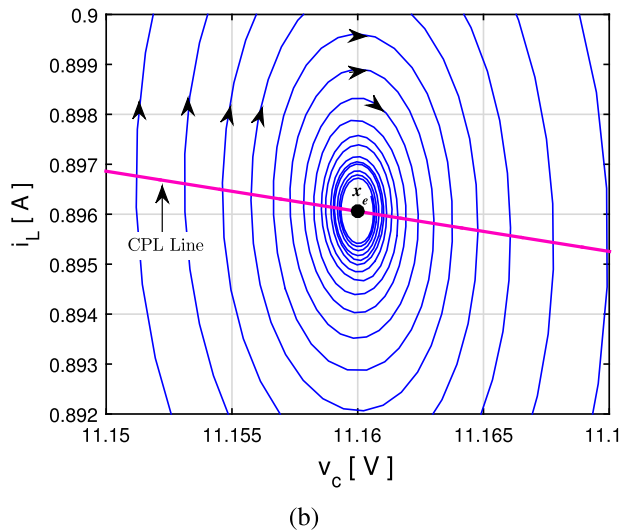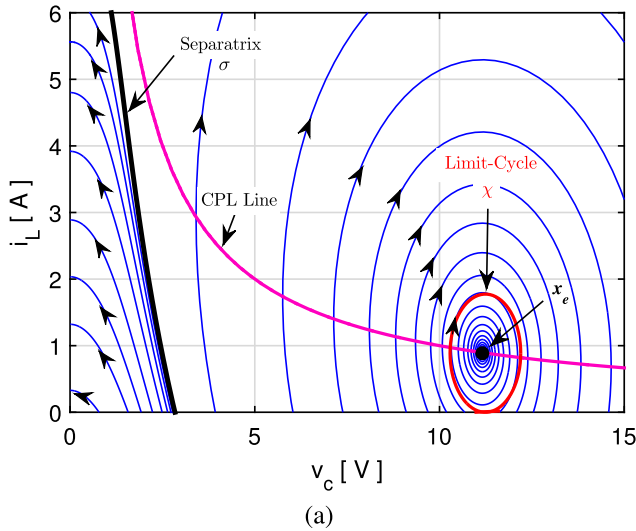

(a)

(b)

FIGURE 3. Phase-portrait obtained by simulating. (a) Phase-portrait of source converter loaded with a CPL. (b) Zoomed area near the operating condition.

one to the left of a separatrix σ, in which the DC bus voltage V_o collapses being an unstable region, and the other to the right of σ, in which V_o presents significant and undesirable oscillations because of the existence of a limit-cycle χ [11], [13].

These oscillations are caused by energy imbalances, which occur during the transient period when LC input filter and output powers are not equal as it occurs in steady state. Therefore, without resistive components in the system, which can dissipate the energy imbalance, this energy will resonate among the energy storage elements in the system. This oscillatory behavior is also observed when attempting regulation if the controller is not adequately designed [11].

III. ROBUST PARAMETRIC CONTROL BACKGROUND
Mathematical models naturally present errors that are neglected, depending on the type of study. An important consideration in model-based control systems is to keep the system stable, subject to parametric variations. However, in the classic controller design, models that ignore uncertainties are used, [11], [29]–[33]. In this way, it is common to use a nominal transfer function for the controller design. Although the controller is developed based on a nominal transfer function, the real system must be stable for all kind of transfer functions that represent the whole set of uncertainties, however, when the system is subjected to different uncertainties, the controller designed deteriorates the system performance. Thereby, uncertainty of a system can be classified as unstructured (non-parametric uncertainty) and structured (parametric uncertainty), [29], [30], [36].

A. ROBUST STABILITY
A system with interval parametric uncertainties is generally described by uncertain polynomials $B(s, q)$ and $A(s, q)$, restricted within pre-specified closed real intervals, as shown in (1), [29], [30].

$$G(s, q) = \frac{B(s, q)}{A(s, q)} = \frac{\sum_{i=0}^{m} \left[b_i^-, b_i^+\right] s^i}{\sum_{i=0}^{n} \left[a_i^-, a_i^+\right] s^i} \quad (1)$$

Many robust stability tests under parametric uncertainty are based on analysis of uncertain characteristic polynomial assumed as an interval polynomial family, [29], [30], such as

$$P(s, p) = \sum_{i=0}^{n} \left[p_i^-, p_i^+\right] s^i \quad (2)$$

Polynomial $P(s, p)$ is stable if and only if all its roots are contained on the Semi-Plan Left (SPL) of the complex plane [37]. Then, $P(s, p)$ is robustly stable if and only if all its polynomials are stable for a set of operating point different from the nominal operating point within its minimum and maximum limits [37]. However, it is not necessary to check stability of an infinite number of polynomials to ensure the robust stability. Robust stability can be checked through the

analysis of four polynomials within $P(s, p)$; these polynomials can be found by Kharitonov theorem [30], [37], [38].

B. ROBUST CONTROLLER DESIGN BY INTERVAL POLE-PLACEMENT

To design the controller, a region of uncertainty is previously defined, considering that the uncertainty is contained in the parameter variation of the plant-model. The controller is designed according to Keel and Bhattacharyya [39], associated with a linear goal programming formulation, which will lead to a set of linear inequality constraints.

Consider $G(s, p)$ a uncertain plant of order n and $C(s, x)$ the controller of order r, defined in (3) and (4) respectively.

$$G(s, p) = \frac{n(s)}{d(s)} = \frac{b_1 s^{n-1} + \cdots + b_{n-1}s + b_n}{s^n + a_1 s^{n-1} + \cdots + a_{n-1}s + a_n} \quad (3)$$

$$C(s, x) = \frac{n_c(s)}{d_c(s)} = \frac{x_0 s^r + x_1 s^{r-1} + \cdots + x_{r-1}s + x_r}{s^r + y_1 s^{r-1} + \cdots + y_{r-1}s + y_r} \quad (4)$$

Let p be the vector of parameters that represent the plant and x the vector of real parameters representing the controller defined in (5) and (6) respectively. In addition, p^o represents the nominal value of plant parameters defined in a hyperbox region of uncertainties.

$$p := [\, b_1 \; b_2 \; \cdots \; b_{n-1} \; b_n \; a_1 \; a_2 \; \cdots \; a_{n-1} \; a_n \,] \quad (5)$$

$$X := [\, x_0 \; x_1 \; \cdots \; x_{r-1} \; x_r \; y_1 \; y_2 \; \cdots \; y_{r-1} \; y_r \,] \quad (6)$$

According to [39], the solution of the Diophantine equation (7) summarizes the classical pole-placement problem, follow as:

$$d(s) = d(s)d_c(s) + n(s)n_c(s) \quad (7)$$

where, $d(s)$ is the closed-loop characteristic polynomial. Therefore, the parameters of the closed-loop characteristic polynomial are represented as follows:

$$d_i = d_i(x, p) \quad (8)$$

Assuming that the desired dynamic of closed-loop system is represented by

$$\Delta_d(s) = s^i + \phi_1 s^{i-1} + \cdots + \phi_{i-1}s + \phi_i \quad (9)$$

where, ϕ_i represent the parameters of the closed-loop desired polynomial.

In order to tune the controller, the closed-loop parameters obtained are compared with the parameters of the closed-loop desired polynomial, which represent the desired dynamics of the system follows as

$$d_i(x, p^o) = \phi_i, \quad i = 1, 2, \ldots, l \quad (10)$$

This problem can be written in its matrix representation, presenting the following relationship, (11), as shown at the bottom of this page.

When the system is subject to parametric uncertainties, the controller performance may deteriorate. Therefore, the controller must guarantee robust performance within an acceptable region of closed-loop parameters variation, so that the closed-loop poles are located in a certain region. Thereby, a desired region is defined as follows:

$$\Phi := \left\{ \phi_i^- \leq \phi_i \leq \phi_i^+ \right\} \quad (12)$$

Therefore, according to [37], replacing the parameters of (12) in (10), it is possible to formulate a linear inequalities set, which restricted the controller and desired polynomial coefficients in the predefined intervals, as shown in (13). Thus, the closed-loop system has its poles within the roots space of interval-desired polynomial, ensuring the robust stability [11], [39].

$$\phi_i^- \leq d_i(x, p) \leq \phi_i^+, \quad \forall i = 1, 2, \ldots, l \quad (13)$$

The robust design problem is summarized in the choice of X (if possible) to satisfy the set of inequality (13) for all $p \in P$. The solution of this problem can be idealized, as a solution to a linear programming problem, therefore different techniques can be used to solve it. However, its standard solution is sometimes efficient and fast, so that this problem can be rewritten as a problem of local minimization, subject to restrictions.

Linear Programming Based on Chebyshev Theorem: The Chebyshev Theorem demonstrates that it is possible to find the largest ball B of center x_c and maximum radius R, whose

$$
\underbrace{\begin{bmatrix}
[b_1] & 0 & \cdots & 0 & 0 & | & 1 & 0 & \cdots & 0 & 0 \\
[b_2] & [b_1] & \ddots & \vdots & 0 & | & [a_1] & 1 & \ddots & \vdots & 0 \\
\vdots & [b_2] & \ddots & 0 & \vdots & | & \vdots & [a_1] & \ddots & 0 & \vdots \\
[b_{m-1}] & \vdots & \ddots & [b_1] & 0 & | & [a_{n-1}] & \vdots & \ddots & 1 & 0 \\
[b_m] & [b_{m-1}] & \ddots & [b_2] & [b_1] & | & [a_n] & [a_{n-1}] & \ddots & [a_1] & 1 \\
0 & [b_m] & \ddots & \vdots & [b_2] & | & 0 & [a_n] & \ddots & \vdots & [a_1] \\
\vdots & 0 & \ddots & [b_{m-1}] & \vdots & | & \vdots & 0 & \ddots & [a_{n-1}] & \vdots \\
0 & \vdots & \ddots & [b_m] & [b_{m-1}] & | & 0 & \vdots & \ddots & [a_n] & [a_{n-1}] \\
0 & 0 & \cdots & 0 & [b_m] & | & 0 & 0 & \cdots & 0 & [a_n]
\end{bmatrix}}_{A}
\underbrace{\begin{bmatrix}
x_0 \\ x_1 \\ \vdots \\ x_{r-1} \\ x_r \\ - \\ y_0 \\ y_1 \\ \vdots \\ y_{r-1} \\ y_r
\end{bmatrix}}_{X}
=
\underbrace{\begin{bmatrix}
[\phi_1] - [a_1] \\ [\phi_2] - [a_2] \\ \vdots \\ [\phi_n] - [a_n] \\ [\phi_{n+1}] \\ \vdots \\ [\phi_m]
\end{bmatrix}}_{B}
\quad (11)
$$

norm is Euclidean, which is contained in the polytope P, described by the set of linear inequalities constraints. The ball center x_c is called Chebyshev Center, as shown in Fig. 4 [36].
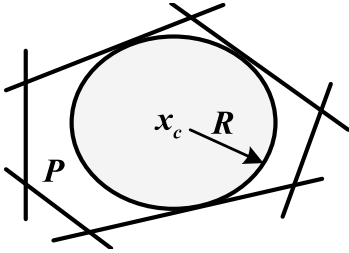

FIGURE 4. Largest ball B inscribed in P.

When the set P is convex, the computing of x_c becomes a convex optimization problem. More specifically, suppose $P \subseteq R^n$ is defined by a set of convex inequalities, i.e., $P = \{a_i x \leq b_i, \ i = 1, \ldots, m\}$. If $R \geq 0$, it can be found x_c by solving the Linear Programming according to the following relations:

$$X' = \arg\left(\min f(X')\right)$$

$$s.t. \begin{bmatrix} A'_{upper} \\ -A'_{lower} \end{bmatrix} X' \leq \begin{bmatrix} B(\phi^+) \\ -B(\phi^-) \\ 0 \end{bmatrix} \quad (14)$$

where,

$$X' = \begin{bmatrix} X \\ R \end{bmatrix}, A' = \begin{bmatrix} A_i & \|a_i\|_2 \\ -A_i & \|a_i\|_2 \\ 0_{1 \times i} & -1 \end{bmatrix} \quad (15)$$

where, $\|a_i\|_2$ is the euclidian norm of coefficients of A_i, A'_{upper} and A'_{lower} represent the lower and upper limit of A', respectively; the cost function is defined as the sum of controller gains within the radio R and the parameter vector X contains the controller gains and the radio of Chebyshev sphere.

IV. MATHEMATICAL MODEL OF THE STUDIED DC MICROGRID

In order to represent the dynamical behavior of the DC MG, a small signal approximation model is employed as an effective mathematical model. Fig. 5 represents the DC MG system with two decoupled outputs, V_{C_1} (DC Bus voltage) and V_{C_2} (CPL output), and a topology employed to control the system. The main characteristic of this MG is that it has a feeder system that regulates the DC bus and feeding a resistive load and a CPL, respectively. Each converter (see Fig 5) can be considered an independent subsystem; therefore, the dynamics of the system can be simplified to the analysis of two independent converters. The dynamic behavior of buck converter, in Continuous Conduction Mode (CCM), can be found in the literature [11], [32].

The equations described in (16) involving the state variables of buck converters are written based on the analysis of their respective equivalent circuits. Fig. 5 shows the DC MG with two outputs V_{C1} and V_{C2}, such that $V_{C_2} < V_{C_1}$, regulated through the duty cycles d_1 and d_2, respectively. The duty cycle of switching Q_1 regulates the DC bus voltage (V_{C1}), and the duty cycle of switch Q_2 regulates the output power of CPL, i.e., $V_{C2}{}^2/R_{L2}$.

Thereby, the outputs of the systems are described in (17).

$$\begin{cases} L_1 \dfrac{di_{L_1}}{dt} = d_1 V_i - V_{C_1} - r_{L_1} i_{L_1} \\ C_1 \dfrac{dV_{C_1}}{dt} = i_{L_1} - \dfrac{V_{C_1}}{R_{L_1}} \\ L_2 \dfrac{di_{L_2}}{dt} = d_2 V_{C_1} - V_{C_2} - r_{L_2} i_{L_2} \\ C_2 \dfrac{dV_{C_2}}{dt} = i_{L_2} - \dfrac{V_{C_2}}{R_{L_2}} \end{cases} \quad (16)$$

$$y_1 = \begin{bmatrix} 0 & V_{C_1} \end{bmatrix}$$
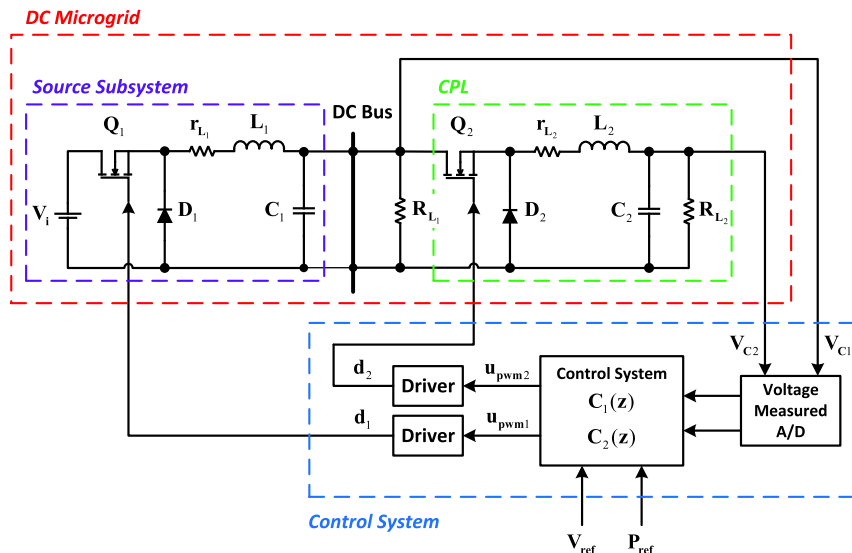$$y_2 = \begin{bmatrix} 0 & P_{CPL} \end{bmatrix} \quad (17)$$

FIGURE 5. Simplified diagram of the DC Microgrid system developed.

Assuming that the electronic switches and diodes are ideal, the linearized model that describes the dynamic steady state behavior of the converter is represented as follows:

$$\frac{V_{C_1}(s)}{V_i(s)} = \frac{\frac{d_1^o}{L_1 C_1}}{s^2 + \left(\frac{1}{R_{L_1} C_1} + \frac{r_{L_1}}{L_1}\right) s + \left(\frac{1}{L_1 C_1} + \frac{r_{L_1}}{R_{L_1} L_1 C_1}\right)} \quad (18)$$

$$\frac{V_{C_2}(s)}{V_{C_1}(s)} = \frac{2\left(\frac{d_2^o}{L_1 C_1}\right)\left(\sqrt{\frac{P_{CPL}}{R_{L_2}}}\right)}{s^2 + \left(\frac{1}{R_{L_2} C_2} + \frac{r_{L_2}}{L_2}\right) s + \left(\frac{1}{L_2 C_2} + \frac{r_{L_2}}{R_{L_2} L_2 C_2}\right)} \quad (19)$$

where, d_1^o and d_2^o are operational point for duty cycle of output 1 and 2, respectively. P_{CPL} is the operating power of CPL.

The nominal values of the parameters, operational point and the meaning of each symbol in (18) and (19) are presented in Table 1.

TABLE 1. Values for the physical parameters of the DC Microgrid develop test system.

Par.	Unit	Var (%)	Nom. Val.	Description
V_i	V	15	15.0	Source input voltage
R_{L_1}	Ω	50	4.0	Loading at output 1
R_{L_2}	Ω	–	4.0	Loading at output 2
C_1	μF	10	2000	Capacitor at output 1
C_2	μF	–	2200	Capacitor at output 2
L_1	μH	10	2.0	Inductor at source subsystem
L_2	μH	–	2.0	Inductor at CPL
r_{L_1}	Ω	15	0.05	Internal resistance of L_1
r_{L_2}	Ω	–	0.05	Internal resistance of L_2
d_1^o	%	–	74.4	Operating duty cycle of output 1
d_2^o	%	–	63.2	Operating duty cycle of output 2
$V_{C_1}^o$	V	–	8.0	Output voltage of source subsystem
P_{CPL}	p.u.	–	0.3	Output power of CPL
f_{sw1}	kHz	–	1.0	Switching frequency of duty cycle d_1
f_{sw2}	kHz	–	5.0	Switching frequency of duty cycle d_2
P_{max}	W	–	20.0	Maximum power at CPL
f_s	kHz	–	1.0	Sampling frequency

V. ROBUST CONTROLLER DESIGN METHODOLOGIES

This section presents the methodologies for designing a fixed order robust controller considering an uncertain family of plants. Such methodologies identify controllers that provide robust stability and performance for a specific and predetermined hyperbox region. This study only considers uncertainties in the parameters in the source subsystem (see Table 1) because oscillations, caused by a CPL, occur in the LC filter of the converter. Therefore, only output 1 will be regulated by a robust controller. A classic controller, based on Classical Pole-Placement (CPP), will regulate output 2 in order to emulate a CPL with a DC-DC buck converter. The robust controller is designed according to presented by [37] and [36]. In this paper, these methodologies will be called ''Control based on Kharitonov's Rectangle (CKR)'' and ''Control based on Chebyshev's Sphere (CCS)''. The proposed controller must ensure robust stability and performance for the entire region of parametric variation.

Fig. 6 illustrates a simplified flowchart of the methodology for designing the robust controller based on interval pole-placement. The process starts in step 1, by defining the nominal plant (18) with its operating conditions; in step 2, the box region of uncertainties is built based on a previously specified uncertainty range delimited by the designer. Since box region of uncertainties influences on the delimitation of the convex region where the control gains will be determined, the correct selection of this box region is an important point to consider in order to have success on the proposed methodology. The lower-and upper-bound of each parameter are provided in Table 1. The closed-loop polynomial is obtained (Step 3) by using the controller parameter and the nominal model (18) selected in step 1, then by replacing the nominal and interval values, defined in step 2, the interval closed-loop polynomial is calculated. The controller function depends on the chosen control structure. In this work, a controller with a PID structure is selected. The transfer function is given below.

$$C_{PID}(s) = \frac{u(s)}{e(s)} = \frac{k_d s^2 + k_p s + k_i}{s} \quad (20)$$

For simplification, transfer function, presented in (18), can be represented as follows:

$$G_1(s) = \frac{V_{C1}(s)}{V_i(s)} = \frac{b_0}{s^2 + a_1 s + a_0} \quad (21)$$

Finally, closed-loop interval polynomial is obtained by using the controller (20) and plant (21) parameters.

$$P_{cl}(s) = s^3 + \left[\varphi_2^-, \varphi_2^+\right] s^2 + \left[\varphi_1^-, \varphi_1^+\right] s + \left[\varphi_o^-, \varphi_o^+\right] \quad (22)$$

The nominal parameters of P_{cl} depend on the parameters of source converter (cf. Table 1), resulting in the following nominal parameters:

$$\varphi_0^o = b_0 k_i \quad (23)$$
$$\varphi_1^o = a_0 + b_0 k_p \quad (24)$$
$$\varphi_2^o = a_1 + b_0 k_d \quad (25)$$

The lower- and upper-limits for these parameters must be computed by replacing the nominal and interval values presented in Table 1 through interval analysis for (21). The region defined by the closed-loop interval polynomial (22) must be inside the region determined by the desired performance polynomial (chosen in Step 4). Particularly, it was chosen for a maximum settling time of less than 0.15 sec. and a damping factor greater than 0.9, defining the desired performance region (26). Note that an auxiliary pole must be added that does not affect the desired dynamics of system to satisfy (9).

$$\Phi = s^3 + [\phi_2] s^2 + [\phi_1] s + [\phi_o] \quad (26)$$

The optimization problem is selected in step 5 and in step 6 is solved. In step 6(A), the cost function is defined as the sum of controller gains and the parameter vector X contains the controller gains, according to [35]. In step 6(B), the cost function is defined as the sum of controller gains with the
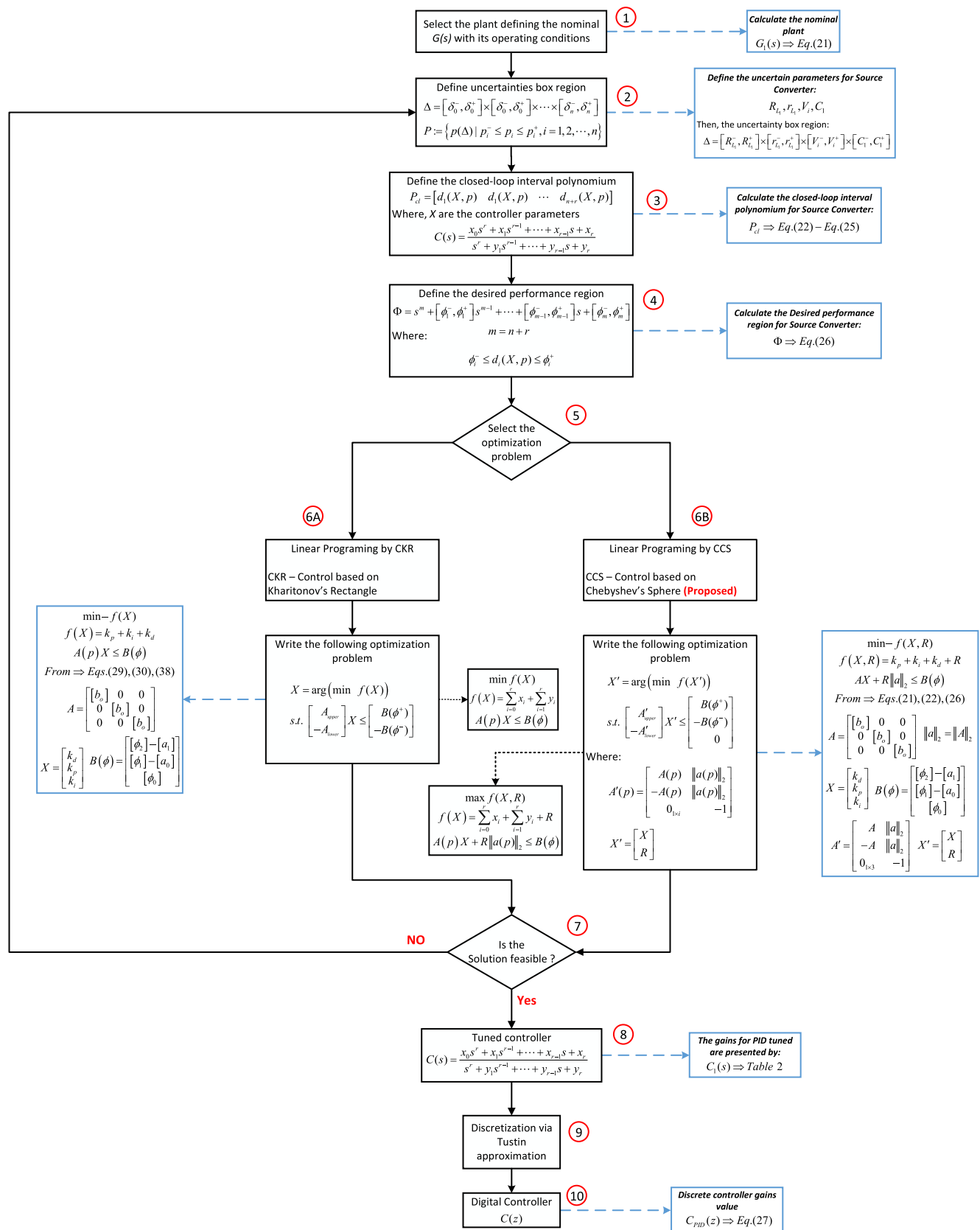
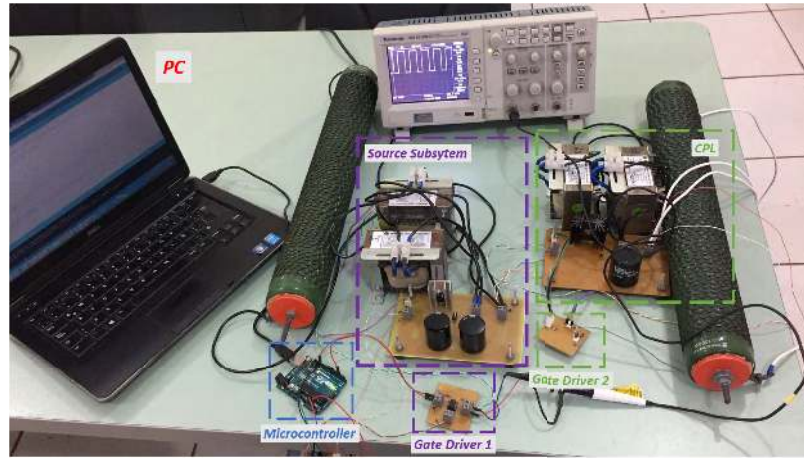**FIGURE 6.** Flowchart of the robust controller design methodologies.

FIGURE 7. The DC Microgrid board developed.

radio R and the parameter vector X contains the controller gains and the radio of Chebyshev sphere.

The feasible solution X^* (obtained in step 6) is verified in step 7 in case of achieving it, advance to step 9, if not, go back to step 2, where you must redefine the system's uncertainties. Then, the feasible solution is used to set the control structure (step 8). In order to obtain the discrete equivalent of the designed controller, the Tustin method [40], [41], was used (Step 9) to perform the discrete approximation, using as a selection criterion of sampling frequency between 2 to 10 times greater than the frequency band of system [40], sampling rate of 1 ms was chosen. Finally, step 10 presents the generic form for obtaining the discrete gains of the digital PID controller. The following equations present discrete PID controller.

$$C_{PID}(z) = \frac{h_0 z^2 + h_1 z + h_2}{z^2 - 1} \qquad (27)$$

VI. DESCRIPTION OF EXPERIMENTS
The Integral Square Error (ISE) is used to assess the performance of the proposed control strategy. In order to design the controllers, the following (nominal) requirements are chosen to regulate the output 1: settling time less or equal than 0.1 sec. and damping factor greater or equal than 0.9. To regulated the output 2 (P_{CPL}), requirements are: settling time less or equal than 0.05 sec. and damping factor greater or equal than 0.9. Note that the dynamics of output 2 is faster than output 1, being this a necessary condition for the power converter acts as a CPL.

The experiments compare the performance of the controllers tuned by CCS, CKR and CPP methodologies using PID control structure.

Table 2 shows each controller gains for the controllers designed to regulated output 1 and 2. Note that only for output 1, robust control methodology is used.

The DC MG system starts with CPL disconnected until source subsystem achieves its steady state (cf. Table 1), then the CPL is connected (t = 0.5 sec) causing a load disturbance

TABLE 2. Values of parameters for the designed controllers.

Controller Gains		CCS Method	CKR Method	CPP Method
$C_1(s)$	k_d	$1.017e^{-5}$	$1.0588e^{-5}$	$1.2024e^{-5}$
	k_p	0.011815	0.010814	−0.009997
	k_i	2.9109	2.6783	2.4169
$C_2(s)$	k_d	−	−	$2.49916e^{-5}$
	k_p	−	−	−0.025413
	k_i	−	−	51.6969

at the DC bus voltage. The brief description of the experiments are presented as follow:

1) Positive variation of CPL power: When the DC MG is operating in its steady state (8V and 0.3 p.u.), the system is subjected to a positive variation of CPL power (t = 1.0 sec.) within an amplitudes range from 0.1 to 0.5 [p.u.].

2) Negative variation of CPL power: The experiment begins in the same way than the experiment described in positive variation test until the DC MG system achieves its steady state (8V and 0.3 [p.u.]). Then, a variation in operating condition at CPL (P_{CPL}) occurs (t = 1 sec.), in order to obtain a considerable negative variation, so the system will operate with the following conditions: $V_{C_1}^o = 8\ V$ and $P_{CPL} = 0.7$ [p.u.]. After that, the system is subjected to a negative variation of CPL power (t = 1.5 sec.) within an amplitude range from 0.1 to 0.5 [p.u.].

3) Positive and negative variation of CPL power: This experiment evaluates the closed-loop performance for positive and negative variation of CPL power. After the multi-converter system reaches its steady state, a positive variation of 0.5 [p.u.] is performed at the operating point of CPL power reference. Then, a negative variation of 0.5 [p.u.] is performed to return to the initial condition.
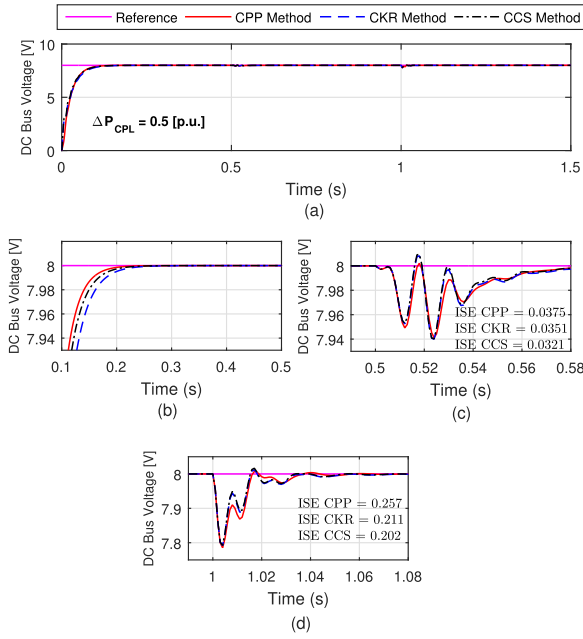
FIGURE 8. Source subsystem performance. (I) Positive variation of CPL power. (II) Negative variation of CPL power.

FIGURE 9. CPL performance. (I) Positive variation of CPL power. (II) Negative variation of CPL power.

These experiments aim to demonstrate that the proposed robust controller is able to compensate oscillations caused by a CPL at DC bus voltage when the system is submitted to positive and negative variations of CPL power operating condition, maintaining the desired performance for the uncertainty region and consequently different operation points.

All the experiments are performed in experimental environment through a DC MG of the prototype developed and

simulation environment using Matlab/Simulink. Fig. 7 shows the system developed for the experimental study.

VII. ASSESSMENT OF RESULTS
A. SIMULATED TESTS
The simulated tests are performed as described in Section VI. Figs. 8 and 9 show the simulated responses performed in the DC MG system, using a PID control
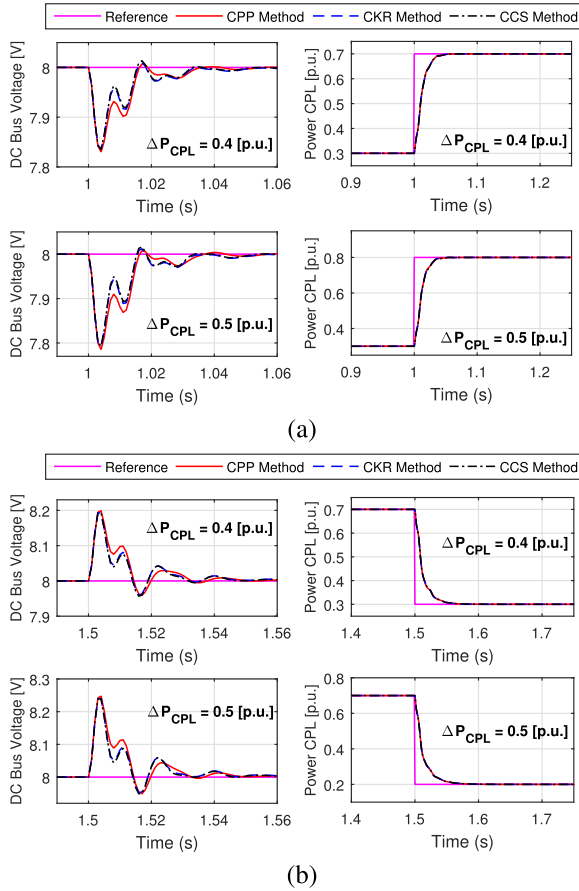
FIGURE 10. Simulated environment of DC microgrid with CPL power variation. (a) Positive variation. (b) Negative variation.

FIGURE 11. The cost function ISE of system outputs when the DC microgrid is subjected to CPL power variations. (a) Positive variation. (b) Negative variation.

FIGURE 12. The control effort of simulated DC microgrid with CPL power variations. (a) Positive variation. (b) Negative variation.

with a positive and negative variation of CPL power, respectively.

The DC MG system starts with CPL disconnected until source subsystem achieves its steady state (see Table 1), then the CPL is connected ($t = 0.5$ *sec.*) causing disturbance at the DC bus voltage. When the DC MG system is operating in its steady state (8V and 0.3 [p.u.]), the system is subjected to a positive variation of CPL power ($t = 1.0$ *sec.*) as shown in Figs. 8(I) and 9(I).

According to Figs. 8(II) and 9(II), the experiment begins in the same way that the experiment described in Fig. 8(I) and 9(I), until the DC MG system achieves its steady state (8V and 0.3 [p.u.]). Then, a variation in operating condition at CPL power (P_{CPL}) occurs at $t = 1$ *sec.*, thus the system will operate with the following conditions: $V_{C_1}^o = 8V$ and $P_{CPL} = 0.7[p.u.]$, after that, the system is subjected to a negative variation of CPL power ($t = 1.5$ *sec.*).

Fig. 10(a) and Fig. 10(b) shows, respectively, the positive and negative variation of CPL power in simulated environment, using a PID control structures.

The simulated results demonstrate that all controllers of source subsystem can compensate oscillations at DC bus voltage caused by CPL power variations. However, the inter-
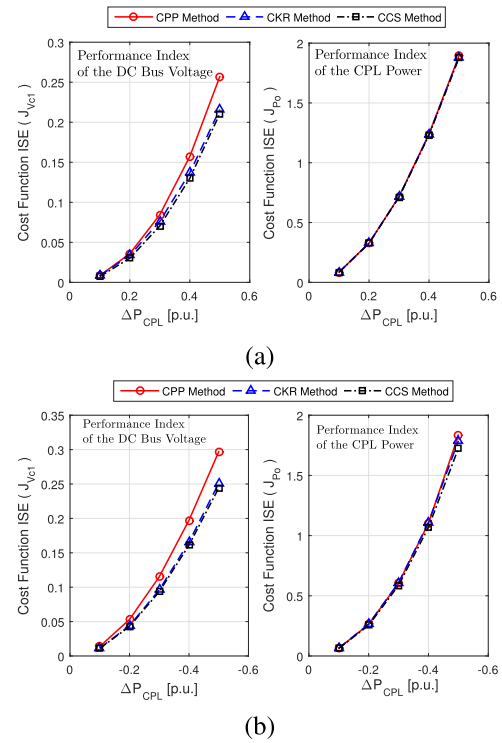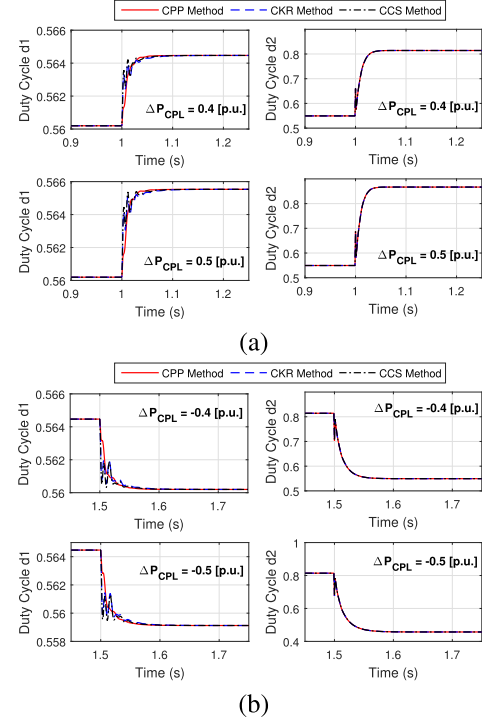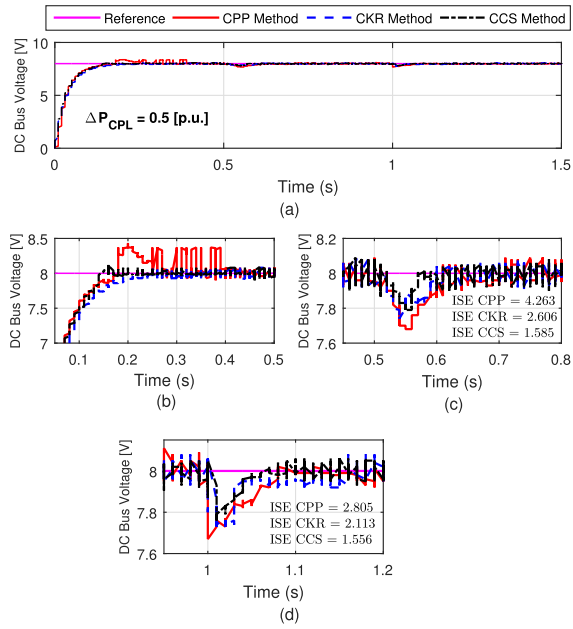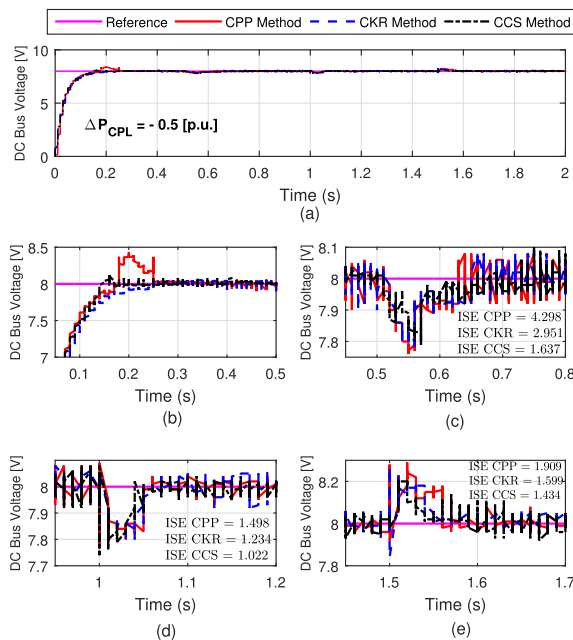
val robust (CCS Method) controller proposed in this paper provides a better performance in comparison with robust controller (CKR Method) and classical controller (CPP Method).
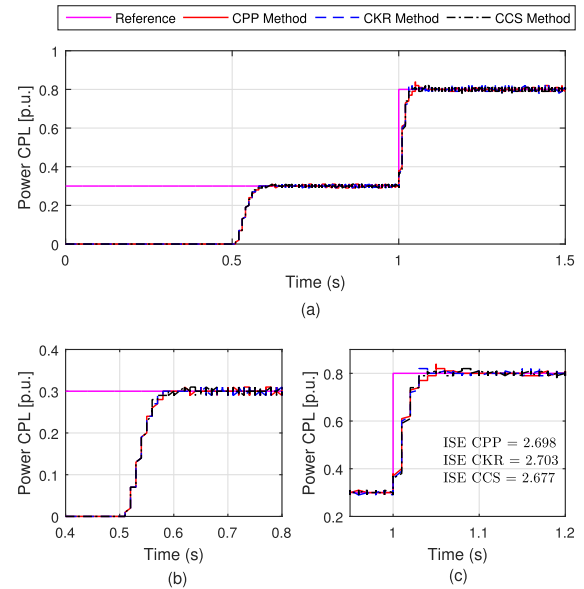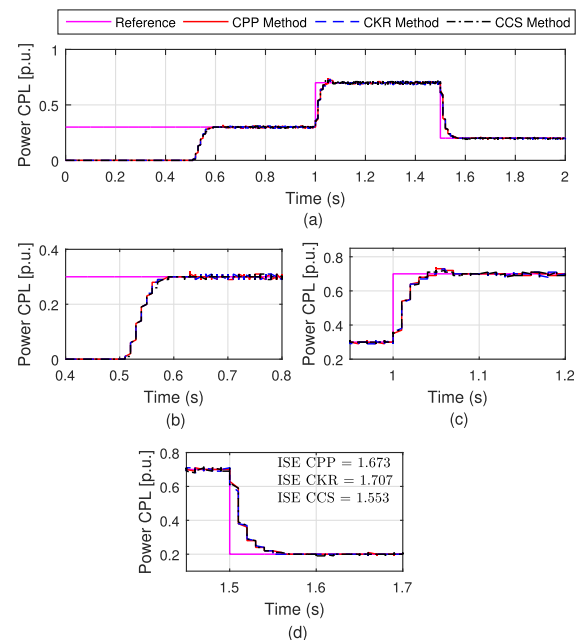
FIGURE 13. Source subsystem performance under CPL power variation. (I) Positive variation. (II) Negative variation.

FIGURE 14. CPL performance. (I) Positive variation of CPL power. (II) Negative variation of CPL power.

Therefore, the impact of CPL power variations is reduced when the CCS method is used, as shown by the ISE performance indices in Figs. 11(a) and 11(b), ratifying the robustness of the proposed methodology. Fig. 12 shows the control effort of controllers of the DC MG system for simulated tests, using a PID control structures. Note that saturation of the control signal does not occur at any time.

B. EXPERIMENTAL TESTS

The experimental tests are performed in the same way as the simulated test. Figs. 13 and 14 show the experimental responses performed in the DC MG system, using PID control with a positive and negative variation of CPL power, respectively.

Fig. 15(a) and Fig. 15(b) shows, respectively, the positive and negative variation of CPL power in experimental environment, using PID control structures.
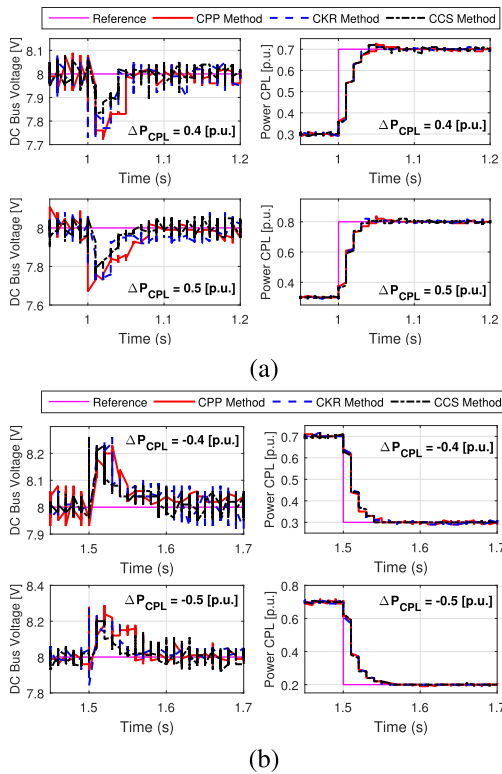
FIGURE 15. Experimental test of DC microgrid under CPL power variation. (a) Positive variation. (b) Negative variation.
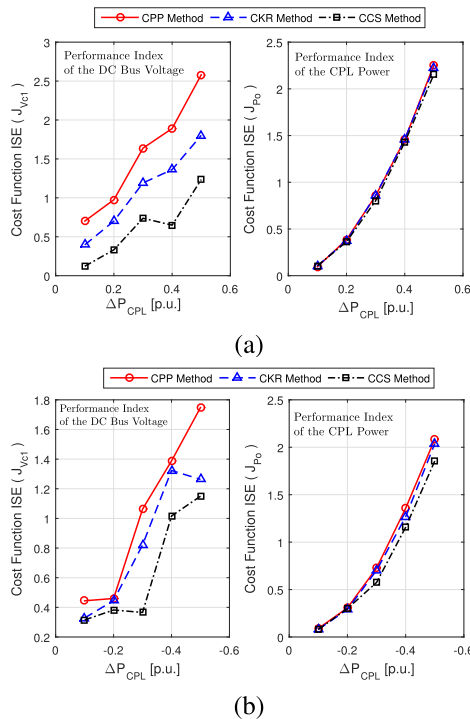

FIGURE 16. The cost function ISE of system outputs when the DC microgrid is subjected to CPL power variations. (a) Positive variation. (b) Negative variation.

The experimental tests show that the robust proposed (CCS) approach outperforms the robust (CKR) approach and
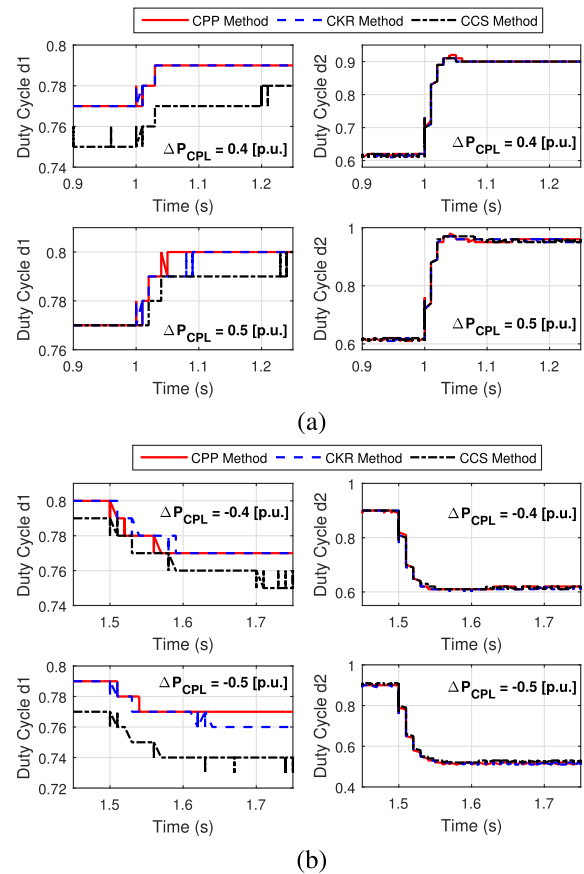

FIGURE 17. The control effort of experimental DC microgrid with CPL power variations. (a) Positive variation. (b) Negative variation.

classical (CPP) approach for several values of CPL power variations (P_{CPL}).

Therefore, the controller proposed provides a better performance with reduced oscillations at DC bus voltage in comparison with the classical controller (CPP) and the classical robust controller (CKR).

Fig. 16 shows the comparison of ISE performance index for the DC MG test system between robust and classical approaches. For most of the operating values of P_{CPL}, the ISE indexes for CPP method show higher values in comparison with CKR and CCS methods.

Although the controller of CPL does not change, different performances can be observed (cf. Fig. 16(b)) due to the oscillation in the DC bus voltage caused by CPL power variations. Thereby, the controller of the voltage regulation stage that better compensates for the oscillations will cause less deterioration in the performance of the power control stage.

The ISE index evaluates the impact of CPL power variations (P_{CPL}) on system performance. Therefore, the robust controller (CCS) shows the best performance for experimental test ratifying the robustness of the proposed approach.

Fig. 17 shows the control effort of controllers of the DC MG system for experimental tests, respectively, using a PID control structures under CPL power variations (P_{CPL}). Note
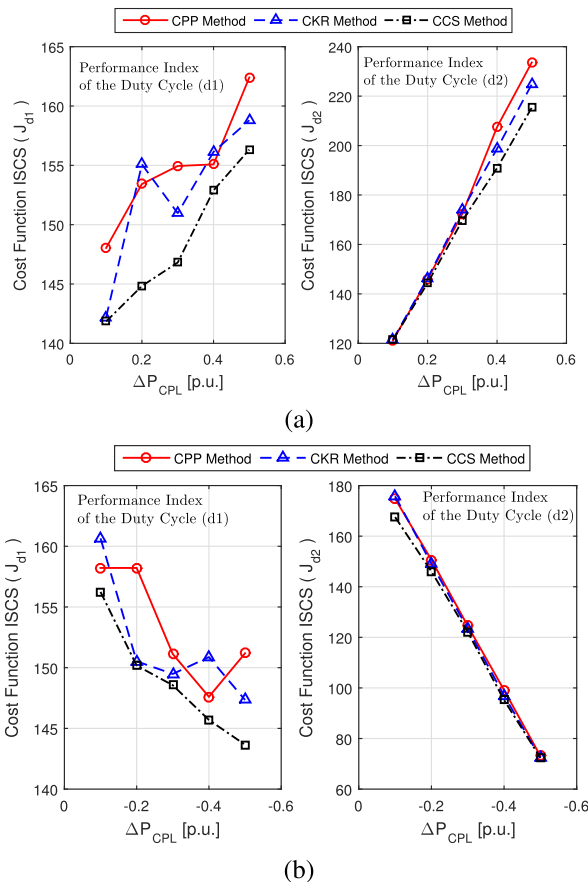
(a)

(b)

FIGURE 18. The integral square of control signal (ISCS) of experimental tests when the DC microgrid is subjected to CPL power variations. (a) Positive variation. (b) Negative variation.

that the saturation of the control signal does not occur at any time.

The Integral Square of Control Signal (ISCS) for experimental tests developed is shown in Fig. 18. Note that the CCS method presents less variations of duty cycle in comparison of others approaches. The DC MG system obtained less degradation in the control system performance when the robust proposed controller regulates the DC bus voltage as shown their ISCS performance indexes in Fig. 18.

Fig 19 shows the experimental evaluation performed in the DC MG system, using a PID control based on CPP approach. Fig 20 shows the experimental evaluation performed in the DC MG system, using a PID control based on CKR approach. Fig 21 shows the experimental evaluation performed in the DC MG system, using a PID control based on CCS approach.

Figs. 19 to 21 show the CPL power variation and the voltage oscillations in the feeder converter by using the classical control methodology and robust control methodologies, respectively. It is worth to note that the CCS approach outperforms the other approach due to the minimum voltage oscillation occurrence, in addition, the oscillation is quickly corrected in comparison with the CPP and CKR approach,
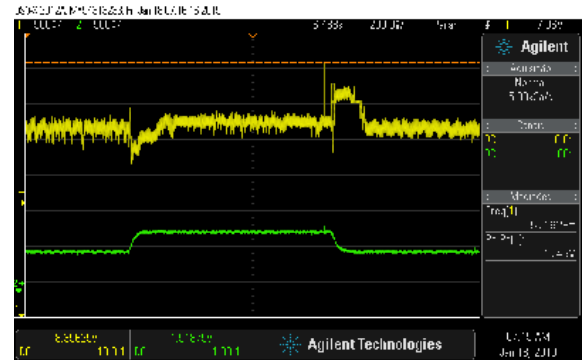

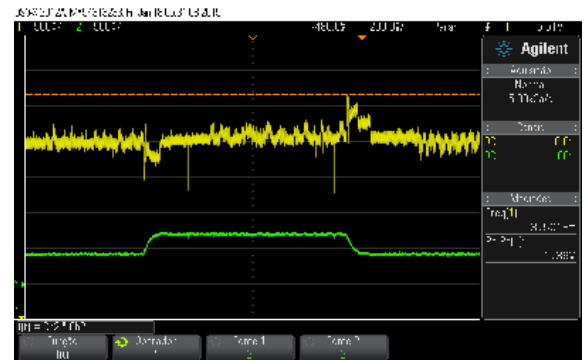**FIGURE 19.** DC MG system performance, using a PID control based on CPP approach.

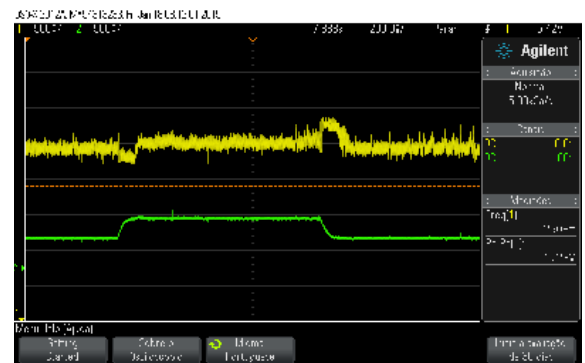**FIGURE 20.** DC MG system performance, using a PID control based on CKR approach.

FIGURE 21. DC MG system performance, using a PID control based on CCS approach.

furthermore the CCS methodology presents the smaller voltage ripple than the CPP and CKR approach.

In order to ratify these results, the integral index of this oscillation for all approaches was calculated, the CKR approach presents 1.24 of the ISE value, the CPP approach presents 1.62 ISE value and the CPP approach presents 2.16 ISE value, therefore, it was ratified that the CCS approach outperforms the others approaches when there is variation of a CPL power in the system.

VIII. CONCLUSION
This paper proposes a novel robust parametric control technique for designing fixed order robust controller, in order to minimize oscillation effects caused by constant power load

in a DC MG system, ensuring robust stability and robust performance for an entire predefined uncertainty region.

The design procedure is based on RPC theory. The proposed technique has been exhaustively evaluated in both computational simulations as well as by means of physical experiments performed in a DC MG board developed, using PID control structures. The proposed robust controller (CCS Method) performance is compared with a robust controller (CKR Method) and a classical controller based on pole-placement (CPP Method).

According to the results obtained via simulation and experimentally, it is concluded that when the DC MG system is subjected to a certain variation of CPL power (P_{CPL}), the CCS method more effectively compensates the oscillations at DC bus voltage (V_{C_1}) improving the performance of the whole system as shown by the performance indicators obtained in this work.

Therefore, the results indicate that the proposed robust controller (CCS Method) is justified and present relevant performance improvements in the DC MG control, offering robust performance and stability.

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