Received 15 October 2020; revised 25 November 2020; accepted 29 November 2020. Date of publication 2 December 2020; date of current version 28 January 2021. The review of this article was arranged by Editor C.-M. Zetterling.

Digital Object Identifier 10.1109/JEDS.2020.3041842

Novel Si/SiC Heterojunction Lateral Double-Diffused Metal Oxide Semiconductor With SIPOS Field Plate by Simulation Study

BAOXING DUAN, SHAOXUAN XUE, XIN HUANG, AND YINTANG YANG (Senior Member, IEEE)

Key Laboratory of the Ministry of Education for Wide Band-Gap Semiconductor Materials and Devices, School of Microelectronics, Xidian University, Xi'an 710071, China

CORRESPONDING AUTHOR: B. DUAN (e-mail: bxduan@163.com)

This work was supported in part by the Science Foundation for Distinguished Young Scholars of Shaanxi Province under Grant 2018JC-017, and in part by 111 under Project B12026.

ABSTRACT A novel Si/SiC heterojunction Lateral Double-diffused Metal Oxide Semiconductor with the Semi-Insulating Polycrystalline Silicon field plate (SIPOS Si/SiC LDMOS) is proposed in this paper for the first time. The innovative terminal technology of Breakdown Point Transfer (BPT) had been applied on Si/SiC MOSFETs. This creative technology improved Breakdown Voltage (BV) of the proposed device, compared with the conventional Si LDMOS (Cov. LDMOS). In order to optimize the trade-off between BV and Specific On-Resistance ($R_{ON,SP}$), the SIPOS field plate is applied on Si/SiC LDMOS for the first time in this paper. At On-State, due to the internal electric field of SIPOS filed plate, the majority carriers accumulation layer is formed on the surface of the drift region for the proposed SIPOS Si/SiC LDMOS, which means $R_{ON,SP}$ will be reduced. Meanwhile, the electric field modulation effect of SIPOS field plate can make the surface electric field distribute evenly, which leads to an increase of BV. In addition, due to the high-thermal conductivity of SiC substrate, the heat-dissipation efficiency of the proposed device is significantly improved. The simulation results show that the BV of SIPOS Si/SiC LDMOS is 428.4V, which increased by 78.4% in comparison with Cov. LDMOS (*BV* of 240.0V) with the same structure parameters. The $R_{ON,SP}$ of SIPOS Si/SiC LDMOS is decreased from 33.2m$\Omega \cdot cm^2$ of Cov. LDMOS to 24.0m$\Omega \cdot cm^2$, decreased by 27.7%. Furthermore, the figure-of-merit (FOM = $BV^2/R_{on,sp}$) of SIPOS Si/SiC LDMOS reaches 7.6MW/cm^2, which means SIPOS Si/SiC LDMOS has enough performance to break the Silicon limit.

INDEX TERMS Si/SiC heterojunction, SIPOS, breakdown point transfer, breakdown voltage, specific on-resistance, figure-of-merit.

I. INTRODUCTION

The contradiction between the low Specific On-Resistance ($R_{ON,SP}$) and high breakdown voltage (*BV*) restricts the development of Power Integrated Circuit. An ideal power device should have the following ideal static and dynamic characteristics: It shall withstand the high voltage in the reverse state with no leakage current. It shall have the large current with no voltage drop in on-state. It shall have a short switching time during switching conversion, which is easy to control and does not use energy. The current research is making the power device close to this ideal direction.

In order to design a Si-based Lateral Double-diffused Metal Oxide Semiconductor (LDMOS) with the high *BV* and low $R_{ON,SP}$, previous researchers proposed the Reduced Surface Electric Field (RESURF) [1]–[2], and other structure and technologies based on the conventional Si LDMOS (Cov. LDMOS) to optimize device performance [3]–[4]. However, due to the restrictions of "Silicon limit" [5]–[6], Si-based devices have reached its performance limitation, so the SiC materials obtain its opportunity. SiC material has the characteristics of the wide bandgap, high-thermal conductivity and critical electric field about 10 times that of the Si material [7]. The superior material properties

of SiC allow it to be widely used in high-voltage and high-temperature applications [8]–[10]. However, SiC-based LDMOS still have many problems to be solved. For example, a high-quality gate oxide is needed by SiC LDMOS, but compared with SiO_2 on Silicon, the oxide layer grown on SiC has a high interfacial-charge density, which will cause the degradation of device performance [11]. According to previous studies, some researchers combined the advantages of Si and SiC materials and proposed a Si/SiC heterojunction device. This heterojunction device has both high quality gate oxide layer and high *BV* [12]. The key to the Si/SiC heterojunction device is the manufacture of Si/SiC wafer with good quality. Currently, Low-Pressure Chemical Vapor Deposition (LPCVD), Molecular Beam Epitaxy (MBE) and wafer bonding processes [13]–[15] have been used to fabricate Si/SiC hybrid substrates. However, experiments have shown that the Si layers grown using LPCVD or MBE are of poor quality due to the stresses generated by the lattice-misfit between Si and SiC [15], [16]. Therefore, in recent years, the Si/SiC substrates are mostly fabricated by wafer bonding process. In 2018, P.M. Gammon et al. proposed a method of producing Si/SiC substrates by wafer bonding silicon-on-insulator (SOI) wafers to 4H-SiC [17]. This method can effectively improve the Si/SiC interface quality problem caused by lattice-misfit.

Therefore, based on those points, a Si/SiC heterojunction LDMOS with the SIPOS field plate (SIPOS Si/SiC LDMOS) is proposed for the first time. This novel device has the following advantages: Firstly, the peak of the electric field is transferred from the surface of drain region to the SiC substrate by the terminal technology of Breakdown Point Transfer (BPT) [18]–[21], which can improve the *BV* compared with Cov. LDMOS. Secondly, at On-State, SIPOS layer, which is deposited on the surface of a thin oxide layer above the drift region, can assist to form a majority carriers accumulation layer on the surface of drift region, and thus form a conductive channel to reduce $R_{ON,SP}$ [22]. Thirdly, the surface electric field of the drift region can be forced to evenly distribute by the electric field modulation effect by SIPOS field plate, so the reverse characteristic of the proposed device is optimized effectively.

II. DEVICE STRUCTURE AND DESCRIPTION

The cross-section of the proposed SIPOS Si/SiC LDMOS is shown in Fig. 1. Different from the conventional Si LDMOS and Si/SiC LDMOS, the novel SIPOS Si/SiC LDMOS, which is based on Si/SiC LDMOS with the deep drain, deposited a SIPOS layer on the thin oxide layer above the drift region and connected with gate and drain electrode. While the BPT technology modulate the vertical and lateral electric field distribution, SIPOS field plate optimizes the $R_{ON,SP}$ of the device as well. Therefore, the performance of the device is improved. Besides, the deep drain region can assist in the vertical depletion, which facilitates the improvement of *BV* as well.

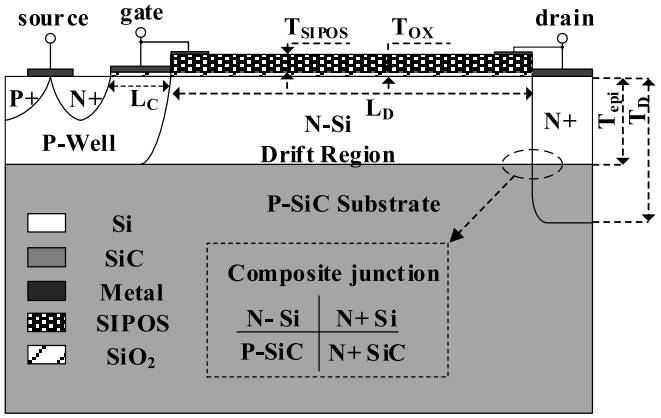

FIGURE 1. Cross-section of SIPOS Si/SiC LDMOS.

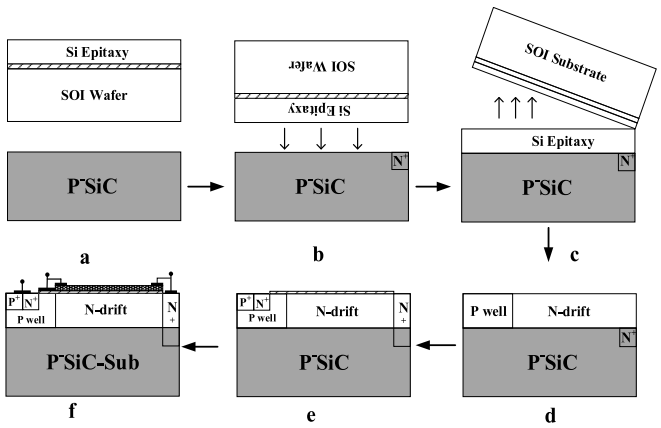

FIGURE 2. Simplified key processes of fabricating SIPOS Si/SiC LDMOS.

The key processes of the proposed device are presented in Fig. 2. The simplified manufacturing processes are as follow: Firstly, use ion implantation to form N^+ region in the SiC substrate. The surface of SiC wafer and SOI wafer are both RCA cleaned. Then, bond the SiC and SOI wafer with the method in [17]. The SOI wafer is thinned by CMP, before a HF solution is used to remove the buried oxide. In order to minimize the defects on the Si surface, the dry-etch to reduce the thickness of Si layer to 3 μm is then performed at the end of wafer bonding, as is shown in Fig. 2(c).

Because the active region is formed in Si layer, the remaining process steps are basically the same as the conventional Si process, which can be summarized as follows: using ion implantation technology to manufacture the N-drift, P-well. Then, the oxide layers are grown on the surface of Si from the edge of source region to the drain. The other part of the drain, source region and P^+ region is formed by using ion implantation technology. Finally, deposit the SIPOS layer on the oxide layer above the drift region by LPCVD technology. In order to obtain the low ohmic contact resistance, source and drain electrode of SIPOS Si/SiC LDMOS is made of Si material. The gate electrode uses the mature silicon power device technology to avoid the defect oxidation gate of SiC material.

TABLE 1. Key parameters in device simulations.

Sym bol	Description	Values	
		SIPOS Si/SiC LDMOS	Cov. LDMOS
N_D	the concentration of N-drift (cm^{-3})	8×10^{15}	1.2×10^{16}
T_D	the depth of drain region(μm)	6	1
N_P	the concentration of P-well (cm^{-3})	4×10^{17}	
T_{OX}	the thickness of oxide under SIPOS FP(μm)	0.09	—
T_{epi}	the thickness of drift region (μm)	3.0	
T_{SIPOS}	the thickness of SIPOS FP(μm)	0.45	—
L_D	the length of drift region (μm)	20	
L_C	the length of channel (μm)	1	

In order to estimate the electric characteristics of the novel SIPOS Si/SiC LDMOS, ISE TCAD is used to simulate and analyze the two-dimensional electric characteristic of the device [23]. The key parameters are listed in Table 1. N_D will be adjusted appropriately with different devices to obtain accurate breakdown voltage. The main physics models are applied by ISE simulation including mobility model, effective intrinsic density model, and recombination model. The mobility model includes *Doping Dependence, HighFieldSat,* and *Enormal(Lombardi)*. The effective intrinsic density model includes *BandGap Narrowing*, and the recombination model includes *SRH* model and *Auger* model. The criterion of breakdown is *BreakCriteria* {*Current (Contact = "drain" Absval =* 1×10^{-7}*)*}. *The parameter is Material = "Silicon Carbide"*.

III. RESULTS AND DISCUSSION

Fig. 3 shows the distribution of equipotential lines when Cov. LDMOS and SIPOS Si/SiC LDMOS are broke down. It can be seen from the figure that, with the assistance of SIPOS layer, the depletion region of the novel device extends deeper in the vertical direction, which indicates that the internal electric field of SIPOS layer can assist in depleting substrate. Meanwhile, the BPT technology is applied to SIPOS Si/SiC LDMOS. It can be seen from Fig. 3 that the highest electric field of SIPOS Si/SiC LDMOS appears in the SiC material (Region B), which implies that the most reverse voltage will be applied on SiC Substrate. By contrast, the highest electric field of Cov LDMOS appears at the Si material (Region A). Due to the high critical breakdown electric field of SiC, this novel device can withstand a higher voltage than that of Cov LDMOS.

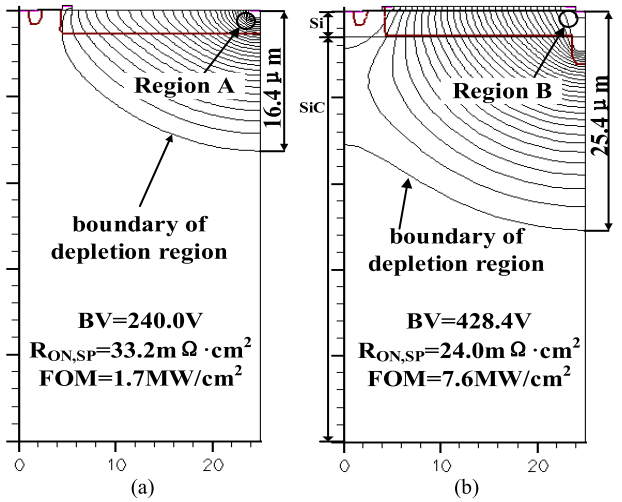

FIGURE 3. Equipotential lines distribution at breakdown of (a) Cov. LDMOS and (b) SIPOS Si/SiC LDMOS.

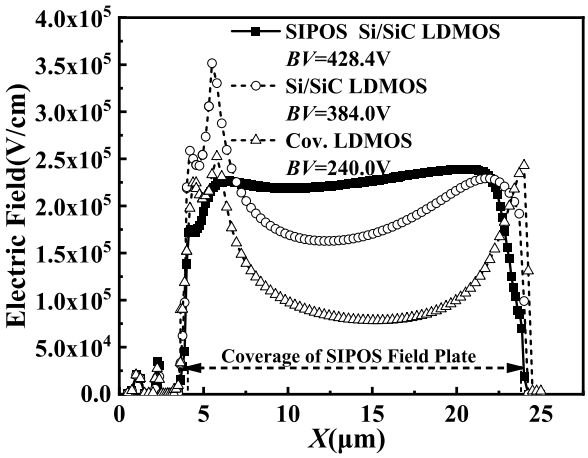

FIGURE 4. Electric field distributions of the optimized SIPOS Si/SiC LDMOS, Si/SiC LDMOS and Cov. LDMOS.

The lateral surface field distribution of Cov. LDMOS, Si/SiC LDMOS and SIPOS Si/SiC LDMOS is shown in Fig. 4. Both the Cov. LDMOS and Si/SiC LDMOS have U-shaped lateral surface electric field distributions due to the RESURF principle [24], which is shown in Fig. 4. Due to the optimization of BPT technology and SIPOS field plate, the lateral electric field distribution of SIPOS Si/SiC LDMOS is approximately a horizontal line. BPT technology can optimize the vertical electric field between gate-drain electrode and substrate electrode, and then improve the lateral electric field distribution. Furthermore, because of the electric field modulation effect of SIPOS field plate, the electric field at the surface of drift region can be forced to be evenly distributed. Therefore, the ideal lateral electric field distribution can be obtained, which leads to the increment of *BV*.

Fig. 5 shows the breakdown characteristic of Cov. LDMOS, Si/SiC LDMOS and SIPOS Si/SiC LDMOS. It

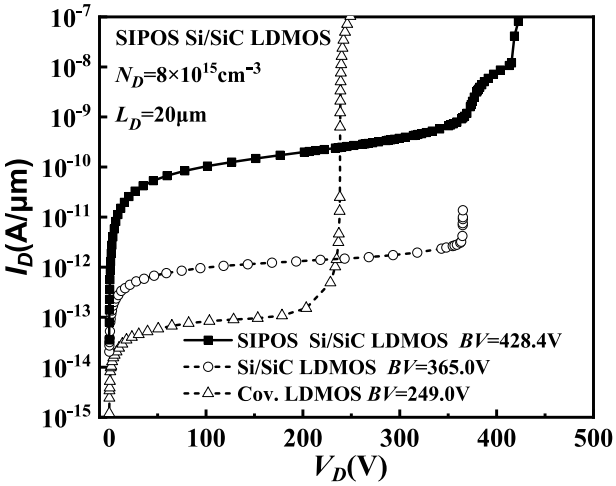

FIGURE 5. Breakdown characteristics for the three LDMOS in Off-State.

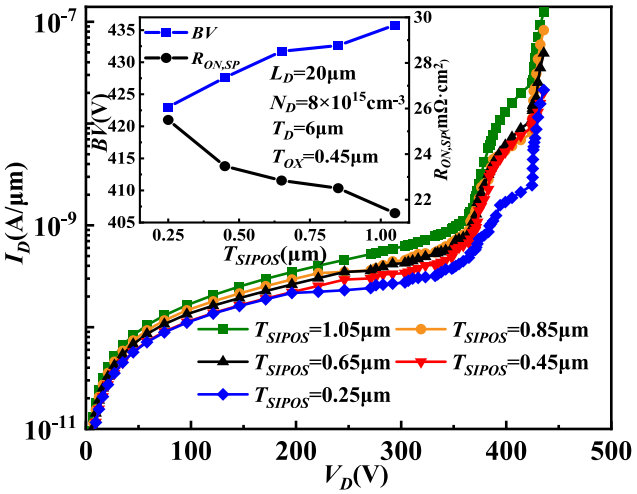

FIGURE 6. Influence of T_{SIPOS} on the characteristic of SIPOS Si/SiC LDMOS.

can be seen from Fig. 5 that with the optimization of SIPOS field plate, the BV of the proposed device reaches 428.4V. However, SIPOS layer also brings about problems which cannot be ignored. When the device is at the reverse state, the leakage current of the proposed device increases from 10^{-12}A of Si/SiC LDMOS to 10^{-10}A, which is because the SIPOS field plate is equivalent to parallel a high resistor to the drift region. Although the leakage current is considerably lower than the forward current of SIPOS Si/SiC LDMOS and can be controlled by increasing the resistivity of SIPOS layer, with the increase of the resistivity of SIPOS, its electric field modulation effect on the drift region will be weakened, and the BV will be reduced [25]. The increase of leakage current is an unavoidable problem for using SIPOS field plate as resistance field plate. In general, the oxygen content of SIPOS layer determines the electrical properties of SIPOS layer. When the oxygen content of SIPOS is in the range of 15% to 35%, the physical and chemical properties will be very stable [26], which is suitable to be used as resistance field plates.

The effect of T_{SIPOS} on the electrical characteristics of proposed device is shown in Fig. 6. The trade-off between BV and $R_{ON,SP}$ of the device is improved with the increase of T_{SIPOS}. Although SIPOS field plate can alleviate the contradiction between high BV and low $R_{ON,SP}$, the reverse breakdown current of the device increases accordingly, which can also be seen in Fig. 6. The influence of T_{SIPOS} on the electrical characteristics had been studied by previous researchers. According to their study, the BV increases with the rise of T_{SIPOS}. Meanwhile, the leakage current enlarges [27]. The simulation results in this paper show no difference with this conclusion.

In addition, SIPOS layer has an obvious effect on switching characteristics. The circuit with a resistive load, shown in Fig. 7, is used to simulate the switching characteristic of devices. In order to ensure that all simulation objects can work normally, we choose to set V_D as 100V, R_{load} as $2 \times 10^6\Omega$ and R_G as 5Ω. The voltage signal applied to gate electrode (V_G) is a square wave, with a high level of 10V and low level of 0V, which can control the switching of devices. The turn-on criterion is defined as an increment of I_D from 0 to 90% of $I_{D(sat)}$ (4.94×10^{-6}A/μm), which means the turn-on criterion $I_{on} = 4.446 \times 10^{-6}$A/μm. Similarly, the turn-off criterion is when I_D decrease from $I_{D(sat)}$ to 10% of $I_{D(sat)}$, which is 0.49×10^{-6}A/μm. Turn-off waveforms of the devices are shown in Fig. 7(a), the turn-off time (T_{off}) of SIPOS Si/SiC LDMOS and Si/SiC LDMOS are close, which are 7.38ns and 7.82ns, respectively. As is shown in Fig. 7(b), the turn-on time (T_{on}) of SIPOS Si/SiC LDMOS and Si/SiC LDMOS are 0.96ns and 0.38ns, respectively. The turn-on time of SIPOS Si/SiC LDMOS is 2.53 times that of Si/SiC LDMOS. This is mainly due to the impact of SIPOS layer. In Off-State, the internal electric field of SIPOS field plate assists in depleting the drift region and in On-State, effected by the internal electric field of SIPOS field plate, a majority carriers accumulation layer is formed on the surface of drift. These leads to the degradation of turn-on characteristics because it will take more time for the device to transition from enhanced depletion state to the majority carriers accumulation state. The optimization of transient characteristics needs to be further investigated.

The effect of T_{OX} on BV and $R_{ON,SP}$ is shown in Fig. 8. It can be seen from this figure that T_{OX} has a slightly impact on BV, but the value of $R_{ON,SP}$ has a nearly linear increase with the raise of T_{OX}. As for the influence on $R_{ON,SP}$, the main reason is that when the device is at on-state, the SIPOS field plate, oxide layer and majority carriers accumulation layer (on the surface of drift region) can be treated as a MOS capacitor [28]. With the increase of T_{OX} (the distance of two capacitor plates), the value of MOS capacitor decreases, so the amount of charge accumulated on the surface of drift is decreased in the same bias voltage, which leads to the rise of $R_{ON,SP}$. Therefore, from the simulation results, a low $R_{ON,SP}$

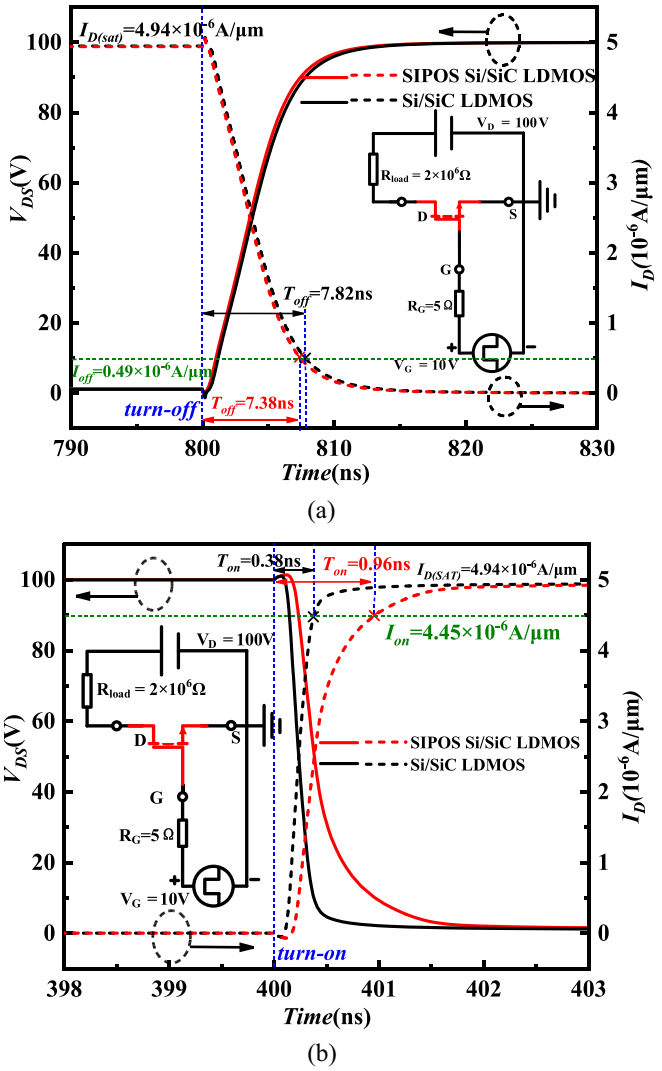

FIGURE 7. (a) Simulated resistive turn-off characteristics of Si/SiC LDOMS and the proposed SIPOS Si/SiC LDMOS. (b) Simulated resistive turn-on characteristics of Si/SiC LDOMS and the proposed SIPOS Si/SiC LDMOS.

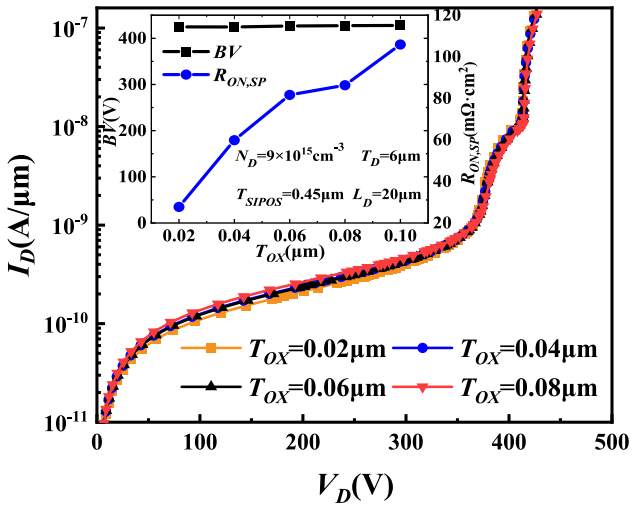

FIGURE 8. The influence of T_{OX} on the characteristic of SIPOS Si/SiC LDMOS.

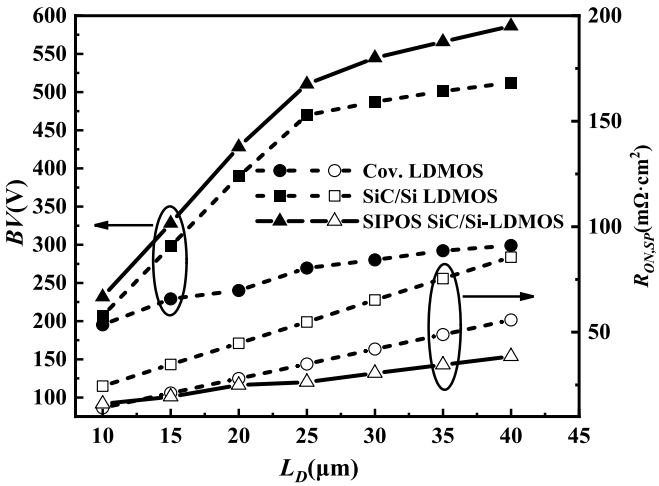

FIGURE 9. *BV* and $R_{ON,SP}$ versus L_D for three kinds of LDMOS.

can be achieved by reducing T_{OX}. However, Fig. 8 also shows that smaller T_{OX} induces a slight increase of reverse current, which will cause the degradation of reliability. And a smaller T_{OX} will increase the surface electric field, it also can easily cause the dielectric breakdown, which will make the proposed device lose its function. Moreover, according to the previous studies, the influence of oxide thickness on switching characteristics of devices cannot be ignored either [22]. Therefore, it is crucial to choose the proper T_{OX} to ensure the performance and reliability of the proposed device.

Fig. 9 shows the relationship between *BV*, $R_{ON,SP}$ and L_D. The *BV* and $R_{ON,SP}$ of the three devices both increase with the raise of L_D. The reason for this phenomenon is obvious. The increase of L_D means that the length of voltage-sustaining region increases accordingly, which also indicates that it can withstand higher reverse voltage.

What's more, it is worth noticing that the proposed SIPOS Si/SiC LDMOS has a steeper slope of *BV* than that of Cov. LDMOS. The electric field distribution of the proposed device is optimized uniform and smooth, since it can modulate the vertical and lateral electric field through the deep drain region and SIPOS field plate [13], [29]. So high *BV* can be obtained by increasing L_D. However, the problems caused by the increasing of L_D should not be ignored. As is shown in Fig. 9, the $R_{ON,SP}$ of all three devices are increased accordingly. This is because the drift resistance goes higher and becomes more dominant during the increasing of L_D. SIPOS Si/SiC LDMOS has the lowest $R_{ON,SP}$ in this three devices, which is attribute to the internal electric field of SIPOS field plate. When the device is at on-state, the internal electric field can attract the majority carries (electrons) and form a majority carriers accumulation layer on the surface of the drift region, which can effectively reduce $R_{ON,SP}$.

Fig. 10(a) shows the influence of T_D on figure of merit ($FOM = BV^2/R_{on,sp}$) and *BV* of SIPOS Si/SiC

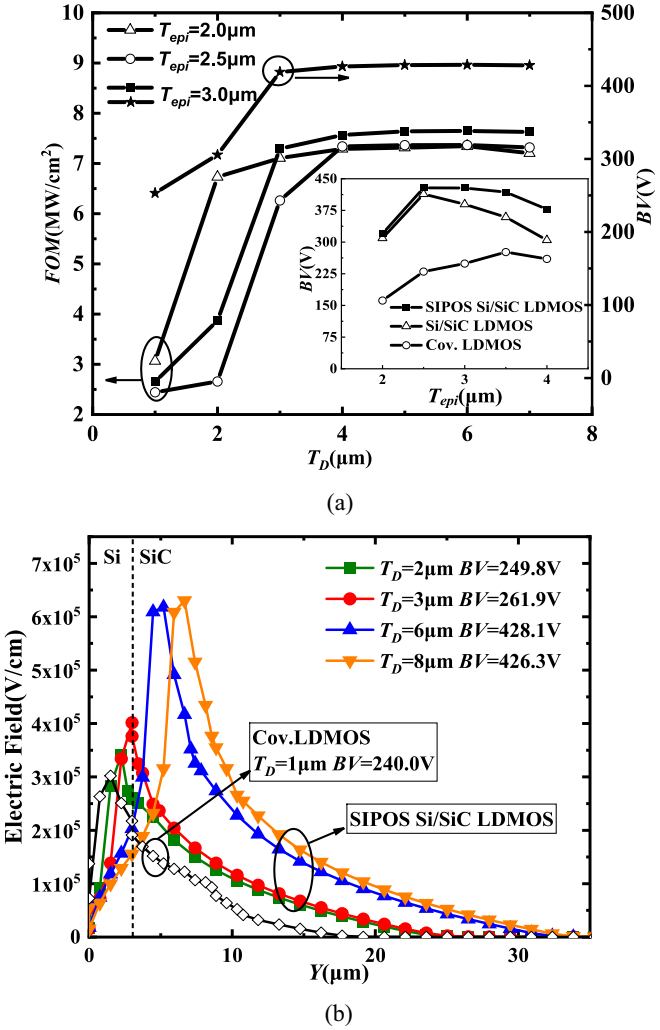

FIGURE 10. (a) *FOM* and *BV* as a function of T_D for SIPOS Si/SiC LDMOS (b) Electric field distributions of SIPOS Si/SiC LDMOS and Cov. LDMOS (X = 23μm).

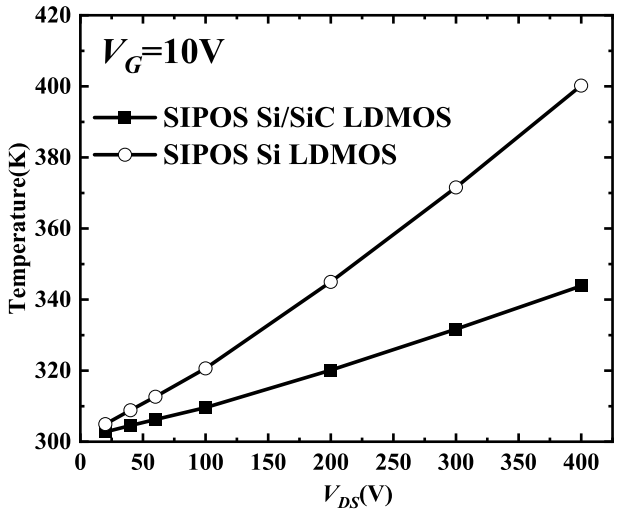

FIGURE 11. Temperature versus V_{DS} for SIPOS Si LDMOS and SIPOS Si/SiC LDMOS.

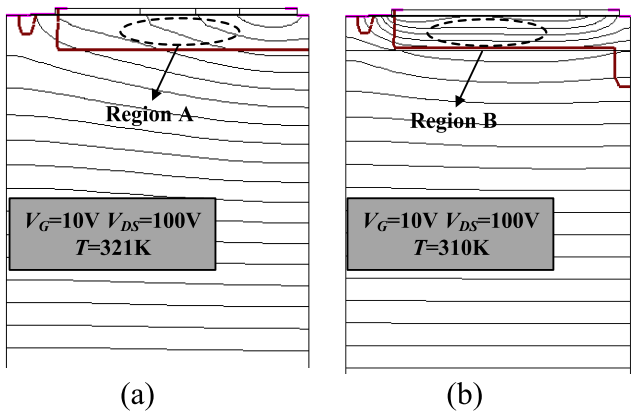

FIGURE 12. Isothermal distribution of (a) SIPOS Si LDMOS and (b) SIPOS Si/SiC LDMOS.

LDMOS. The *FOM* and *BV* of the device reach saturation when T_D increases to 4μm, which means increasing T_D after 4μm will not improve performance of the proposed device, on the contrary, it will increase process complexity. Furthermore, when the T_D is further deepened, the performance has slightly degraded. It can also be seen from Fig. 10(a) that the increase of T_{epi} can be regard as the decrease of T_D, which means that the proposed structure can achieve a better performance with a thinner epitaxial layer [20].

As is shown in Fig. 10(b), the T_D determines whether the highest electric field of the device appears in the Si material or SiC material. When T_D is greater than 3μm, the maximum electric field appears in SiC substrate, which means the BPT technology takes effect.

Temperature field of SIPOS Si LDMOS and SIPOS Si/SiC LDMOS has been simulated by ISE TCAD. We can clearly observe the trend of temperature versus V_{DS} for the two devices. In Fig. 11, as the V_{DS} increases, the operating temperature of SIPOS Si/SiC LDMOS devices is significantly lower than that of SIPOS Si LDMOS, due to the high thermal conductivity of SiC substrates. Fig. 12 shows the two-dimensional isotherm distribution of SIPOS Si/SiC LDMOS and SIPOS Si LDMOS at the same bias voltages, from which we can see the overall temperature distribution trend more intuitively. The isotherm distribution in the drift region (Region B) of SIPOS Si/SiC LDMOS becomes more uniform, compared with that of SIPOS Si LDMOS (Region A), which indicates the SiC substrate can dissipate the heat faster and avoid heat accumulation. It can be seen that the temperature characteristics of the proposed device have been significantly improved, especially in the high-power condition.

IV. CONCLUSION

In order to obtain high breakdown voltage and lower specific on-resistance, a novel Si/SiC heterojunction LDMOS with the SIPOS field plate is proposed in this paper. The Breakdown Point Transfer technology has been applied on

Si/SiC LMODS, which improved the breakdown voltage. According to the analysis of ISE TCAD, the breakdown voltage of SIPOS Si/SiC LDMOS is 428.4V, which is improved by 78.4% compared with 240.0V of conventional Si LDMOS with the same structure parameters; The specific on-resistance is optimized from $33.2\text{m}\Omega \cdot \text{cm}^2$ of conventional Si LDMOS to $24.0\text{m}\Omega \cdot \text{cm}^2$, decreased by 25%. Compared with the conventional Si LDMOS, the SIPOS Si/SiC LDMOS alleviates the trade-off between BV and $R_{ON,SP}$. The Si/SiC heterojunction also improves the temperature characteristics of the device especially in the high-power condition. However, there are also some problems to be solved, such as the large leakage current and the degradation of switching characteristic. To solve the problem thoroughly, more in-depth research is needed. But it is undenied that this novel device still has excellent characteristics of large breakdown voltage and small specific on-resistance, which are expected to be applied in high-voltage applications.

REFERENCES

[1] M. Mehrad, A. A. Orouji, and M. Taheri, "A new technique in LDMOS transistors to improve the breakdown voltage and the lattice temperature," *Mater. Sci. Semicond. Process.*, vol. 34, pp. 276–280, Jun. 2015, doi: 10.1016/j.mssp.2015.02.057.

[2] J. Zhang, Y.-F. Guo, D. Z. Pan, K.-M. Yang, X.-J. Lian, and J.-F. Yao, "Effective doping concentration theory: A new physical insight for the double-RESURF lateral power devices on SOI substrate," *IEEE Trans. Electron Devices*, vol. 65, no. 2, pp. 648–654, Feb. 2018, doi: 10.1109/TED.2017.2786139.

[3] A. W. Ludikhuize, "A review of RESURF technology," in *Proc. 12th Int. Symp. Power Semicond. Devices ICs*, Toulouse, France, 2000, pp. 11–18, doi: 10.1109/ISPSD.2000.856763.

[4] J. A. Appels and H. M. J. Vaes, "High voltage thin layer devices (RESURF devices)," in *Proc. Int. Electron Devices Meeting*, Washington, DC, USA, 1979, pp. 238–241, doi: 10.1109/IEDM.1979.189589.

[5] B. Duan, Z. Cao, X. Yuan, S. Yuan, and Y. Yang, "New superjunction LDMOS breaking silicon limit by electric field modulation of buffered step doping," *IEEE Electron Device Lett.*, vol. 36, no. 1, pp. 47–49, Jan. 2015, doi: 10.1109/LED.2014.2366298.

[6] G. Deboy, N. Marz, J.-P. Stengl, H. Strack, J. Tihanyi, and H. Weber, "A new generation of high voltage MOSFETs breaks the limit line of silicon," in *Proc. Int. Electron Devices Meeting Tech. Dig.*, San Francisco, CA, USA, 1998, pp. 683–685, doi: 10.1109/IEDM.1998.746448.

[7] C. W. Chan, F. Li, A. Sanchez, P. A. Mawby, and P. M. Gammon, "Comparative study of RESURF Si/SiC LDMOSFETs for high-temperature applications using TCAD modeling," *IEEE Trans. Electron Devices*, vol. 64, no. 9, pp. 3713–3718, Sep. 2017, doi: 10.1109/TED.2017.2719898.

[8] K. Shenai, R. S. Scott, and B. J. Baliga, "Optimum semiconductors for high-power electronics," *IEEE Trans. Electron Devices*, vol. 36, no. 9, pp. 1811–1823, Sep. 1989, doi: 10.1109/16.34247.

[9] P. G. Neudeck, "Progress in Silicon Carbide semiconductor electronics technology," *J. Electron. Mater.*, vol. 24, pp. 283–288, Apr. 1995, doi: 10.1007/BF02659688.

[10] R. Kirschman, "Status of silicon carbide (SiC) as a widebandgap semiconductor for hightemperature applications: A review," in *High-Temperature Electronics*. New York, NY, USA: Wiley, 1999, pp. 511–524, doi: 10.1109/9780470544884.ch69.

[11] L. Chen, O. J. Guy, M. R. Jennings, P. Igic, S. P.Wilks, and P. A. Mawby, "Study of a novel Si/SiC hetero-junction MOSFET," *Solid-State Electron.*, vol. 51, no. 5, pp. 662–666, May 2007, doi: 10.1016/j.sse.2007.02.026.

[12] B. Duan, J. Lv, Y. Zhao, and Y. Yang, "SiC/Si heterojunction VDMOS breaking silicon limit by breakdown point transfer technology," *Micro Nano Lett.*, vol. 13, no. 1, pp. 96–99, Jan. 2018, doi: 10.1049/mnl.2017.0444.

[13] S. Lotfi, L.-G. Li, Ö. Vallin, L. Vestling, H.Norström, and J. Olsson, "LDMOS-transistors on semi-insulating silicon-on-polycrystalline-silicon carbide substrates for improved RF and thermal properties," *J. Solid State Electron.*, vol. 70, pp. 14–19, Apr. 2012, doi: 10.1016/j.sse.2011.11.019.

[14] H. Shinohara, H. Kinoshita, and M. Yoshimoto, "Si metal-oxide-semiconductor field-effect transistor on Si-on-SiC directly bonded wafers with high thermal conductance," *J. Appl. Phys. Lett.*, vol. 93, no. 12, 2008, Art. no. 122110, doi: 10.1063/1.2991449.

[15] M. R. Jennings *et al.*, "Si/SiC heterojunctions fabricated by direct wafer bonding," *J. Electrochem. Solid-State Lett.*, vol. 11, no. 11, pp. H306–H308, 2008.

[16] P. M. Gammon, "Development of SiC heterojunction power devices," Ph.D. dissertation, Dept. Eng., Univ. Warwick, Coventry, U.K., 2011.

[17] P. M. Gammon *et al.*, "Development, characterisation and simulation of wafer bonded Si-on-SiC substrates," *Mater. Sci. Semicond. Process.*, vol. 78, pp. 69–74, May 2018, doi: 10.1016/j.mssp.2017.10.020.

[18] B. Duan, X. Yang, J. Lv, and Y. Yang, "Novel SiC/Si heterojunction power MOSFET with breakdown point transfer terminal technology by TCAD simulation study," *IEEE Trans. Electron Devices*, vol. 65, no. 8, pp. 3388–3393, Aug. 2018, doi: 10.1109/TED.2018.2849606.

[19] L. Sun, B. Duan, X. Yang, Y. Wang, and Y. Yang, "Analysis of the novel Si/SiC hetero-junction IGBT characteristics by TCAD simulation," *J. Superlattices Microstruct.*, vol. 122, pp. 631–635, Oct. 2018.

[20] B. Duan, Y. Huang, Y. Yang, and J. Xing, "Si/SiC heterojunction lateral double-diffused metal oxide semiconductor field effect transistor with breakdown point transfer (BPT) terminal technology," *Micro Nano Lett.*, vol. 14, no. 10, pp. 1092–1095, Sep. 2019.

[21] X. Wang, B. Duan, X. Yang, and Y. Yang, "Novel power MOSFET with partial SiC/Si heterojunction to improve breakdown voltage by breakdown point transfer (BPT) terminal technology," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 559–564, Jun. 2020, doi: 10.1109/JEDS.2020.2997086.

[22] D. Jaume, G. Charitat, J. M. Reynes, and P. Rossel, "High-voltage planar devices using field plate and semi-resistive layers," *IEEE Trans. Electron Devices*, vol. 38, no. 7, pp. 1681–1684, Jul. 1991, doi: 10.1109/16.85167.

[23] *ISE TCAD Release 10.0 DESSIS*, Integr. Syst. Eng., Zurich, Switzerland, 2004.

[24] S. G. Nassif-Khalil, L. Z. Hou, and C. A. T. Salama, "SJ/RESURF LDMOST," *IEEE Trans. Electron Devices*, vol. 51, no. 7, pp. 1185–1191, Jul. 2004, doi: 10.1109/TED.2004.829876.

[25] S.-K. Chung, "Analytic model for field-plate-edge breakdown of planar devices terminated with field plate and semiresistive layer," *IEE Proc. Sci. Meas. Technol.*, vol. 151, no. 1, pp. 21–24, Jan. 2004, doi: 10.1049/ip-smt:20030852.

[26] A. Mimura, M. Oohayashi, S. Murakami, and N. Momma, "High-voltage planar structure using SiO2-SIPOS-SiO2film," *IEEE Electron Device Lett.*, vol. 6, no. 4, pp. 189–191, Apr. 1985, doi: 10.1109/EDL.1985.26092.

[27] T. Matsushita *et al.*, "Highly reliable high-voltage transistors by use of the SIPOS process," *IEEE Trans. Electron Devices*, vol. 23, no. 8, pp. 826–830, Aug. 1976, doi: 10.1109/T-ED.1976.18494.

[28] D. A. Neamen, *Semiconductor Physics and Devices Basic Principles*, Beijing, China: Publ. House Electron. Ind., 2013

[29] S. Yuan, B. Duan, H. Cai, Z. Cao, and Y. Yang, "Novel LDMOS with assisted deplete-substrate layer consist of super junction under the drain," in *Proc. 29th Int. Symp. Power Semicond. Devices IC's (ISPSD)*, Sapporo, Japan, 2017, pp. 279–282, doi: 10.23919/ISPSD.2017.7988951.