

# Novel Soft-Switching DC–DC Converter with Full ZVS-Range and Reduced Filter Requirement— Part I: Regulated-Output Applications

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**Abstract**—A novel soft-switching topology for dc–dc converters is proposed. It is well suited for applications in the range of a few hundred watts to a few kilowatts. It is essentially a hybrid combination of an uncontrolled half-bridge section and a phase-shift controlled full-bridge section, realized with just four switches. The main features of the proposed topology are zero-voltage-switching down to no-load without serious conduction loss penalty, constant frequency operation and near-ideal filter waveforms. The improved filter waveforms result in significant savings in the input and output filter requirement, resulting in high power-density. The new topology requires two transformers and two dc-bypass capacitors. The combined VA rating of the two transformers is more than that of the single transformer of conventional full-bridge converters, for variable-input applications. In Part I of the paper, the converter operation is analyzed for typical switch-mode power supply applications, where the input voltage varies widely but the output voltage is fixed and is well regulated. Experimental results obtained from a 100-W/200-kHz proof-of-concept prototype confirm the superior features of the proposed hybrid configuration.

**Index Terms**—DC–DC converters, hybrid converters, phase-shifted full-bridge, zero-voltage-switching.

## I. INTRODUCTION

THE phase-modulated full-bridge converter (PMC) [1]–[3] is a preferred topology for dc–dc power-conversion, especially at power levels above a few hundred watts. Its main attractive features are zero-voltage turn-on switching (ZVS), constant switching frequency and simple control similar to that of the hard-switched full-bridge PWM converter. The main disadvantage of the phase-modulated converter is that achieving ZVS below, for example, one-half load is at the expense of significant increase in the conduction losses [4].

The schematic diagram of the conventional PMC is shown in Fig. 1(a), and the idealized waveforms of the transformer voltage and primary current are shown in Fig. 1(b). Zero-voltage-switching is achieved relying mainly on the transformer primary current to charge/discharge the appropriate switch capacitances just prior to turn-on. From ZVS point of view, the left-leg switches ( $T_A^+$  and  $T_A^-$ ) and the right-leg switches ( $T_B^+$  and  $T_B^-$ ) operate under significantly different conditions. The right-leg switches undergo turn-on/turn-off

during the transition from the power-transfer interval to the freewheeling interval, while the left-leg switches turn on/off during the transition from the freewheeling interval to the power-transfer interval. As shown in Fig. 1(b), during the right-leg transition, the transformer primary current does not change direction and remains in the proper direction to achieve discharging of the appropriate switch capacitance to achieve ZVS. However, during the left-leg transition the current reduces and eventually changes polarity. Therefore, the energy available for charging/discharging the switch capacitance is less, and hence, achieving ZVS for the left-leg switches is more difficult. The energy available is a function of the load current, and at light-loads ZVS is lost [1]–[4].

There are two main ways by which the ZVS load range can be increased in the conventional PMC. The first approach is to make the leakage inductance of the transformer very large or to add an external inductor in series with the transformer primary. This approach, while extending the ZVS load-range, results in high loss of volt-seconds, requiring the transformer turns-ratio to be compromised. The net result is increased switch current and conduction losses. Use of saturable inductors [5], [6] instead of linear inductors reduces the volt-seconds lost to a certain extent, but still cannot achieve ZVS at very light loads. The second approach to increasing the ZVS load range is to increase the magnetizing current of the transformer. In conventional PMC, this results in significant increase in the rms switch current, since during the entire freewheeling interval the magnetizing current circulates through the switches at its peak value.

Therefore, in conventional PMC, ZVS at light-loads is achieved only at the expense of increased conduction losses. Many modifications of the basic PMC have been proposed to extend the ZVS range down to very light loads, with smaller penalty on conduction losses. A commutation aid network consisting of an external inductor in series with the primary of the transformer and two clamping diodes is proposed in [7], [8]. Use of saturable inductors along with increased magnetizing current is discussed in [5] and secondary-side control using mag-amps is suggested in [9].

A novel hybrid full-bridge converter that achieves ZVS right down to no-load without serious conduction loss penalty was proposed in [10]. Apart from the improved soft-switching characteristics, another distinguishing feature of this hybrid converter is that the filter waveforms, both at the input and the output are close to ideal (which is pure dc). Hence, the filter requirements are significantly less. The present paper is a more

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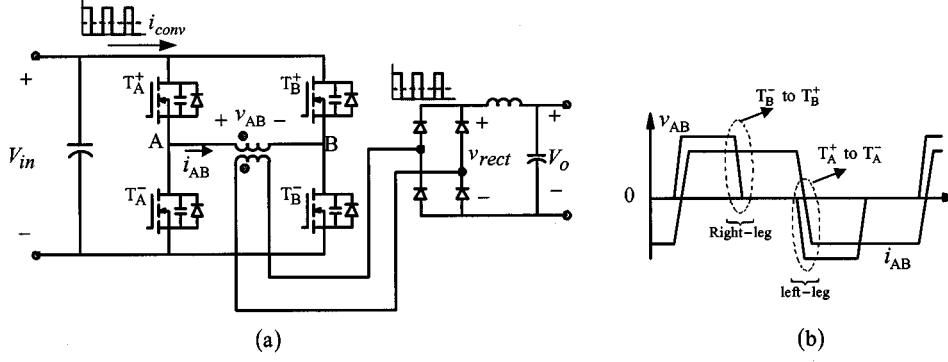


Fig. 1. Conventional phase-modulated full-bridge converter (PMC): (a) schematic diagram and (b) waveforms of transformer primary voltage and current.

complete presentation of the hybrid configuration proposed in [10].

## II. PROPOSED CONFIGURATION

The schematic diagram of the proposed configuration is shown in Fig. 2. As seen, it is a hybrid combination of a half-bridge section, comprising of the switches  $T_A^+$  and  $T_A^-$ , and the transformer  $T_1$ , and a full-bridge section comprising of the switches  $T_A^+$ ,  $T_A^-$ ,  $T_B^+$  and  $T_B^-$ , and the transformer  $T_2$ . Since the switches  $T_A^+$  and  $T_A^-$  are common to both the sections, the hybrid combination is realized using just four switches as in a regular full-bridge converter (with the same total switch ratings). The output of each section is added at the secondary, rectified and filtered to obtain regulated dc output.

As will be explained in detail in later sections, the half-bridge section is uncontrolled (i.e., operates with full pulse-width always) while the pulse-width of the full-bridge section is controlled by varying the phase-shift between the two legs, A and B. All the four switches are operated at fixed 50% duty-ratio (neglecting the small time-delay provided to achieve ZVS transitions) and constant switching frequency.

## III. PRINCIPLE OF OPERATION

The principle of operation of the proposed converter is explained using the idealized waveforms shown in Fig. 3. Since all the switches are operated at fixed 50% duty-ratio, the voltage across transformer  $T_1$ ,  $v_{T_1}$  is a pure square wave with full pulse-width. The phase-shift between the two legs—A and B, is controlled, therefore the voltage across the transformer  $T_2$ ,  $v_{T_2}$  is a pulse-width-modulated waveform, as shown in Fig. 3. When these two transformer voltages are added at the secondary, the four-step waveform,  $v_{\text{bridge}}$  results. Rectifying this voltage results in  $v_{\text{rect}}$ , which as seen in Fig. 3, is close to the ideal waveform (steady dc), with significantly lower high-frequency content compared to the conventional converters.

As mentioned earlier, the output is regulated against variations in the input voltage and load, by suitably varying the phase-shift and hence the pulse-width of the full-bridge section. The turns-ratios of the two transformers are designed based on the range of variation in the input voltage and the output. The turns-ratio of  $T_1$  is chosen such that at the maximum input voltage ( $V_{\text{in, max}}$ ), its secondary voltage just equals the desired

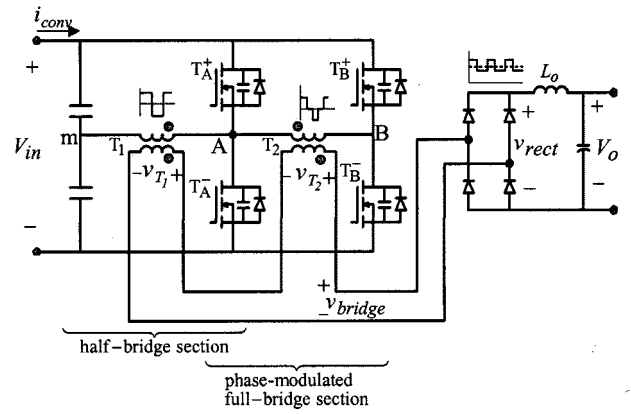


Fig. 2. Schematic diagram of the proposed configuration.

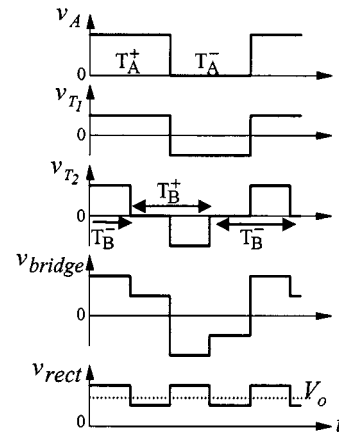


Fig. 3. Idealized waveforms of the proposed configuration.

output voltage,  $V_o$ . At maximum input voltage, the full-bridge section operates with zero pulse-width, and hence does not contribute to the output voltage. As the input voltage drops from the maximum value, the contribution from  $T_1$  to the output voltage drops proportionately, and the full-bridge section delivers the balance of the output, by suitably increasing its pulse-width. The turns-ratio of  $T_2$  is chosen such that the full-bridge section can deliver the balance of the output right down to the minimum

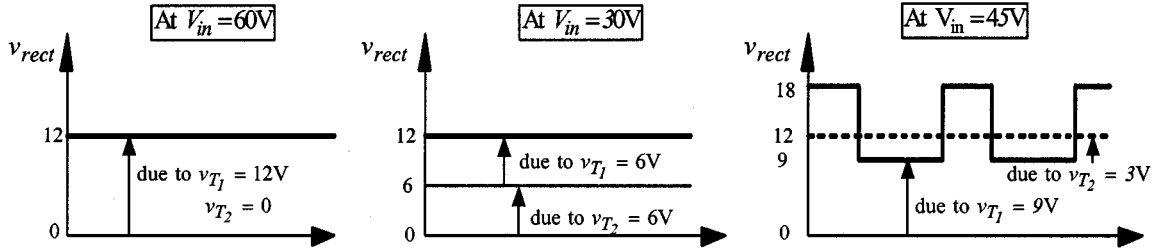


Fig. 4. Rectifier output waveform at different input voltages.

input voltage ( $V_{in, \min}$ ). Hence, the turns-ratio for the two transformers are given by

$$n_1 \frac{V_{in, \max}}{2} = V_o \quad (1)$$

$$n_1 \frac{V_{in, \min}}{2} + n_2 V_{in, \min} = V_o \quad (2)$$

where  $n_1$  and  $n_2$  are the turns-ratios of the transformers  $T_1$  and  $T_2$  respectively. As a specific example consider the following specifications (used in the prototype).

Input voltage 30 V to 60 V dc.

Output voltage 12 V regulated.

When the input is at 60 V, the contribution from  $T_1$  is to be 12 V. Hence the turns-ratio of  $T_1$  is 0.4. When the input voltage falls to 30 V, contribution from  $T_1$  drops proportionately to 6 V and  $T_2$  has to contribute the balance 6 V. Therefore, the turns-ratio of  $T_2$  is 0.2. It may be noted that in the above analysis, the effect of leakage inductance has been neglected in order to explain the operating principles clearly. In the actual converter, the effect of leakage inductance and resulting volt-sec loss have to be considered while selecting the transformer turns-ratios. Especially at high switching frequencies the loss of volt-seconds can be significant.

Fig. 4 shows the idealized rectifier output voltage,  $v_{rect}$  corresponding to three different input voltages. As seen, the waveforms are close to the desired steady dc voltage under all operating conditions. The input current drawn by the converter also has similar waveforms as those shown in Fig. 4 (neglecting the magnetizing current of the transformers).

The input-output relationship for the converter is given by (3). The small-signal model of the converter, as well as the controller design are similar to that of the regular phase-modulated full-bridge converter (PMC)

$$V_o = n_1 \frac{V_{in}}{2} + D n_2 V_{in} \quad (3)$$

where  $D$  is the duty-ratio of the full-bridge output.

#### IV. REDUCED FILTER REQUIREMENT

Fig. 5 compares the waveforms ( $v_{rect}$ ) seen at the output LC filter, for the conventional and proposed configurations, corresponding to the input-output specifications given in Section III.

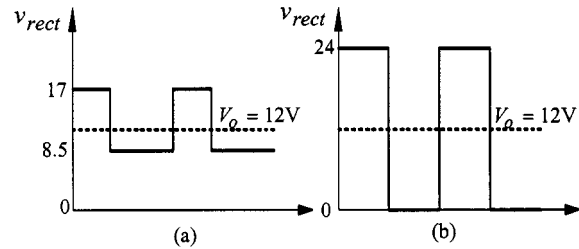


Fig. 5. Worst-case rectifier output waveform: (a) proposed configuration and (b) conventional PMC.

Due to the improved waveforms, the filter requirement in the proposed configuration is significantly less. The exact reduction in the filter requirement is a function of the range of input voltage variation.

The peak-to-peak ripple in the output inductor current for the conventional PMC and the proposed hybrid converter at any given input voltage is given by (4) and (5), respectively

$$i_{L_{pk-pk}, PMC} = \frac{V_o(1 - D_{PMC}) \frac{T_s}{2}}{L_o} \quad (4)$$

where  $D_{PMC}$  is the duty-ratio of the  $v_{rect}$  waveform and is given by  $D_{PMC} = V_{in, \min}/V_{in}$ :

$$i_{L_{pk-pk}, Hybrid} = \frac{\left(V_o - n_1 \frac{V_{in}}{2}\right) (1 - D_{Hybrid}) \frac{T_s}{2}}{L_o} \quad (5)$$

where  $D_{Hybrid}$  is obtained from (3).

Fig. 6 shows the peak-to-peak inductor current (in per-unit of full-load current) for the PMC and the proposed configuration at various input voltages, based on (4) and (5). As seen, the ripple current increases monotonically in the case of PMC, while for the hybrid configuration, it reaches a maximum at some critical input voltage and reduces beyond that. At both the minimum and the maximum input voltages, the ripple current is zero. The worst-case ripple in the new configuration is significantly lower compared to that of the PMC. The critical voltage, at which the maximum ripple occurs for the new configuration, is given by (6) and is derived in Appendix A

$$V_{in, worst} = \sqrt{V_{in, \min} V_{in, \max}} \quad (6)$$

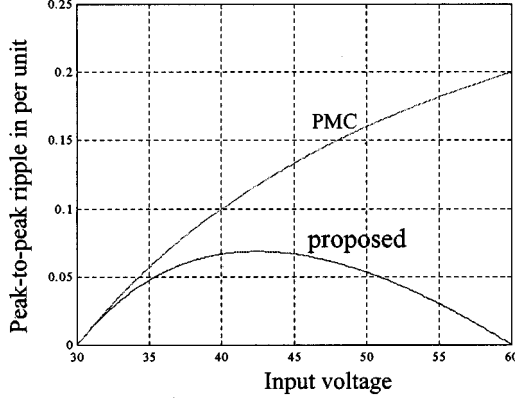


Fig. 6. Peak-to-peak inductor ripple current as a function of input voltage.

For PMC, the worst-case ripple occurs at the maximum input voltage. The savings in the inductance requirement in the proposed converter, to limit the worst-case ripple to a given value, compared to PMC, depends on the range of input variation and can be estimated using (4)–(6). Fig. 7 shows quantitatively the savings in the inductor requirement as a function of the range of input variation. For example, for a 1 : 2 variation in the input (i.e.,  $V_{in, max}/V_{in, min} = 2$ ), the inductor requirement reduces by a factor of about three. Apart from reducing the overall size and cost, smaller output inductor also helps to achieve better dynamic performance.

Since the input current drawn by the hybrid converter has similar waveform as that of  $v_{rect}$ , there is a similar saving in the input inductor requirement also. However, the combined VA rating of the two transformers in the hybrid converter is more than the VA rating of the single transformer of the conventional PMC. The exact increase, once again, depends on the range of input variation. For a 1 : 2 variation in the input, the combined rating of the two transformers of the hybrid converter is 1.5 times that of the transformer of the conventional PMC. However, the overall magnetics requirement—considering the transformer, input and output inductors and any inductance needed for ZVS—is smaller in the proposed hybrid converter. Also, as discussed in Part II of this paper, for applications where the input is fairly constant and the output needs to vary widely, the combined rating of the two transformers is the same as that of the single transformer of conventional converters, while the filter requirement is significantly less.

## V. ZVS CHARACTERISTICS OF THE PROPOSED CONVERTER

The mechanism of zero-voltage-switching in the proposed hybrid converter is similar to that of the conventional PMC, in that it relies on the transformer primary current to charge/discharge the appropriate switch capacitance just prior to turn-on. However, the main feature of the proposed hybrid converter is that ZVS can be achieved right down to no-load without significant increase in the conduction losses. Just as in PMC, in the new configuration also achieving ZVS for the left-leg switches is more difficult, since the load current changes direction during the left-leg transitions [see Fig. 1(b)]. However

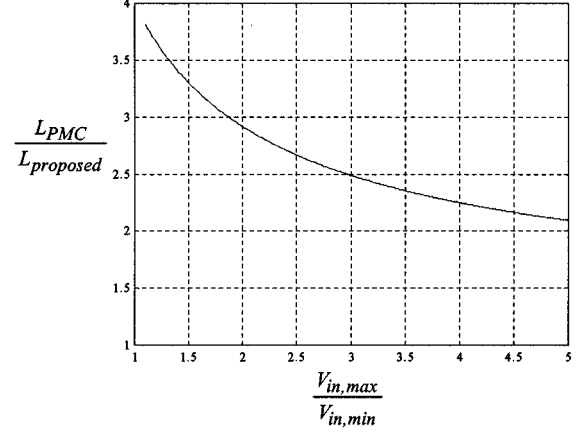


Fig. 7. Savings in filter requirement versus range of input variation.

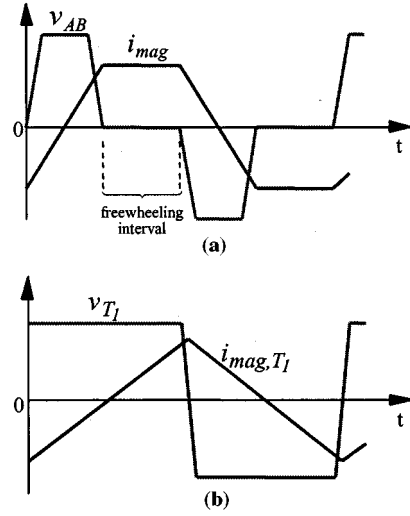


Fig. 8. Magnetizing currents (a) conventional PMC and (b) proposed configuration.

in the new configuration, ZVS is achieved relying mainly on the magnetizing current,  $i_{mag, T_1}$  of the transformer  $T_1$ , which is purposely made large. Unlike in PMC, this large magnetizing current does not appreciably increase the conduction losses, as explained in Section V-A. The magnetizing current of transformer  $T_2$  is designed to be as small as possible. Also, for typical specifications, no series inductance is required, and hence the volt-second lost is minimum, corresponding to the inherent leakage inductance of the transformers.

### A. Superior Characteristics of the Magnetizing Current of $T_1$ of the New Configuration

Fig. 8 compares the magnetizing current of transformer  $T_1$ ,  $i_{mag, T_1}$  of the new configuration with that of the conventional PMC. In the new configuration, increasing  $i_{mag, T_1}$  does not result in significant conduction loss penalty mainly due to the following reasons.

- 1) In conventional PMC, the main reason for the significant increase in the conduction losses with increased magnetizing current is that during the entire freewheeling

interval, the magnetizing current circulates at its peak value through the transformer primary and the switches, as shown in Fig. 8. The result is a pronounced increase in the RMS value of the transformer as well as the switch currents. In the proposed hybrid configuration, there is no corresponding freewheeling interval in the magnetizing current of transformer  $T_1$ , as seen in Fig. 8. Also, within a half-switching-period, the average value of  $i_{mag, T_1}$  is zero, and its contribution to the total rms current at large loads is negligible. For example, consider a magnetizing current of amplitude equal to 60% of the maximum reflected load current, and operation at a duty-ratio of 0.4. The increase in the conduction losses in the switches as well as in the transformer primary due to this magnetizing current, in the new configuration, is only 12%. Under identical conditions, the increase in conduction losses in conventional PMC is 98%.

- 2)  $i_{mag, T_1}$  in the new configuration does not flow through the right-leg switches where large magnetizing current is not required, thus significantly reducing the total conduction losses.
- 3) In conventional PMC, the peak value of magnetizing current does not vary with the input voltage. The magnetizing current of  $T_1$  of the new converter increases with the input voltage. This is desirable, since the energy needed to achieve ZVS also increases with input voltage.

Due to the above advantages,  $i_{mag, T_1}$  in the new configuration can be made large, thus achieving ZVS for the critical left-leg switches even at no-load, without significant conduction loss penalty. Reference [11] suggests the use of an inductor across the midpoint of the split capacitor (point “m”) and the center-point of each of the two legs, to aid in ZVS. The magnetizing current of this inductor has the above desirable characteristics. However, to achieve ZVS down to no-load the magnetizing current required can be quite high, typically above 60% of the full-load reflected load current (in both the proposed configuration as well as that of [11]). Therefore the rms current, and hence the VA rating of the inductor can be quite significant. In the proposed configuration the transformer, which provides the magnetizing current is also used for a major part of the power transfer. Since the load current and the magnetizing current are not in phase, the increase in the rms current rating of the transformer due to the large magnetizing current is negligible. Also, as explained earlier, due to the hybrid arrangement, the filter requirement in the new configuration is significantly lower than the conventional converters.

### B. Analysis of Left-Leg Transition

In the following analysis of the left-leg transitions, the effect of parasitic capacitance of the transformer and the junction capacitance of the secondary-side diodes have been neglected. Also, for simplicity, the capacitances across the primary-side switches are assumed linear and equal.

Consider the switches  $T_A^+$  and  $T_B^+$  in Fig. 2 gated on initially. The half-bridge portion delivers power to the output and its magnetizing current is increasing in the positive direction, while in the full-bridge portion the reflected load current just freewheels

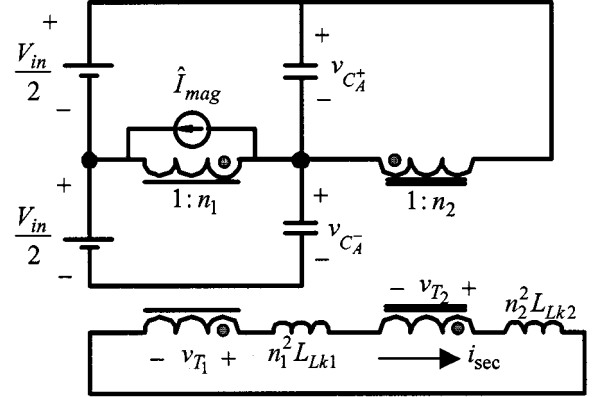


Fig. 9. Equivalent circuit corresponding to the resonant interval of the left-leg transition.

through  $T_A^+$  and the body-diode  $D_B^+$ . The left-leg transition begins when  $T_A^+$  is turned off. In conventional PMC, as soon as  $T_A^+$  is turned off, the transformer voltage becomes negative and the reflected load current begins to fall resonantly [4]. In the new configuration, the transformer voltage of the half-bridge section still remains positive, and the sum of the two secondary voltages becomes negative only when the voltage across  $T_A^+$ , ( $v_{C_A}^+$ ) reaches  $V_{start}$  given by

$$V_{start} = V_{in} \frac{n_1}{2(n_1 + n_2)}. \quad (7)$$

For the turns-ratios obtained in Section III,  $V_{start}$  is 33% of the final value. Hence only 67% of the voltage across the capacitance needs to be discharged resonantly, which is a significant advantage compared to the conventional PMC. When  $v_{C_A}^+$  reaches  $V_{start}$ , the sum of the secondary voltages becomes negative and all the four secondary side diodes conduct, effectively shorting the series-connected secondary windings. The corresponding equivalent circuit of this resonant interval is shown in Fig. 9. The expression for  $v_{C_A}^+$  is given by (8) and is derived in Appendix B

$$v_{C_A}^+(t) = [\hat{I}_{mag} + (n_1 + n_2)I_o] \sqrt{\frac{L_{eq, pri}}{C_{eq}}} \sin(\omega t) + V_{start} \quad (8)$$

where

$$\omega = \frac{1}{\sqrt{L_{eq, pri} C_{eq}}}; \quad L_{eq, pri} = \frac{L_{Lk1} n_1^2 + L_{Lk2} n_2^2}{(n_1 + n_2)^2}.$$

$C_{eq} = C_A^+ + C_A^- = 2C_A^+$ ;  $L_{Lk1}$ ,  $L_{Lk2}$ -leakage inductances of  $T_1$  and  $T_2$  respectively referred to the primary. This resonant interval ends when  $v_{C_A}^+$  reaches  $V_{in}$  or if the secondary current reaches  $-I_o$  before  $v_{C_A}^+$  reaches  $V_{in}$ .

Equation (8) is similar to that of conventional PMC in the left-leg resonant transition interval, except for the initial voltage in the capacitor  $C_A^+$  (equal to  $V_{start}$ ). The design of the amplitude of the magnetizing current of  $T_1$  and the value of  $L_{eq}$  (usually just the leakage inductances) is done such that the amplitude of the resonant swing represented by (8) is equal

to  $(V_{in, max} - V_{start})$ , even at no-load. At no-load, during the left-leg transition  $C_A^+$  charges linearly at a rate proportional to the amplitude of the magnetizing current as given in (9)

$$v_{C_A^+}(t) = \frac{\hat{I}_{mag} t}{C_{eq}}. \quad (9)$$

Therefore, as the first iteration, the amplitude of the magnetizing current can be chosen to satisfy (9), with the delay time  $T_d$  set equal to the sum of one-fourth of the resonant period and the time for  $v_{C_A^+}$  to reach  $V_{start}$ . The value of the leakage inductance can be determined based on the desired delay time  $T_d$ . The value of the magnetizing current and the series inductance needed are lower than in the conventional PMC because of the lower voltage amplitude (for the resonant swing) required. It should be noted that the main advantage of the proposed configuration is that even a large magnetizing current does not significantly contribute to the total conduction losses.

### C. Right-Leg Transition

Just as in PMC, in the new configuration also the reflected load current always aids in ZVS for the right-leg switches, and hence it is easy to achieve ZVS for the right-leg switches. However, if ZVS is dependant only on the load current, then at extremely light loads, the long delay times needed for the charging/discharging of the capacitances of the right-leg switches may not be practical. Hence it is preferable to have a small inductor connected between the mid-point of the split capacitor to the mid-point of the right leg. It may be noted that the magnetizing current of  $T_2$  cannot be relied upon to charge/discharge the right-leg MOSFET's, since the voltage across  $T_2$  varies from full pulse-width to zero. Near zero pulse-widths, the magnetizing current is too small to achieve ZVS transitions. In the proposed configuration, the current ratings of the switches of the two legs are not symmetrical. The current rating of the right-leg switches is  $n_2/(n_1 + n_2)$  times the rating of the left-leg switches. For a 1 : 2 variation in the input, the current rating of the right-leg switches is one-third of the left-leg switches. Therefore, the intrinsic as well as the external capacitance across the right-leg switches is much lower, requiring very small current to achieve complete discharge at turn-on. The peak current through the extra inductor is typically less than 20% of the load-current component of the right-leg switches. Therefore, the rating of the extra inductor for the right-leg switches is very small, about 6% of the total VA rating of the converter.

## VI. PRACTICAL CONSIDERATIONS

The four-diode output rectifier scheme as shown in Fig. 2, with two diodes conducting at any given time is not suitable for applications requiring low output voltages. The scheme shown in Fig. 10 with two-diode rectifier, similar to the center-tapped rectifiers in conventional configurations is suitable for such applications. It has identical ZVS characteristics as that of the configuration of Fig. 2 and results in similar reduction in the filter requirement. Current-doubler rectifier configuration, which results in better utilization of the transformer, can also be used

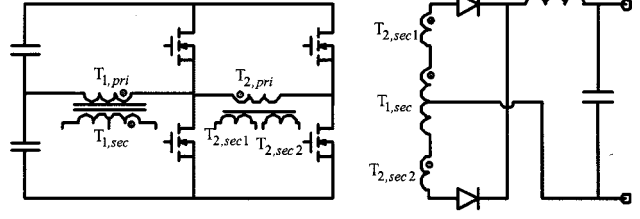


Fig. 10. Configuration with two-diode output rectifier.

for the low output voltage applications. Synchronous rectification, which results in very low rectifier conduction losses, is also equally applicable to the proposed configuration.

One of the drawbacks of conventional PMC is the ringing of the junction capacitance of output diodes with the large series inductance introduced for ZVS, resulting high voltage-stress across the diodes. This drawback is present in the new configuration as well. However, since the series inductance required is much less for the new configuration, the energy involved is correspondingly less, and it becomes practical to use R-C snubber networks to reduce the voltage stress across the output diodes. Also, saturable reactors can be effectively used to reduce the ringing and the associated losses just as in conventional PMC [5], [6].

During start-up and during overload/short-circuit conditions, when the output voltage needs to be below the normal specified value, it becomes necessary to control the normally uncontrolled half-bridge section also. This does not require any elaborate control circuitry. The gate signals to the switches are normally fully enabled, but under the above conditions, they are enabled only when the diagonal switches are gated ON. With this arrangement all the four switches operate in duty-ratio controlled mode (like hard-switched full-bridge converter) during the abnormal conditions and the output can be controlled right down to zero volts.

## VII. EXPERIMENTAL RESULTS

A prototype with the following specifications was built using the configuration shown in Fig. 10.

Input voltage	30 V to 60 V dc.
Output voltage	12 V dc regulated.
Maximum output power	100 W.
Switching frequency	200 kHz.
ZVS Range	Full-load to no-load.

For the left-leg switches, IRF540 with an external capacitance of 3.3 nF were used, and for the right-leg, IRF530 with an external capacitance of 1 nF were used. The transformer turns-ratio and filter inductors were designed as per the procedure outlined in Sections III and IV. The magnetizing current needed to achieve ZVS down to no-load was about 60% of the reflected load current and no external series inductor was added. Commercially available phase-shift IC (ML4828 from Micro Linear) was used for the controller. The closed loop compensator was designed based on the same principles as the conventional PMC.

Fig. 11(a) shows the primary voltages of the two transformers, corresponding to minimum input voltage and

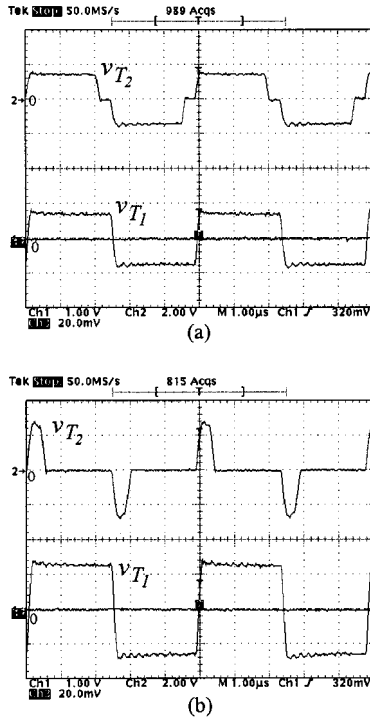


Fig. 11. Transformer voltages (a) at low input voltage and (b) at high input voltage.  $v_{T1}$ : 20 V/div,  $v_{T2}$ : 40 V/div; Hori: 1  $\mu$ s/div.

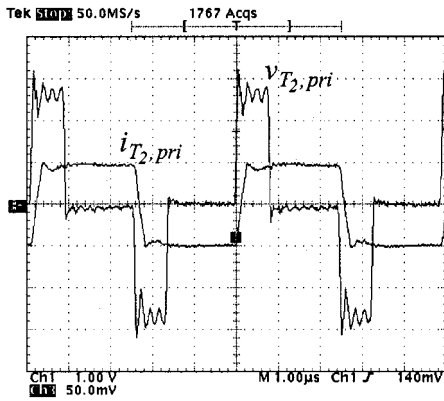


Fig. 12. Primary voltage and current of transformer  $T_2$ . 20 V/div, 2 A/div; Hori: 1  $\mu$ s/div.

Fig. 11(b) shows the same voltages corresponding to the maximum input voltage. As seen, the half-bridge is uncontrolled, while the pulse-width of the full-bridge output is modulated to regulate the output voltage. Fig. 12 shows the primary voltage and current of the full-bridge transformer at full-load.

Fig. 13 shows the rectifier output waveform,  $v_{rect}$ , the final output voltage,  $V_o$  and the ripple component of the output inductor current, at the minimum, intermediate and high input voltages. As seen, the rectifier output waveform is instantaneously close to the average value ( $V_o$ ), resulting in very little ripple in the inductor current, even with a small value of inductance (9  $\mu$ H). Also as seen, the peak-to-peak magnitude of the ripple current is lower at either extremes and is maximum at the intermediate input voltage.

Fig. 14(a) and (b) show the gate-to-source and drain-to-source voltages of a left-leg MOSFET and a right-leg MOSFET respectively, during turn-on, at 3% load. As seen, the drain voltage falls to zero well before the gate voltage reaches threshold, demonstrating ZVS turn-on. ZVS is achieved easily at higher loads. This proof-of-concept prototype was not optimized to achieve the maximum possible efficiency. The measured efficiency at full-load and low input voltage is 86%. The efficiency remains fairly constant down to light loads below 20% load. As expected the dominant losses are in the output rectification stage, where 100-V Schottky diodes are used.

### VIII. CONCLUSIONS

A novel soft-switching dc-dc converter is proposed. It is a hybrid combination of an uncontrolled half-bridge section and a phase-shift controlled full-bridge section, realized using just four switches. It achieves zero-voltage-switching down to no-load without serious conduction loss penalty, due mainly to the superior characteristics of the magnetizing current of the uncontrolled half-bridge transformer. The proposed configuration also results in near-ideal filter waveforms, thus significantly reducing the filter requirement both at the input and at the output sides. The operating principles and the ZVS characteristics of the proposed configuration are analyzed for variable input, constant-output applications. Experimental results obtained from 100-W/200-kHz prototype confirm the superior features of the proposed configuration.

The converter discussed in this paper is the subject of a U.S. Patent application [12].

### APPENDIX A

#### DERIVATION OF WORST-CASE INPUT VOLTAGE AT WHICH THE MAXIMUM RIPPLE CURRENT OCCURS

The design equations for choosing the turns-ratios for the two transformers of the proposed configuration are given in Section III [(1) and (2)], which give the following expressions:

$$n_1 = \frac{2V_o}{V_{in,max}} \quad (A1)$$

$$n_2 = V_o \left( \frac{1}{V_{in,min}} - \frac{1}{V_{in,max}} \right). \quad (A2)$$

Using (3) of Section III, and (A1) and (A2), the duty-ratio,  $d$  can be expressed in terms of the minimum and maximum input voltages as

$$D = \frac{V_{in,max} - V_{in}}{V_{in,max} - V_{in,min}} \frac{V_{in,min}}{V_{in}}. \quad (A3)$$

The voltage across the output inductor when both the half-bridge and the full-bridge section are delivering power to the output is

$$v_{L_o} = V_{in} \left( \frac{n_1}{2} + n_2 \right) - V_o. \quad (A4)$$

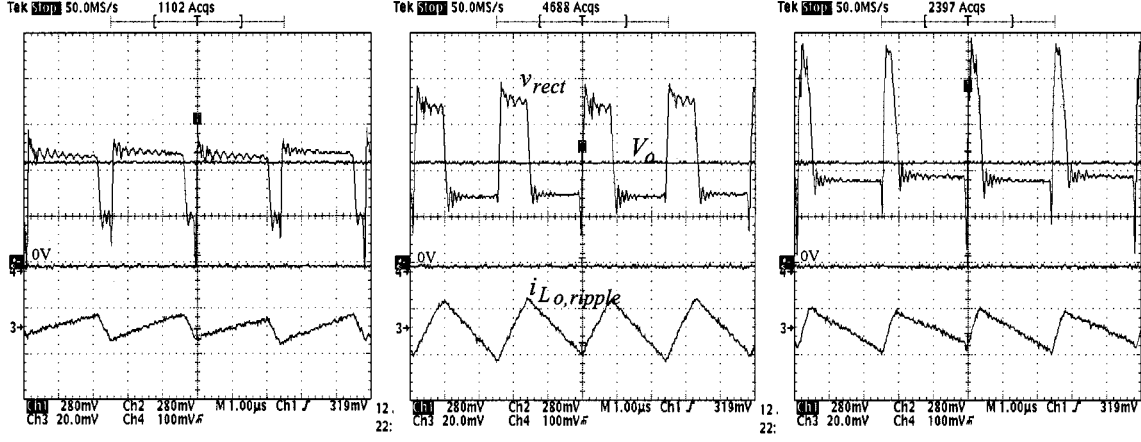


Fig. 13. Voltage and ripple current of output inductor at different input voltages. 5.6 V/div, 0.5 A/div; Hori: 1  $\mu$ s/div.

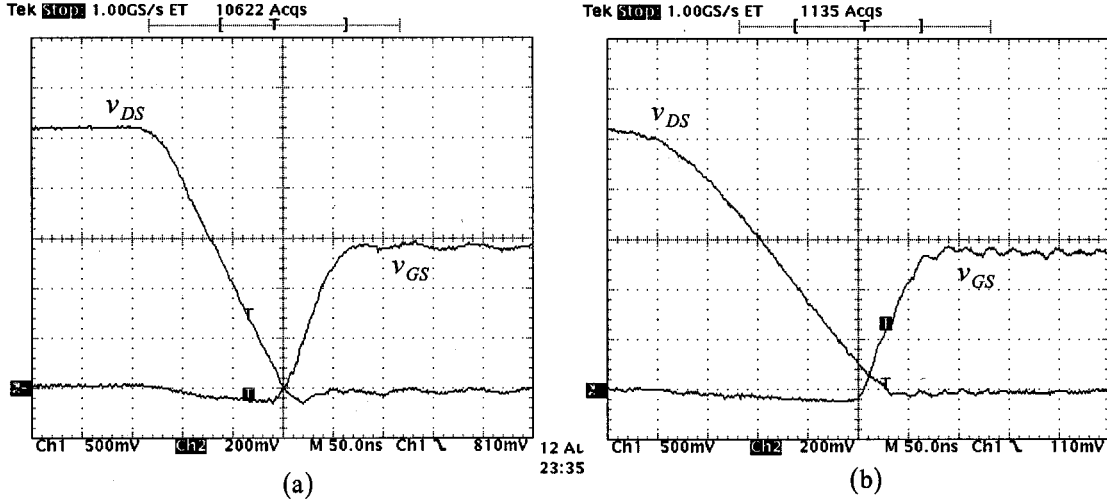


Fig. 14. Gate and drain voltages during turn-on at 3% load: (a) for right-leg switches and (b) for left-leg switches.  $v_{DS}$ : 10 V/div,  $v_{GS}$ : 4 V/div; Hori: 50 ns/div.

Using (A3) and (A4), the peak-to-peak ripple current,  $\Delta I_{pk-pk}$  in the output inductor at any given input voltage is given by

$$\Delta I_{pk-pk} = \frac{\overbrace{\left( V_{in} \left( \frac{n_1}{2} + n_2 \right) - V_o \right)}^{v_{L_o}} \overbrace{\left( \frac{(V_{in, \max} - V_{in})}{V_{in}} \frac{V_{in, \min}}{V_{in, \max} - V_{in, \min}} \right)}^D \frac{T_s}{2}}{L_o} \quad (A5)$$

To find the worst-case input voltage at which  $\Delta I_{pk-pk}$  is maximum, (A-5) is differentiated with respect to  $V_{in}$  and equated to zero

$$\frac{d\Delta I_{pk-pk}}{dV_{in}} = \frac{V_{in, \min}}{V_{in, \max} - V_{in, \min}} \frac{T_s}{2L_o} \left[ \frac{V_o V_{in, \max}}{V_{in}^2} - \left( \frac{n_1}{2} + n_2 \right) \right] \quad (A6)$$

Equating (A6) to zero to find the worst-case input,  $v_{worst}$  and using (A1) and (A2)

$$V_{in, worst}^2 = \frac{V_o V_{in, \max}}{\frac{n_1}{2} + n_2} = \frac{V_o V_{in, \max}}{V_o / V_{in, \min}} = V_{in, \min} V_{in, \max} \quad (A7)$$

$$\therefore V_{in, worst} = \sqrt{V_{in, \min} V_{in, \max}} \quad (A8)$$

## APPENDIX B

### EXPRESSION FOR THE SWITCH VOLTAGE DURING THE RESONANT INTERVAL OF THE LEFT-LEG TRANSITION

The equivalent circuit corresponding to the resonant left-leg transition is given in Fig. 9. Since the two secondary-side leakage inductances are in series and have the same initial current, they can be combined together as  $L_{sec}$ , defined as

$L_{sec} = L_{Lk1}n_1^2 + L_{Lk2}n_2^2$ , where,  $L_{Lk1}$  and  $L_{Lk2}$  are the leakage inductances of the transformers  $T_1$  and  $T_2$  respectively, referred to the primary side. The combined inductance  $L_{sec}$  is in series with  $v_{sec}$  which is the sum of the two secondary voltages

$$v_{sec} = v_{T1} + v_{T2} = n_1 \frac{V_{in}}{2} - v_{C_A^+}(n_1 + n_2). \quad (B1)$$

Since  $C_A^+ = C_A^-$ , the voltage across the capacitor  $C_A^+$  can be expressed as

$$C_{eq} \frac{dv_{C_A^+}}{dt} = i_{C_A^+} = \hat{I}_{mag} + (n_1 + n_2)i_{sec} \quad (B2)$$

where  $C_{eq} = C_A^+ + C_A^- = 2C_A^+$ . The expression for the secondary current,  $i_{sec}$ , using (B-1) can be written as

$$L_{sec} \frac{di_{sec}}{dt} = n_1 \frac{V_{in}}{2} - v_{C_A^+}(n_1 + n_2). \quad (B3)$$

Taking Laplace of (B3) and rearranging

$$i_{sec}(s) = \frac{n_1 V_{in}}{2L_{sec}s^2} - \frac{(n_1 + n_2)}{L_{sec}} \frac{v_{C_A^+}(s)}{s} + \frac{i_{sec}(0)}{s} \quad (B4)$$

where  $i_{sec}(0)$  is the initial secondary current at the start of the resonant interval and is equal to the load current,  $I_o$ . From (B2)

$$i_{sec}(s) = \frac{C_{eq}s v_{C_A^+}}{(n_1 + n_2)} - \frac{C_{eq}v_{C_A^+}(0)}{(n_1 + n_2)} - \frac{\hat{I}_{mag}}{s(n_1 + n_2)}. \quad (B5)$$

Equating (B4) and (B5) and rearranging

$$\begin{aligned} & \left[ \frac{C_{eq}s}{(n_1 + n_2)} + \frac{(n_1 + n_2)}{sL_{sec}} \right] v_{C_A^+}(s) \\ &= \frac{n_1 V_{in}}{2L_{sec}s^2} + \frac{i_{sec}(0) + \hat{I}_{mag}/(n_1 + n_2)}{s} + \frac{C_{eq}v_{C_A^+}(0)}{(n_1 + n_2)} \end{aligned} \quad (B6)$$

$$\boxed{\nu_{C_A^+}(t) = [\hat{I}_{mag} + (n_1 + n_2)I_o] \sqrt{\frac{L_{eq,pri}}{C_{eq}}} \sin(\omega t) + V_{start}} \quad (B7)$$

where

$$\begin{aligned} V_{start} &= v_{C_A^+} = \frac{n_1}{(n_1 + n_2)} \frac{V_{in}}{2} \\ L_{eq,pri} &= \frac{L_{sec}}{(n_1 + n_2)^2} = \frac{L_{Lk1}n_1^2 + L_{Lk2}n_2^2}{(n_1 + n_2)^2} \end{aligned}$$

and

$$\omega = \frac{1}{\sqrt{L_{eq,pri}C_{eq}}}.$$

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