AN ABSTRACT OF THE DISSERTATION OF

Jeong Seok Chae for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on November 22, 2010.

Title: Novel Structures for High-Speed Delta-Sigma Data Converters.

Abstract approved:_____

Gabor C. Temes

As CMOS processes keep scaling down devices, the maximum operating frequencies of CMOS devices increase, and hence circuits can process very wide band signals. Moreover, the small physical dimensions of transistors allow the placing of many more blocks into a single chip, including highly accurate analog blocks and complicated digital blocks, which can process audio to communication data. Nowadays, wideband and low-power data converter is mandatory for mobile applications which need a bridge between analog and digital blocks.

In this dissertation, low-power and wideband techniques are proposed. An embedded-adder quantizer with dynamic preamplifier is proposed to achieve power-efficient operation. Various double-sampling schemes are studied, and novel schemes are presented to achieve wideband operation without noise folding effect. To reduce timing delay and idle tones, a high speed DEM which alternates two sets of comparator references is proposed. Multi-cell architecture is studied to insure higher performance when the number of modulators increases.

0.18 μm double-poly/4-metal CMOS process was used to implement a prototype IC. 20 MHz signal bandwidth was achieved with a 320 MHz sampling clock. The

peak SNDR was 63 dB. The figure-of-merit FoM = $P/(2*BW*2^{ENOB})$ was 0.35 pJ/conversion, with a 16 mW power consumption. Measurement results show that the proposed design ideas are useful for low-power and wideband delta-sigma modulators which have low OSR.

A second-order noise-coupled modulator with an embedded-zero optimization was proposed to reduce power consumption by eliminating some of the integrators. This architecture makes easier the implementation of the small feedback capacitors for high OSR modulators.

Novel Structures for High-Speed Delta-Sigma Data Converters

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APPROVED:

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Director of the School of Electrical Engineering and Computer Science

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Dean of the Graduate School

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Jeong Seok Chae, Author

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CHAPTER 1. INTRODUCTION

1.1. Motivation

Analog-to-digital converters (ADCs) are bridges transferring the information of the analog environment to the digital domain. Their applications have been extended to devices such as bio-medical electronic, consumer, instrumentation, and communication appliances. Especially, ADCs of communication systems have been increased their bandwidth requirement to deliver from the voice to the mobile broadband standard [1]. The bandwidth of the delta-sigma data converter is, also, going up to high speed applications thanks to the higher cut-off frequency which can be achieved as the process shrinks down [2]. For these wideband delta-sigma modulators, we need to adjust the design parameters of the systems such as the over-sampling ratio (OSR), the order of the modulators and the number of quantizer levels to get the optimized point between bandwidth requirement and low power consumption. Normally, this simple adjustment does not bring the minimum power consumption with low OSR ADCs because of low efficiency of noise-shaping. Innovative circuit level design techniques can lower the power consumption and overcome speed limitations with optimized digital components and digital-like analog components [3]. This relaxation can be extended by more effective systems such as low-distortion [4] and/or noise-coupling [5] topology.

In this thesis, novel system and circuit level design techniques are presented to increase the efficiency of delta-sigma data converter. The figure-of-merit (FoM) defined as dissipated power divided by bandwidth and two to the power of effective

number of bits can be a quantitative efficiency of a data converter. Silicon level experimentation shows the effectiveness of the novel techniques.

1.2. Contributions

Four low-power and wide-band techniques are shown in this thesis. They are:

- Embedded-adder quantizer: This is novel technique to reduce the power consumption of the modulators. It merges the adder of the low-distortion modulator and the preamplifier of the quantizer.
- Double-sampling scheme: Previous techniques were proposed in [6] to reduce the noise folding effect and increase the bandwidth. The technique was improved in this research by removing the fundamental cause of the mismatches.
- High speed dynamic element matching (DEM): Previous methods were presented in [7, 8]. However, they are not optimized for the critical delay path. A novel DEM technique [9] is proposed to reduce the delay which is required for modulator stability and the tone which creates by the partitioned DEM.
- Architectural approaches: The last contribution of this research is combining these three techniques in a multi-cell structure and/or noise-coupling scheme to achieve wideband and low-power operation of the modulators which have low OSR.

1.3. Thesis Organization

After this introduction, Chapter 2 proposes low power techniques with a low-distortion architecture and a dynamic embedded-adder quantizer. Chapters 3 and 4

propose wideband techniques with a double-sampled switched capacitor circuit and a fast DEM technique respectively. Chapter 5 describes system level design of the implemented architecture with a discrete-time ΔΣ ADC. Chapter 6 discusses circuit level design issues. Chapter 7 describes test environment, measurement results and comparison results with the implemented IC. Especially, one problem which comes from small sampling capacitors is also shown in this chapter. Chapter 8 describes a high-order noise-coupled ADC which is applicable to the proposed embedded-adder quantizer. Chapter 9 summarizes the contributions of this research and concludes the dissertation.

CHAPTER 2. LOW POWER DESIGN TECHNIQUES

In this chapter, power budgets of discrete-time ΔΣ ADCs are summarized. From this summary, low-distortion architecture is selected as low-power modulator to reduce the power consumption of opamps. One disadvantage of this architecture is analyzed. An embedded-adder quantizer minimizing power consumption is proposed in this chapter.

2.1. Low-Distortion Architecture

To compare the power of modulator building blocks, power budgets of four discrete-time ΔΣ ADCs are summarized in Table 2.1. Each modulator is divided into three blocks which are integrators, quantizer, and clock-plus-digital block. Integrators are the most power-hungry block and dissipate more than 72 percent of total modulator power. The power of quantizer and clock-plus-digital circuit increases as signal-to-noise-plus-distortion ratio (SNDR) increases. However it is smaller than the power of integrators as shown in Table 2.1 and hence we are going to focus on integrator design to minimize power consumption.

Table 2.1: Summary of power budgets of discrete-time ΔΣ ADCs

	Power [%]			SNDR [dB]	Clock Frequency [MHz]
	Integrators	Quantizer	Clock+Digital		
Bos[10]	71.8	9.9	18.3	65	320
Lee[11]	72.2	5.6	22.2	76	132
Balmelli[12]	78.8	10.0	11.2	72	200
Reutemann[13]	76.9	6.0	17.1	79	80

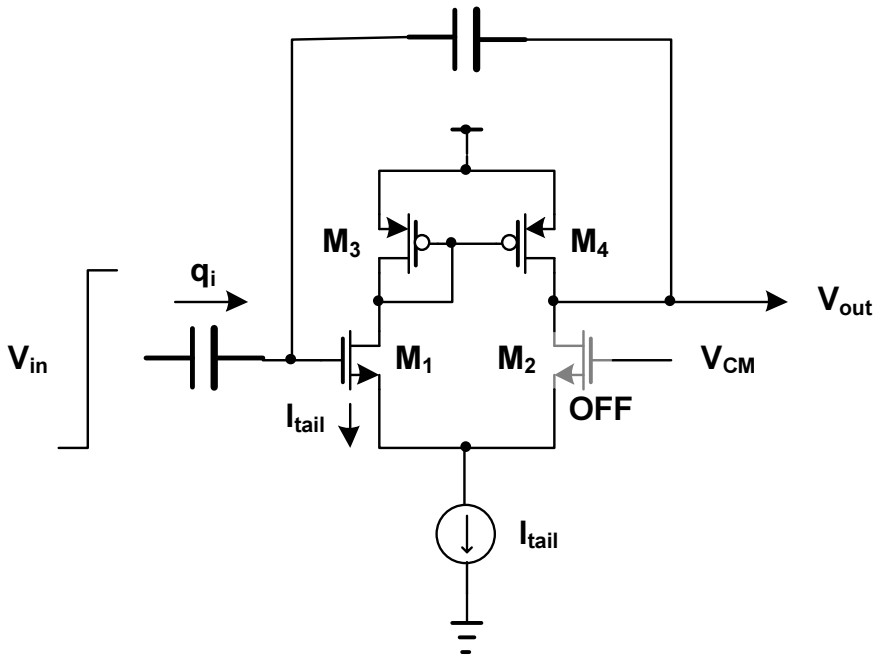


Figure 2.1: Slewing condition of a simple opamp.

The power dissipation of opamps is decided by two constraints, slew rate and settling time. Following the rule of thumb described in [14], we can allocate 25% of a half-clock-period for slewing. Remaining 75% of a half-clock-period can be used for settling time of opamp. These two constraints give us two current numbers and higher number is selected to guarantee final value of opamp outputs. Previous works [15-18] devoted their effort to change the static bias current required for slewing to dynamic current to minimize the bias current of opamp. They use class-AB amplifiers [15], inverters [16, 17], and dynamic-biasing techniques [18]. However, all of them require additional circuit complexity. If we get rid of the main reason of slewing with the architectural design of modulators, power consumption can be minimized without additional efforts.

Slewing condition can be explained by the input charge of the circuit shown in Figure 2.1. If the input charge(q_i) which increases the current of input transistor(M_1) is too big and the maximum current(I_{tail}) of input transistor(M_1) is smaller than

designed, linear relationship between input and output of opamp can not be satisfied because input transistor(M_2) enters cut-off mode [19]. However, if the input charge is small and tail current can be shared by both transistors, M_1 and M_2, all transistors are in saturation-mode which keeps the linear characteristic of opamp and prevents slewing condition.

The low-distortion architecture [4] was proposed to achieve good linearity of ADCs by using the feedforward paths. A third-order modulator which has low-distortion architecture is depicted in Figure 2.2. Since signal does not go through the integrators of the modulator, nonlinearity of opamps can not be shown up at the output of the modulator, V. In addition to this advantage, it gives us power saving. As depicted in Figure 2.2, the outputs of integrators only process shaped noises without signal. Hence, the incoming charge of integrators can be reduced by increasing the number of the quantizer levels, i.e. decreasing quantization noise, E. For certain levels of qunatizer, we do not need to consider the slew rate of opamps. Only settling time will decide the power consumption of opamps. However, one bad thing of this architecture is that the power saving is limited by the adder which has large incoming charge which introduces slewing condition, and low feedback factor, β, which comes from input branches of the adder.

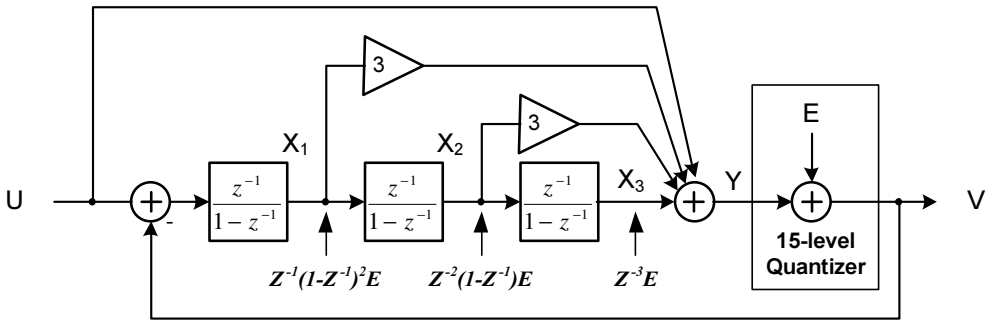


Figure 2.2: A third-order modulator with 15-level quantizer.

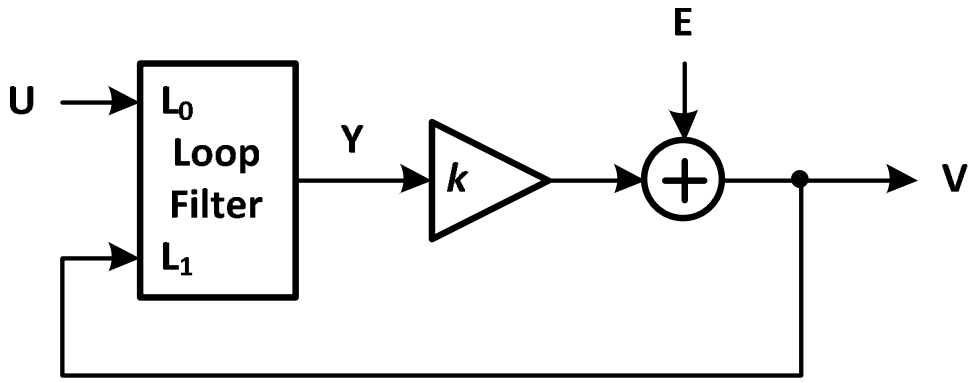


Figure 2.3: An equivalent model of Figure 2.2 when settling error is modeled as the gain block of *k*.

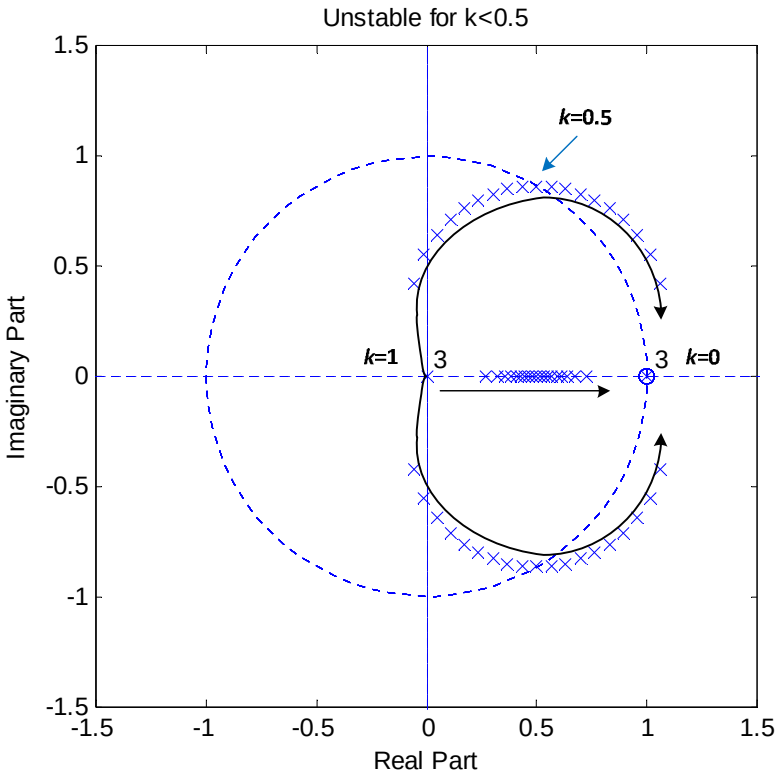


Figure 2.4: Root-locus of poles and zeros by decreasing *k* from 1 to 0.

2.2. Stability

In addition to slewing, the stability of the adder limits settling time requirement. Before moving onto this topic, let us examine general thought about noises added at the output of the adder. If we calculate noise-transfer function (NTF) from the adder output to the output of the modulator shown in Figure 2.2, it can be described as

$$NTF = (1 - Z^{-1})^3 \tag{2.1}.$$

Since this NTF is same as NTF of the modulator, any noise coming into the output of the adder can be shaped with the order of modulators and hence the settling error of the adder can be shaped by NTF to relax settling requirement. However, this statement is not true with the stability condition. For simplicity, let us assume that the adder as a block only has linear settling error. It can be modeled as a gain block shown in Figure 2.3. As we relax settling requirement, the coefficient of gain block, *k*, decreases and poles of modulator moves to the output side of the unit circle. Z-plane root-locus of poles and zeros are depicted in Figure 2.4 by decreasing *k*. When *k* becomes smaller than 0.5, the modulator becomes unstable. To get time domain information, MATLAB simulation was done with the modulator of Figure 2.2 and various *k* values of Figure 2.3. OSR is set to eight. When *k* became smaller than 0.8, SNDR starts to decrease (Figure 2.5). Finally, system becomes unstable when *k* equals 0.5. This result matches well with root-locus. Hence, to ensure the performance of modulator, the bandwidth of the adder should satisfy this settling requirement. This looks like easy to achieve, but it is hard when the modulator has higher order than the second and needs low power adder.

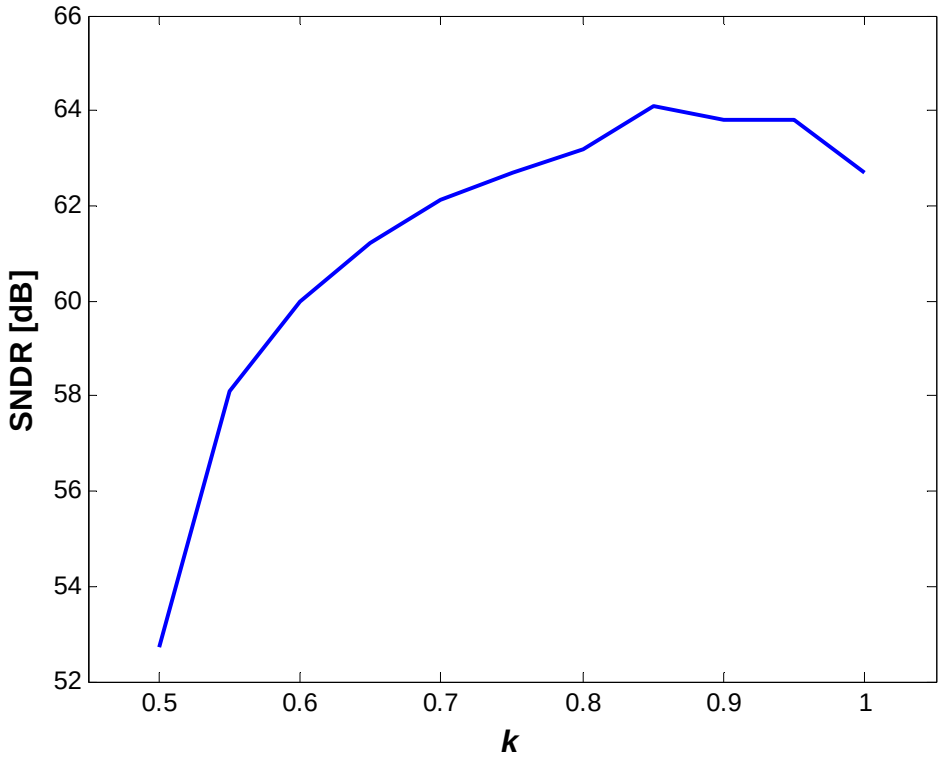


Figure 2.5: Peak SNDR with various values of *k*.

2.3. Adder Bandwidth Requirement

Wideband low-distortion modulators which have higher order than second have many feedforward branches and large coefficient values to build a signal-transfer function (STF) which has flat gain of 1 over the whole frequency range. However, these input branches bring low feedback factor, β, to the adder. We need wideband opamps to manage this small value which decreases the bandwidth of opamp with the sampling capacitors of the multi-bit quantizer. Different types of adders [5][20-21] were proposed to relax this high bandwidth requirement. They still have problems such as requiring wideband adder, increasing the current of first stage opamp, and reducing the stability of the modulator. Here, we have found a power-efficient dynamic adder which does not have feedback configuration.

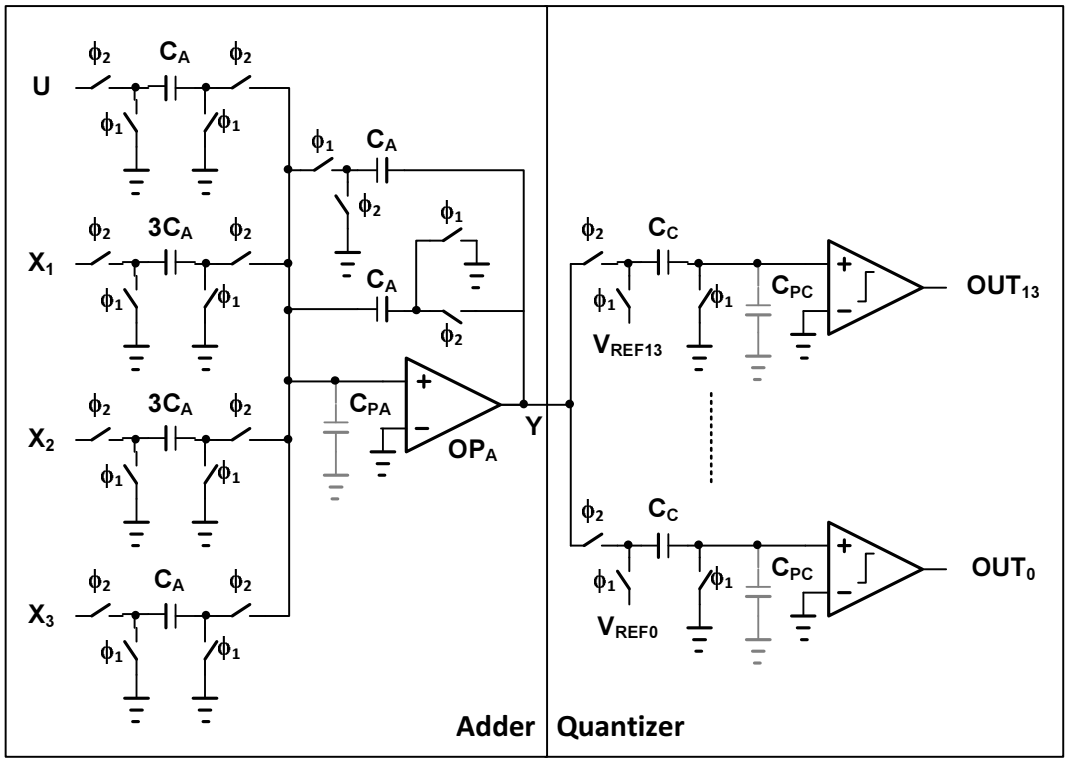


Figure 2.6: A switched-capacitor-based adder with a 15-level quantizer

For single-bit modulators, passive adders are good enough because modulator only requires the sign of the adder output. However, multi-bit modulators require active adders to keep the gains of the adders and relax the design requirements of the quantizers. As shown in Figure 2.6, the feedback factor of the active adder is 1/9 without considering parasitic input capacitor(C_{PA}) of the opamp(OP_A) which is not small for wideband opamps. It is getting worse by increasing the order of modulator.

To calculate bandwidth requirement of OP_A, we can assume the clock phase when ϕ_2 is "HIGH". From [14], close-loop bandwidth can be denoted as

$$\omega_{ADD} = \frac{\beta g_{ma}}{C_{LA}} \tag{2.2}$$

when g_{ma} is the transconductance of the input transistor of OP_A, β is the feedback factor of the adder, and the load capacitor, C_{LA}, is same as Equation 2.3.

$$C_{LA} = C_A + 14\frac{C_C \cdot C_{PC}}{C_C + C_{PC}} + \frac{8C_A \cdot C_A}{8C_A + C_A} \tag{2.3}$$

If $C_C >> C_{PC}$, Equation 2.3 becomes

$$C_{LA} = C_A + 14C_{PC} + \frac{8C_A}{9}. \tag{2.4}$$

By substituting Equation 2.4 into Equation 2.2, bandwidth can be calculated as

$$\omega_{ADD} = \frac{g_{ma}}{(17C_A + 126C_{PC})}. \tag{2.5}$$

Bandwidth of the first integrator shown in Figure 2.7 can be calculated by using the same way and denoted in Equation 2.6 when sampling capacitance of the second stage is one quarter of the first stage's.

$$\omega_{1st} = \frac{g_{m1}}{(3/2)C_1} \tag{2.6}$$

C_1 is capacitance of first-stage sampling network and g_{m1} is the transconductance of first-stage opamp. To compare Equation 2.5 and 2.6, we need to make some assumptions. They are: C_1 is ten times bigger than C_A, C_A is four times bigger than C_{PC}, and ω_{1st} is 7/2 times higher than ω_{ADD}. Ratio between C_1 and C_A is decided by the thermal noise limit of ADCs and the minimum capacitance of a fabrication process. Ten is chosen for a 12bit ADC and 0.18μm 4-metal double-poly CMOS process. From the process limitation, the ratio between C_A and C_{PC} is set. Comparison result can be shown by the settling time of the first stage opamp and the stability of the adder examined in chapter 2.2. By using Equation 2.5, Equation 2.6, and three assumptions, g_{ma} and g_{m1} can be described by common variables. They are

$$g_{ma} = \frac{2\omega_{1st}}{7}(1.7C_1 + 3.15C_1) \approx 1.4\omega_{1st}C_1 \tag{2.7}$$

$$g_{m1} = 1.5\omega_{1st}C_1. \tag{2.8}$$

Even though Equations 2.7 and 2.8 vary with the process technologies and the expected performances of ADC, the power of the adder is not negligible compared with the most-power-hungry analog block, first integrator, because current is proportional to the transconductance of transistors with a fixed over-drive voltage.

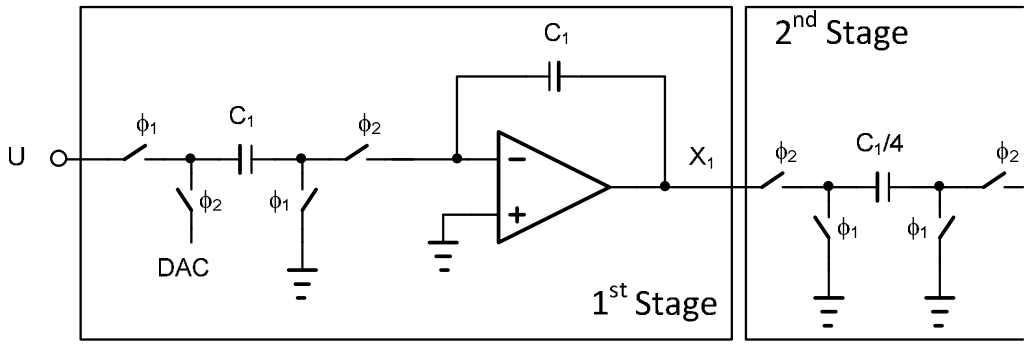


Figure 2.7: First-stage integrator with a second-stage sampling network.

2.4. Embedded-Adder Quantizer

From the analysis of previous chapter, the power consumption of adder is increased by the low feedback factor of opamp. This problem can be remedied by the proposed feedback-free adder. Figure 2.8 shows the proposed embedded-adder quantizer, which merges the framed parts of Figure 2.9, i.e., the adder, the preamplifiers, and the gain blocks. Transistors M_{I1} to M_{I10} are differential input pairs, used to process the reference voltages, input signals, and the outputs of integrators. Resistors are connected to their sources to achieve constant G_ms even with large swing of inputs and common mode variations. Gains of input branches can be set by the size ratio of transistors and resistors. The inputs connected to reference voltages have a gain of 2 to improve the nonlinearity when the reference voltages are too low. The inputs connected to modulator input and integrator outputs have gains decided by feedforward branches. To reduce the kickback noise which goes to sampling capacitors and opamps, cascode stages ($M_{C1} – M_{C10}$) are added.

The operation of the proposed adder can be explained as follows. When ϕ_C is *"LOW"*(Figure 2.10), nodes *OUTP* and *OUTN* are precharged to *VDDC*, the power supply voltage of the quantizer through the transistors, M_{PD1} and M_{PD2}. After ϕ_C goes *"HIGH"* and M_{ND1} turns on (Figure 2.11), all inputs are added together in current which is proportional to gate voltages and gains. The evaluation starts to detect speed

difference of discharging output nodes. With dynamic operation, the transconductances of M_{I1} - M_{I10} can be designed large enough to keep constant G_ms with source degeneration resistors, without static power consumption, because the currents of the input transistors only discharge the parasitic capacitors of *OUTP* and *OUTN*. This dynamic operation [22] promises high speed, by eliminating the static bias currents that slow down the discharging speed of the outputs. 14 preamplifiers are required to build a 15-level quantizer. The comparator samples data without switched capacitor samplers, and hence it brings additional digital power saving. A following regenerative latch samples the voltage differences between two outputs of preamplifiers during the transition.

Power comparison between the earlier quantizer [5] and the proposed one is summarized in Table 2. For fair comparison, same process and extrapolated frequency are used. The proposed scheme has lower power without independent adder and input sampling networks. Hence, large power saving can be achieved with the proposed scheme.

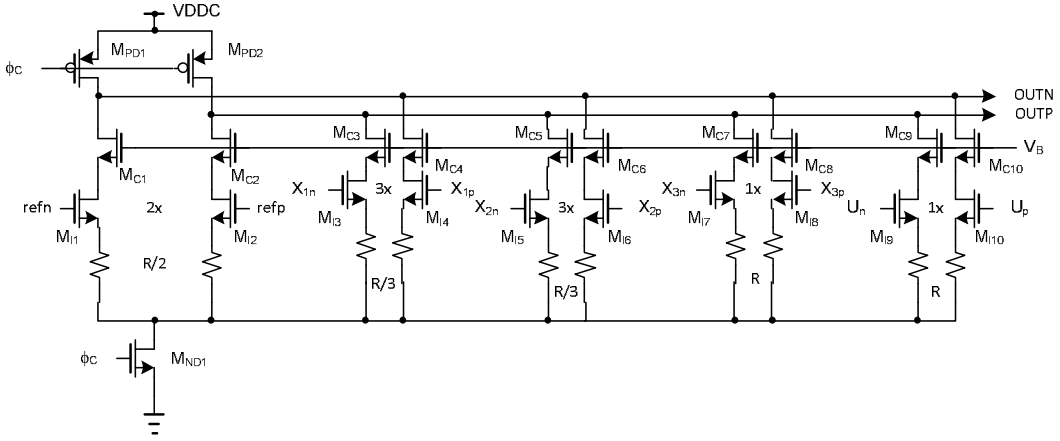


Figure 2.8: A proposed power-efficient embedded-adder quantizer.

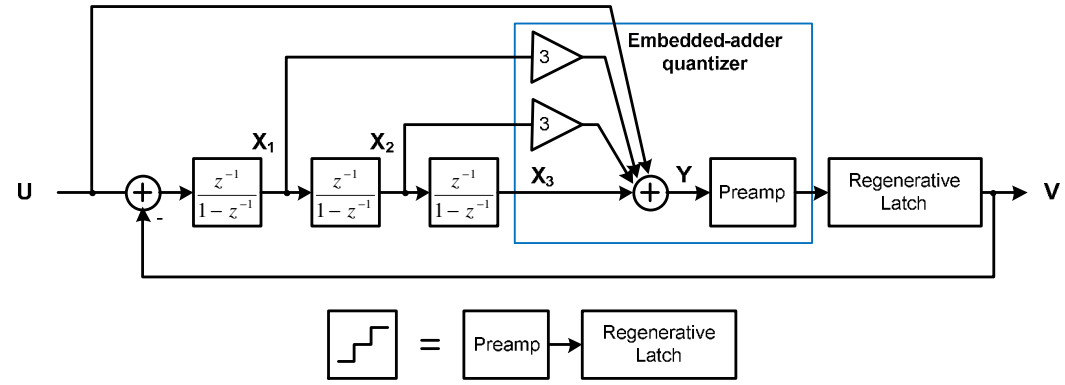


Figure 2.9: A third-order modulator with framed part of embedded-adder quantizer

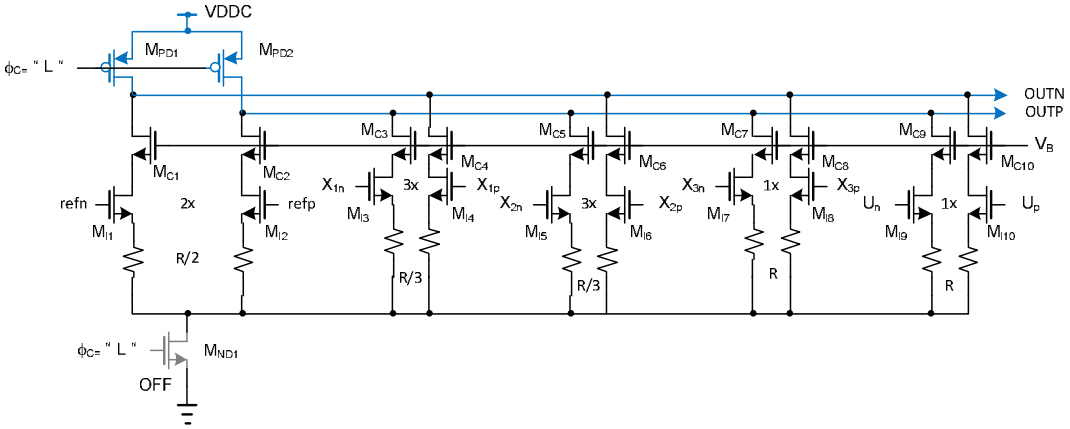


Figure 2.10: Precharging when ϕ_C is “LOW”

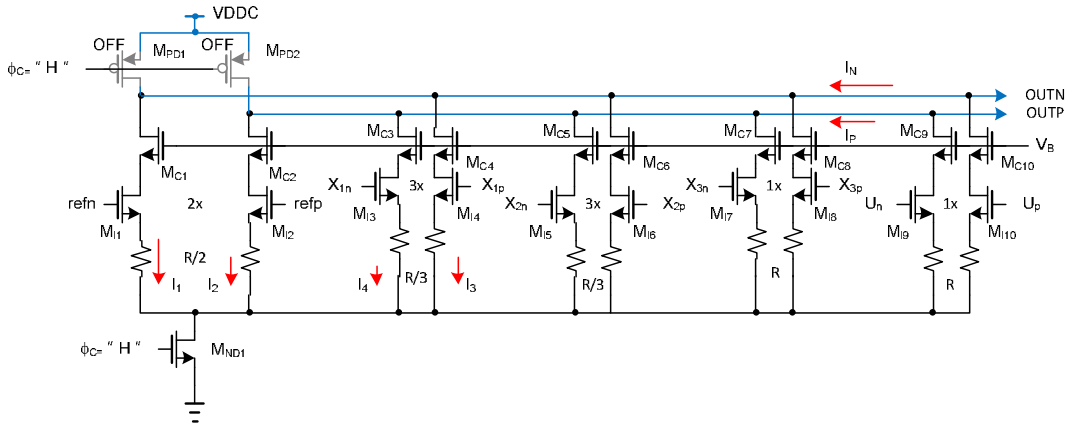


Figure 2.11: Evaluation when ϕ_C is “HIGH”

Table 2.2: Quantizer power comparison

	Sampling frequency [MHz]	Power [mW]
[5] (measured)	200	3.56
[5] (extrapolated)	320	5.70
Proposed (measured)	320	4.39

CHAPTER 3. WIDEBAND DESIGN TECHNIQUE 1

Various double-sampled (DS) integrators are studied and the main problem called noise folding effect, is analyzed. A novel DS integrator is proposed to eliminate the fundamental cause of folding. Bandwidth of an example modulator is doubled by using the proposed integrator without increasing in-band noise floor.

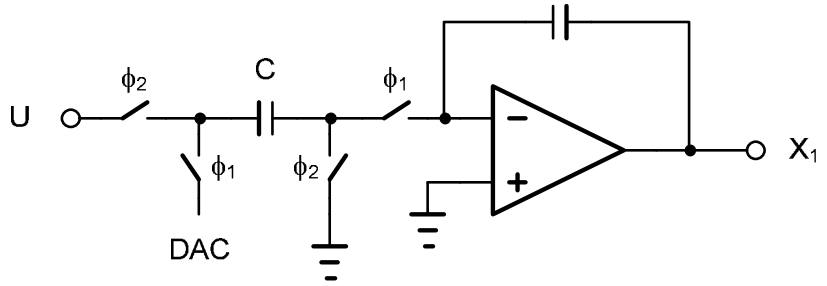
3.1. Introduction

As the bandwidths of ΔΣ ADCs increase up to telecommunication specifications, many papers focus on continuous-time (CT) ΔΣ ADCs, but the inherent characteristics of CT ΔΣ ADCs make this kind of data converter only suitable for low resolution applications. Recently, high resolution and high bandwidth discrete-time (DT) ΔΣ ADCs were introduced. They, however, do not have high bandwidths compared with CT ΔΣ ADCs because of the sampled operation of DT integrators. For DT ΔΣ ADCs, the bandwidth can be increased two times by using time-interleaved architectures and DS architectures. Time-interleaved architectures have problems such as domino effect [24], image signal around $f_s/2$ [11], and additional zeros [25]. They make time-interleaved architectures unattractive for ΔΣ ADCs.

For switched-capacitor (SC) filters, a DS integrator which does not have these kinds of problems was proposed by Choi [26] using two time-interleaved sampling capacitors. A problem of DS integrator analyzed by Hurst [27] is noise folding which comes from mismatches of two sets of DACs. He proposed a randomization technique for the gain mismatch minimization but it is only effective for low over-sampling ratio (OSR) cases. Ribner [28] used a four-phase clocking to eliminate this problem. His architecture, however, does not take the advantage of double sampling integrators which doubles the bandwidth by using the idle time of actual two-phase

clocking integrator. Yang [29] showed a way to apply $(1+z^{-1})$ term to the feedback loop for moving the mismatch factor in front of the first integrator output. This method reduces the noise folding effect by first-order shaping characteristics of second-order DS modulator from the single-ended analysis. Burmas [30] proposed an additive-error switching method to modulate out the DAC mismatch to $f_s/2$, but it needs additional capacitors to prevent signal dependent offset integration which introduces second harmonic and noise folding. Thanh [31] presented individual-level averaging (ILA) for the mismatch shaping with a little SNDR degradation. Senderowicz [32] proposed a bilinear integrator which cancels mismatches differentially. A problem of this DS integrator is the reduced stability of modulators due to the additional pole introduced by adding the bilinear term. Vleugels [7] simplified the modulator architecture by using delays for feedforward paths but her modulator still has same stability problem. Yang, Nagari [33], Rombouts[34], and Kim[35] replaced one of the $(1+z^{-1})$ terms in feedback paths by z^{-1} for high order modulators to stabilize their modulators. This method needs small modulator coefficients which increase the total modulator area. A method showed in [25], [36] is putting zeros at $f_s/2$. These additional zeros change the power spectral density (PSD) at $f_s/2$. They reduce noise folding and signal-to-quantization-noise ratio (SQNR). Recently, Koh proposed an ingenious double-sampling integrator [37]. Its transfer function is equal to "1" and there is no mismatch integration. However, as shown in [30], signal dependent offset integration reduces the performance of the modulator. Lee [38] proposed a novel scheme which has $(1+\delta z^{-1})$ term. δ only depends on mismatches between DAC capacitors and hence has a very small value which does not affect the SNDR and stability. Finally, a novel double-sampling integrator which uses only one sampling network is proposed.

The remainder of this chapter is divided into five main sections. Section 2 shows various kinds of DS integrators. Section 3 presents the problems of conventional DS integrators. Section 4 explains the scheme of [38]. Section 5 describes the proposed double-sampling integrator. Summary follows in Section 6.



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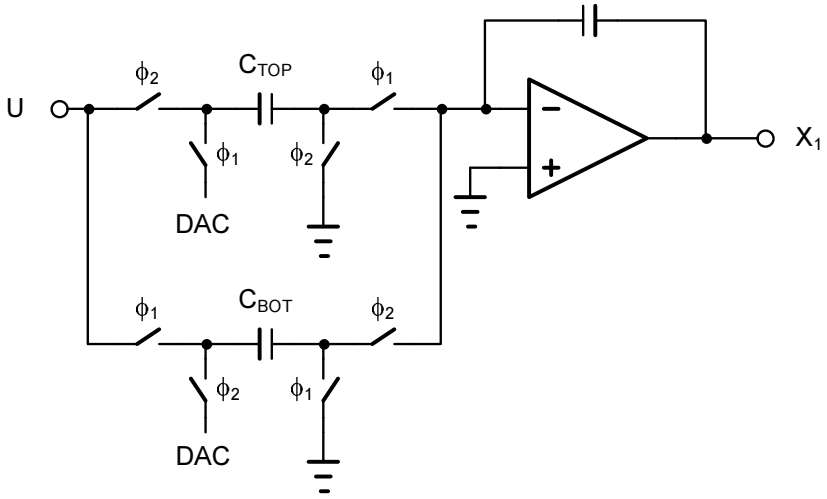

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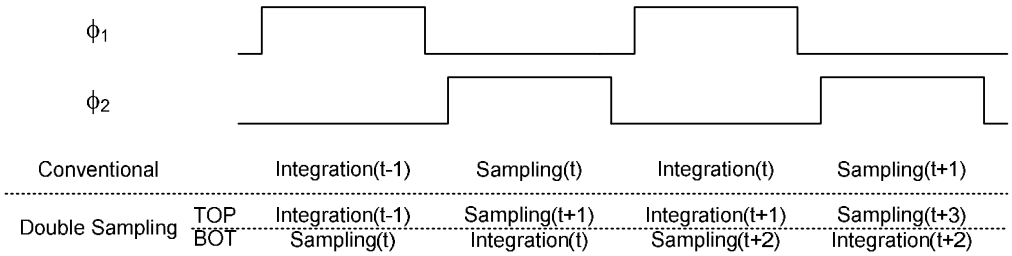


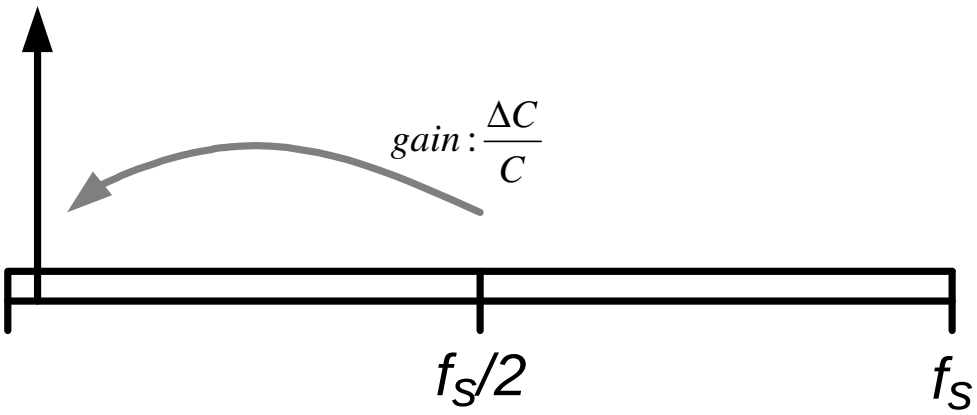
(c)

Figure 3.1: Sampling schemes with (a) a single-sampling integrator, (b) a double-sampled integrator and (c) the timing diagrams.

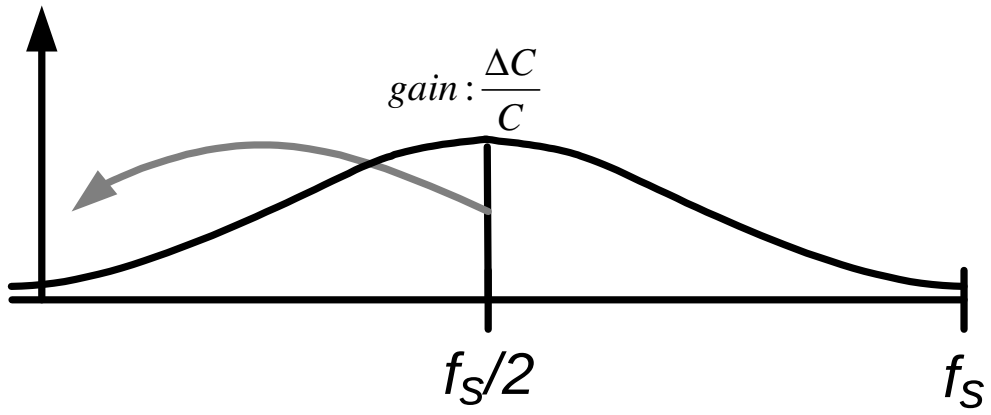
3.2. Double-Sampled Integrators

For the conventional integrator of Figure 3.1(a), we need two phases to accumulate the sampled data into the integrator. DS integrators (Figure 3.1(b)) are used to double the modulator bandwidth by sharing the phases of sampling and integration as shown in Figure 3.1(c). It has twice wider bandwidth than the single-sampled integrators without major power increase.

Noise folding is a well-known problem of the DS ΔΣ ADCs which brings the shaped quantization noise power around half of the sampling frequency back to the signal band. This folded noise increases the total noise of the modulator. The inputs of ΔΣ ADCs usually are filtered by anti-aliasing filters. Hence, even though there is modulation with capacitor mismatch, noise folding effect is negligible as shown in Figure 3.2(a). Here, we will only deal with the DAC feedback paths of integrators which have high quantization noise power around $f_s/2$ as illustrated in Figure 3.2(b). C is the average of the two sampling capacitors and ΔC is the difference between them.



(a)



(b)

Figure 3.2: Noise folding for (a) the input signal path and (b) the DAC feedback path.

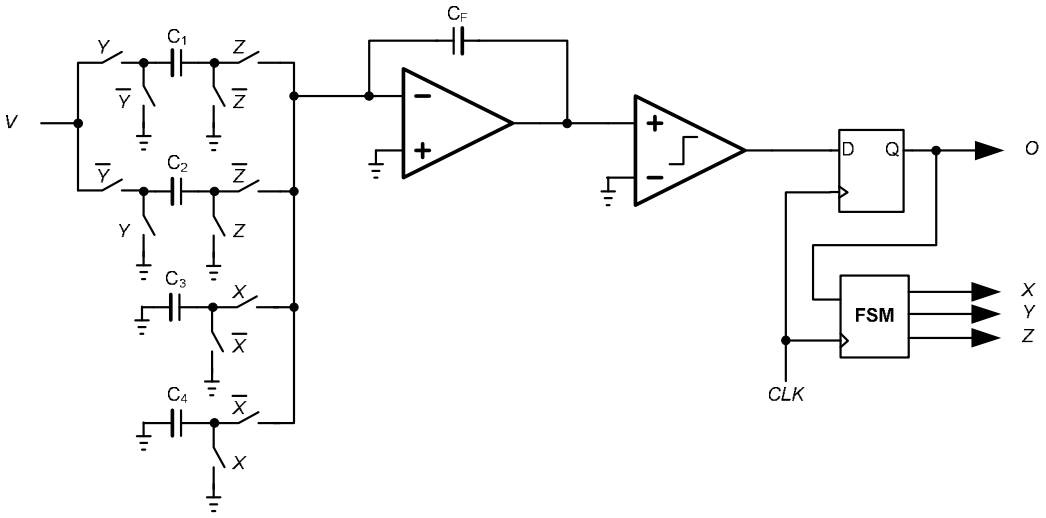


Figure 3.3: A first-order ΔΣ modulator using additive-error switching SC integrator (omitting input sampling capacitors).

3.2.1. Additive-Error Switching [30]

The additive-error switching proposed by Burmas et al. (Figure 3.3) remedies noise folding using state-machine-controlled integrator. The switching algorithm is:

1) When the output O of the ΔΣ modulator changes, the same capacitor used for previous operation transfers charge into the integration capacitor, C_F, to toggle the polarity of mismatch by toggling Y and holding Z.

2) When the previous and present data are the same, mismatch of opposite sign can be added for every clock phase by toggling Y and Z.

Assume the common-mode reference capacitance is

$$C = \frac{C_1 + C_2}{2} \tag{3.1}$$

and the differential reference capacitance is

$$\Delta C = C_1 - C_2 \tag{3.2}$$

With the algorithm and equations of [30], the charge moved to the C_F is

$$Q_F = CVO[n] + \frac{\Delta C}{2} V(-1)^n \tag{3.3}$$

where time $n = 0$ corresponds to a period during C_1 was selected and switched from zero to V which is always constant. The first term is the expected integration value, and the second term (caused by gain mismatch of integrator) is modulated to $f_s/2$. In Figure 3.3, $\overline{X}$, $\overline{Y}$, and $\overline{Z}$ are nonoverlapping complementary signals of X, Y, and Z, respectively. The FSM is controlled by the following equations:

$$X[n] = X[n-1] \oplus O[n] \oplus O[n-1] \tag{3.4}$$

$$Y[n] = Z[n] \oplus O[n] \tag{3.5}$$

$$Z[n] = \overline{Z[n-1] \oplus O[n] \oplus O[n-1]}. \tag{3.6}$$

The reason for X and $\overline{X}$ of Figure 3.3 is offset cancellation, if we assume all capacitors are equal to C. This will be discussed in the Section 3.3. Disadvantages of this scheme are doubled loading capacitance due to two capacitors working together for offset cancellation and large area for four capacitors.

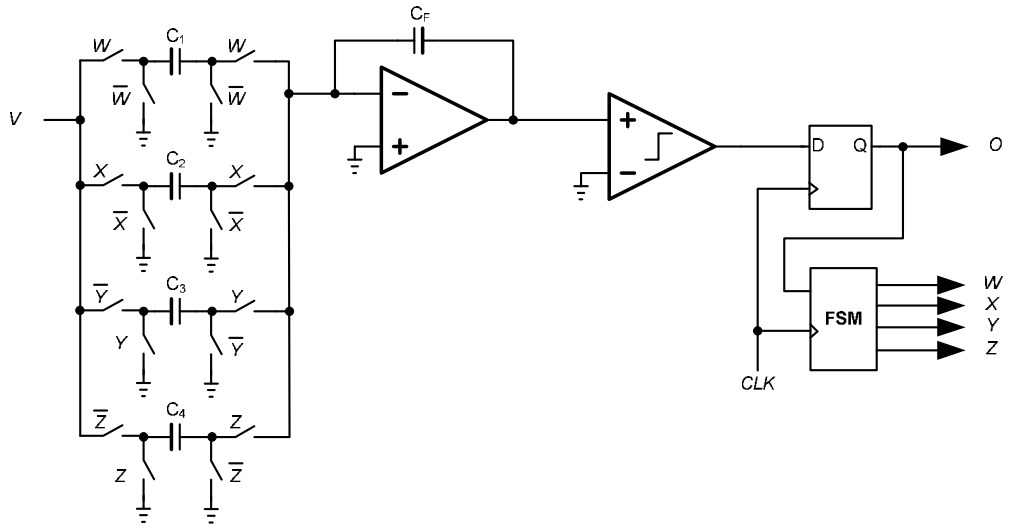
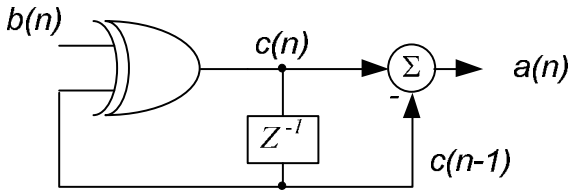


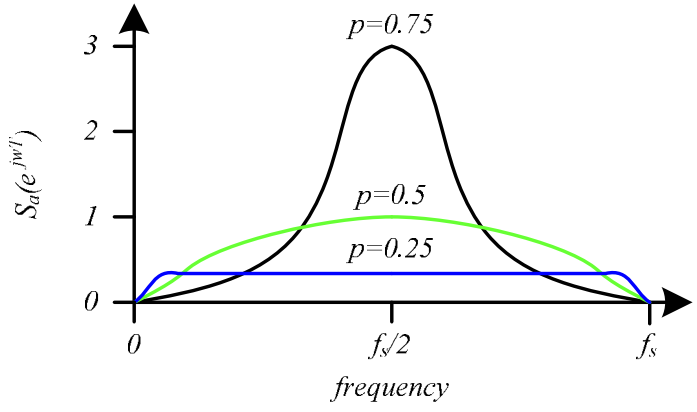
Figure 3.4: A first-order ΔΣ modulator using individual-level averaging SC integrator (omitting input sampling capacitors).



(a)

b(n)	c(n-1)	c(n)	a(n)
0	0	0	0
0	1	1	0
1	0	1	1
1	1	0	-1

(b)



(c)

Figure 3.5: Alternate mark inversion [31]: (a) coder, (b) truth table, and (c) power spectral density.

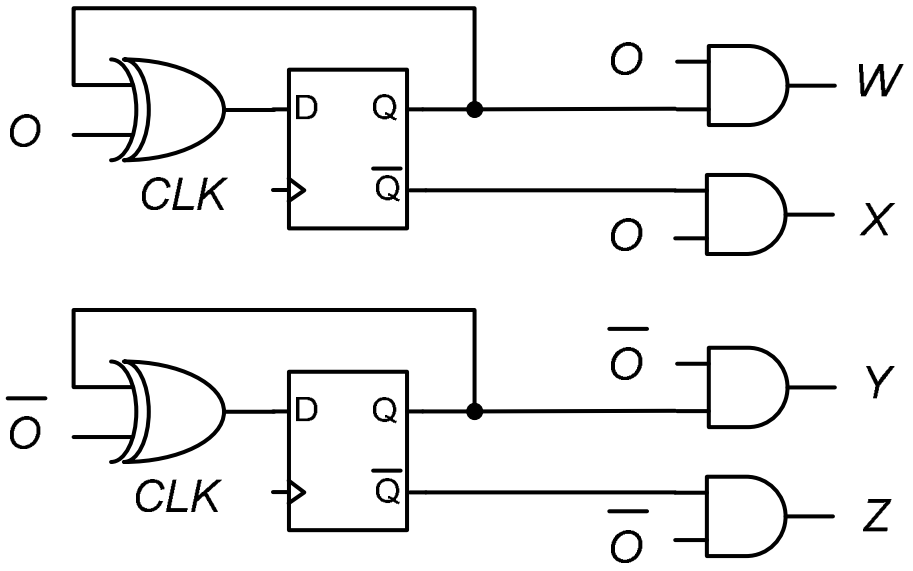


Figure 3.6: A finite state machine for Figure 3.5.

3.2.2. Individual-Level Averageing (ILA) [31]

To reduce the loading capacitor of [30], Thanh et al. proposed a method which shapes the mismatch using four capacitors and alternate mark inversion (AMI). Figure 3.4 presents the integrator with ILA controlled by AMI encoders. $\overline{W}$, $\overline{X}$, $\overline{Y}$, and $\overline{Z}$ are nonoverlapping complementary signals of *W*, *X*, *Y*, and *Z,* respectively. Figure 3.5(a) is an AMI encoder which has truth table as shown in Figure 3.5(b) and PSD of *a(n)* in Figure 3.5(c). If *b(n)=0*, *a(n)* is encoded only to zero but if *b(n)=1*, *a(n)* can be ±*1*. For the same value of input *b(n)*, the noise PSD due to DAC mismatch can be pushed out to around $f_s/2$ followed by ILA algorithm, i.e. by randomization of alternated two capacitors. Figure 3.5(c) represents PSD of *a(n)*, and p is the probability of *b(n)=1*. Using two blocks of Figure 3.5(a) and one inverter, we can modulate the mismatch out for the both levels of *b(n)*. Figure 3.6 is a finite state machine proposed by Thanh et al.. $\overline{O}$ is complementary signals of modulator output *O*. Four capacitors are still required to make mismatch shape out around $f_s/2$.

3.2.3. Bilinear $(1+z^{-1})$ Integrator [29]

Yang presented a way which moves the mismatch factor from the input of integrator to the output of integrator to make mismatch shape out from baseband by using inherent noise shaping of ΔΣ modulator. It is shown in Figure 3.7 if we assume C and ΔC are the same as in Equation 3.1 and 3.2. Figure 3.7(a) is an inverting integrator without delay. The output is

$$V_{OUT} = -\frac{1}{1-z^{-1}}\frac{C}{C_F}V + \frac{\Delta V}{1-z^{-1}}\frac{\Delta C}{C_F} \tag{3.7}$$

where $\Delta V = V_1 z^{-1} - V_2$ and ϕ_2 is advanced phase. From Equation 3.7, ΔC is still affecting the input of the integrator because of the integrator transfer function of mismatch term. Bilinear integrator can be implemented by changing two ground connections of Figure 3.7(a) to $-V_1$ and $-V_2$. The output of Figure 3.7(b) can obtained as

$$V_{OUT} = -\frac{1+z^{-1}}{1-z^{-1}}\frac{C}{C_F}V + \frac{1-z^{-1}}{1-z^{-1}}\frac{\Delta C}{C_F}\Delta V \tag{3.8}$$

$$= -\frac{1+z^{-1}}{1-z^{-1}}\frac{C}{C_F}V + \Delta V\frac{\Delta C}{C_F}. \tag{3.9}$$

The first term is bilinear integrator output and the second term is mismatch term which has ΔC moved from the input to the output of the integrator. This method was generalized for high-order and various types of ΔΣ modulators by Rombouts et al. [34]. This method uses two capacitors to implement the feedback DACs.

3.2.4. Fully-Floating Bilinear Integrator [32]

Senderowicz et al. proposed a differential bilinear integrator which for each input of opamp, only one capacitor is required to cancel DAC mismatches. The operation of the integrator shown in Figure 3.8 can be explained by analyzing the charge of two input capacitors. It is given by

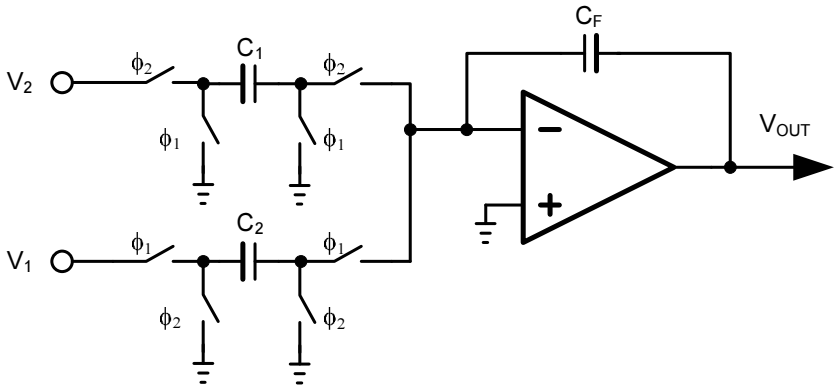
$$Q^{+} = -V(1+z^{-1})(C - \Delta C/2) \tag{3.10}$$

$$Q^{-} = V(1+z^{-1})(C+\Delta C/2) \tag{3.11}$$

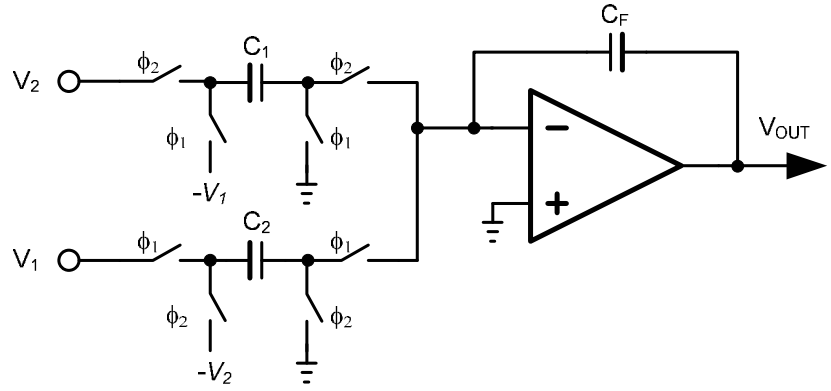
if we assume $C_1 = C - \Delta C/2$ and $C_2 = C + \Delta C/2$. Both capacitors work at the same time, so the differential charge is

$$Q^{-} - Q^{+} = 2V(1+z^{-1})C. \tag{3.12}$$

In Equation 3.12, there is no capacitor mismatch term which is shown in Equation 3.10 and 3.11, so this integrator is not affected by the gain mismatch of the DAC. Modulation occurs only in the common-mode (CM) input signal component, which is rejected by the differential structure. This integrator, however, has a problem which is a loss in the signal-to-quantization-noise ratio (SQNR) because of the extra factor, $(1+z^{-1})$. This will be analyzed in Section 3.3.



(a)



(b)

Figure 3.7: A double-sampling SC integrator: (a) delay-free and (b) bilinear [29].

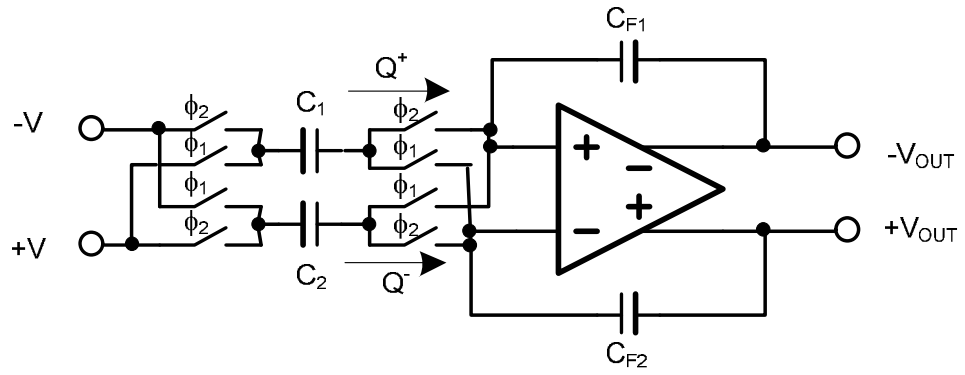


Figure 3.8 : Senderowicz's fully-floating differential SC integrator.

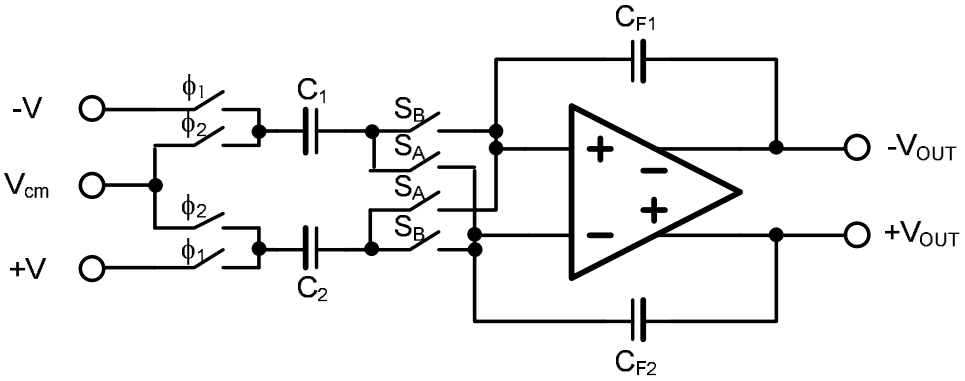


Figure 3.9: Koh's floating differential SC integrator with switches for SC DAC.

3.2.5. Koh's Integrator [37]

Koh et al. proposed an integrator which reuses charge sampled into input capacitors because reference voltage has same magnitude all the time, even for a multi-bit DACs. As we can see in Figure 3.9, the voltage-to-charge transfer function of the integrator is 1 and only one capacitor can perform the two-phase integration for each input of opamp if we assume all capacitors are same to *C*. S_A and S_B are controlled by ΔΣ modulator output to subtract feedback values. They are complementary signals to change the charge polarity injected into integration capacitors. SNDR and stability are not degraded but this integrator has a problem called signal dependent offset sampling and discussed by Burmas [30]. The problem will be discussed in the next section.

3.3. Problems with Double-Sampled Integrators

3.3.1. Signal Dependent Offset Integration

If the switches connected to virtual ground nodes change data-dependently, the value stored by offset integration is not constant [30]. Analysis of signal dependent offset integration will be shown with Koh's integrator [37].

The starting conditions of analysis are S_B closed and $\phi_1=1$ where ϕ_1 and ϕ_2 are differential nonoverlapping clocks and S_A and S_B are complementary value (Figure 3.10(a)). The stored charges of C_1 and C_2 are equal to

$$Q_1 = -C(V+\Delta/2) \tag{3.13}$$

$$Q_2 = C(V+\Delta/2), \tag{3.14}$$

respectively, if we assume $C_1 = C_2 = C$ and Δ is the offset voltage of opamp. When the clock phases change from ϕ_1 to ϕ_2 and the DAC data change, i.e. the unchanged switches connected S_A and S_B (Figure 3.10(b)), ϕ_1 and ϕ_2, toggle the polarity of charge, both capacitors are discharged, so the charges integrated into the C_{F1} and C_{F2} are

$$Q_{F1} = -(C(-V-\Delta/2)-C(V_{cm}-\Delta/2)) = C(V+V_{cm}) \tag{3.15}$$

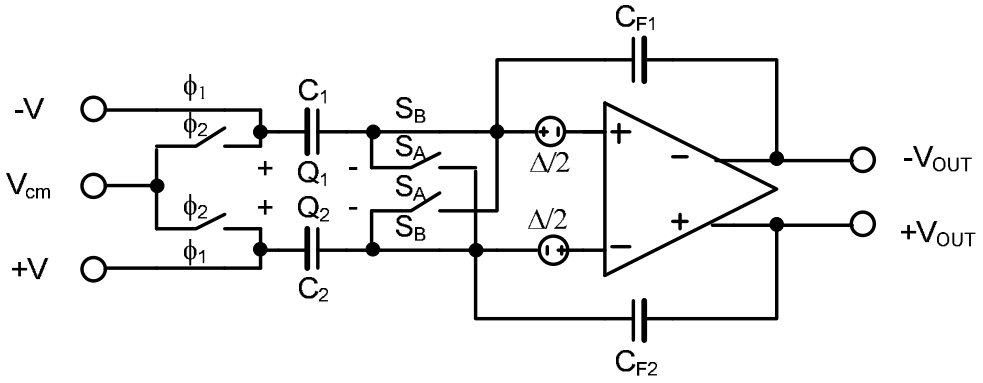
$$Q_{F2} = -(C(V+\Delta/2)-C(V_{cm}+\Delta/2)) = -C(V-V_{cm}) \tag{3.16}$$

and the differential charge is

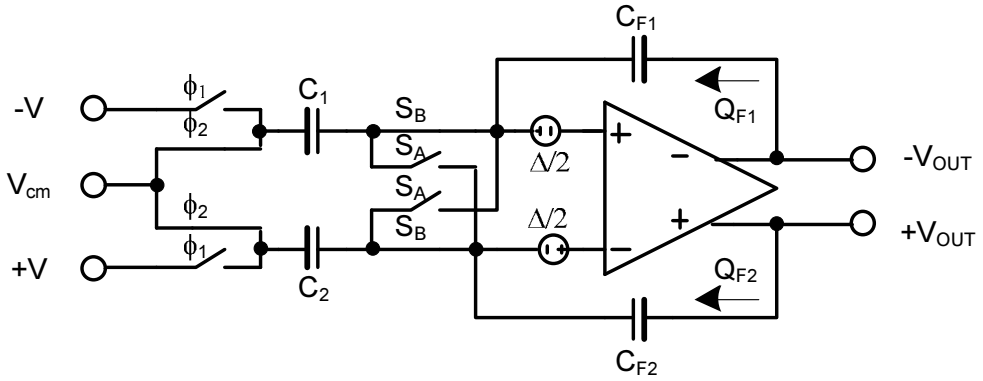
$$Q_{F2} - Q_{F1} = -2CV. \tag{3.17}$$

Equation 3.17 does not show any offset term.

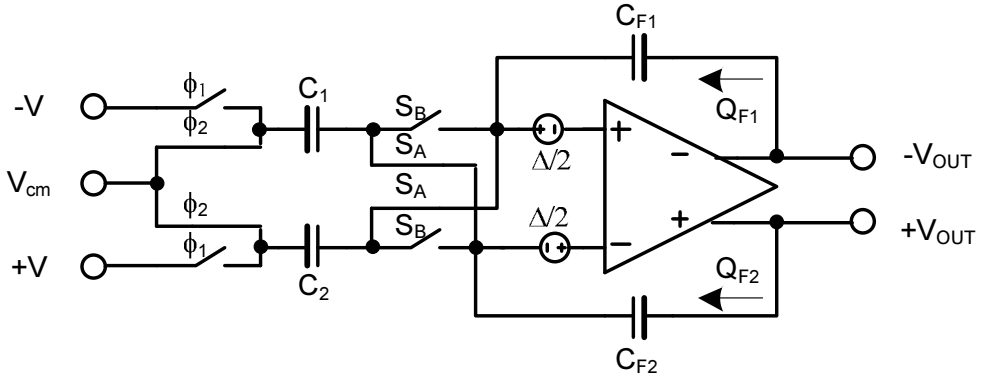
When the digital input data do not change, the integrated charge can be calculated by starting from Figure 3.10(a), i.e. the sampled charges are same as Equation 3.13 and 3.14. After changing the switch connections from ϕ_1 to ϕ_2 and from S_B to S_A (Figure 3.10(c)), the capacitors are discharged and hence the charges integrated into the integration capacitors are



(a)



(b)



(c)

Figure 3.10: Integrator operations of [37]: (a) $S_B=1$ and $\phi_1=1$, (b) $S_B=1$ and $\phi_2=1$, and (c) $S_A=1$ and $\phi_2=1$.

$$Q_{F1} = -(C(V+\Delta/2)-C(V_{cm}-\Delta/2)) = -C(V-V_{cm}+\Delta) \quad (3.18)$$

$$Q_{F2} = -(C(-V-\Delta/2)-C(V_{cm}+\Delta/2)) = C(V+V_{cm}+\Delta) \quad (3.19)$$

and the differential charge is

$$Q_{F2} - Q_{F1} = 2CV+2\Delta. \quad (3.20)$$

From the right-side term of Equation 3.20, we can see an offset term which is not differentially canceled out. This integration adds offset into the first integrator only when the output of DAC maintains and makes same problem as [30]

3.3.2. Stability of ΔΣ ADC Using A Bilinear Integrator

Senderowicz et al. [32] proposed the second-order modulator shown in Figure 3.11. The signal transfer function (STF) and NTF are given by

$$STF = \frac{K_1K_2(1+z^{-1})^2}{(K_1K_2-K_2)z^{-3}+(2K_1K_2+1)z^{-2}+(K_1K_2+K_2-2)z^{-1}+1} \quad (3.21)$$

$$NTF = \frac{(1-z^{-1})^2}{(K_1K_2-K_2)z^{-3}+(2K_1K_2+1)z^{-2}+(K_1K_2+K_2-2)z^{-1}+1}. \quad (3.22)$$

From Equation 3.21 and 3.22, the increased order of the modulator to the third brings stability problems. The parameters, K_1 and K_2 should be small and can be found by trial-and-error which is an inefficient way. Vleugels et al, [7] presented a method to remove the $(1+z^{-1})$ term of the feedforward path. However, her method has the stability problem because of $(1+z^{-1})$ terms at the feedback paths. Yang et al. [29] proposed a way to remedy the stability problem by replacing one of the $(1+z^{-1})$ feedback terms with z^{-1}. This method makes system design complicated [34] and is inapplicable to a low distortion architecture [4] which has only one feedback path to the first integrator. To understand the stability problem, a second-order low distortion ΔΣ ADC with bilinear feedback (Figure 3.12) is analyzed. The transfer function of $(1+z^{-1})/2$ is chosen for the feedback path to make DC gain equal to one.

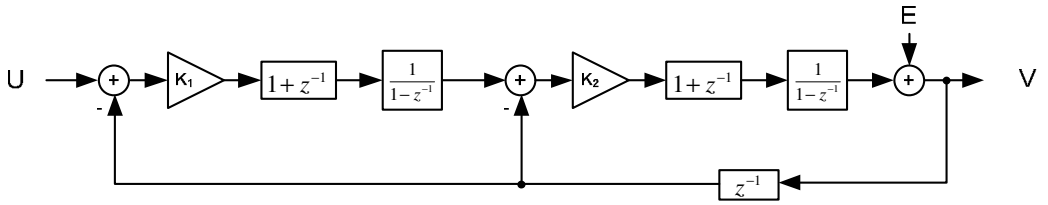


Figure 3.11: Senderowicz's second-order ΔΣ modulator.

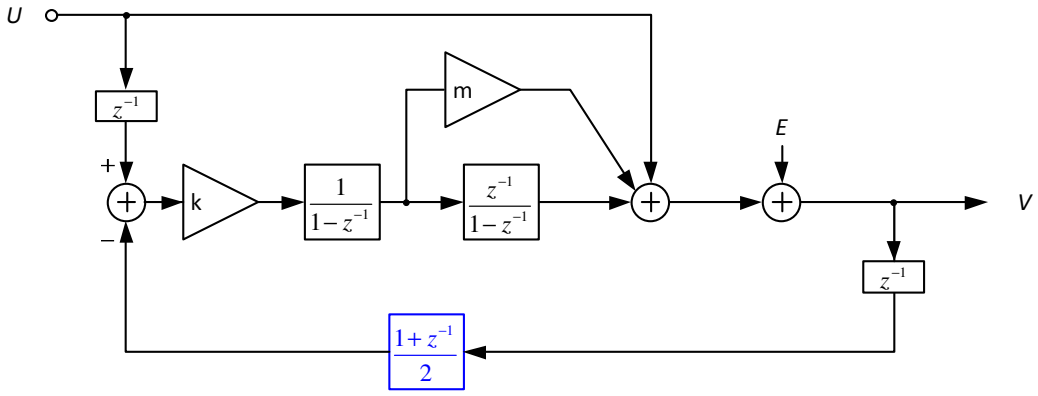


Figure 3.12: A second-order low-distortion ΔΣ modulator with the Senderowicz integrator.

The STF and NTF are given by

$$STF = \frac{(k-km+1)z^{-2}+(km-2)z^{-1}+1}{\frac{k}{2}(1-m)z^{-3}+(\frac{k}{2}+1)z^{-2}+(\frac{km}{2}-2)z^{-1}+1} \tag{3.23}$$

$$NTF = \frac{(1-z^{-1})^2}{\frac{k}{2}(1-m)z^{-3}+(\frac{k}{2}+1)z^{-2}+(\frac{km}{2}-2)z^{-1}+1}. \tag{3.24}$$

The stability of this loop becomes third-order one. To stabilize modulator loop, the poles of STF and NTF should be located the inside of the unit circle in the z-plane. Stable transfer functions can be found by sweeping one of two parameters, k and m, when we keep the other one constant with the MATLAB SIMULINK simulation. Three poles cannot be set independently because only two parameters are available. An example modulator is stabilized by k = 0.5 and m = 2.5. However, the performance of this modulator is degraded by 3 dB unlike the ideal one which does not have the $(1+z^{-1})$ term at the feedback path [38].

3.4. Proposed Double-Sampled Integrator 1

The proposed scheme is shown in Figure 3.13 [38]. This integrator has two more input capacitors in addition to the fully floating input capacitors of Figure 3.8 to eliminate the effect of the z^{-1} term which is the part of the $(1+z^{-1})$ term. Analysis of the proposed integrator starts when ϕ_1=1. First, the charges of the switched capacitors, C_1 and C_2, are

$$Q_1(n) = C_1[u(n) + u(n-1)] \tag{3.25}$$

$$Q_2(n) = -C_2[u(n) + u(n-1)] \tag{3.26}$$

and they are described by the summation of nth and $(n-1)$th data. The charges of two unswitched capacitors are

$$Q_3(n) = C_3[u(n) - u(n-1)] \tag{3.27}$$

$$Q_4(n) = -C_4[u(n) - u(n-1)] \tag{3.28}$$

and they are denoted by subtraction of $(n-1)$th data from the nth data. The total differential charge delivered to the feedback capacitor is

$$dQ = Q^+ - Q^- = (C_1 + C_2 + C_3 + C_4)\cdot u(n) + (C_1 + C_2 - C_3 - C_4)\cdot u(n-1). \tag{3.29}$$

Dividing Equation 3.29 by total input capacitance gives

$$\frac{dQ}{(C_1 + C_2 + C_3 + C_4)} = u(n) + \frac{(C_1 + C_2 - C_3 - C_4)}{(C_1 + C_2 + C_3 + C_4)}\cdot u(n-1). \tag{3.30}$$

The second term of Equation 3.30 is completely eliminated by the ideal capacitor values. When capacitor mismatches appear, Equation 3.30 becomes $(1+\delta z^{-1})$ where

$$\delta = \frac{C_1 + C_2 - C_3 - C_4}{C_1 + C_2 + C_3 + C_4}. \tag{3.31}$$

Performance degradation which comes from the $(1+\delta z^{-1})$ term is negligible compared with the circuit of Figure 3.8 because δ is typically less than 0.001 for CMOS processes. Since the charges represented by the equations from 3.25 to 3.28 remain the same during the phases, ϕ_1 and ϕ_2, noise folding cannot happen.

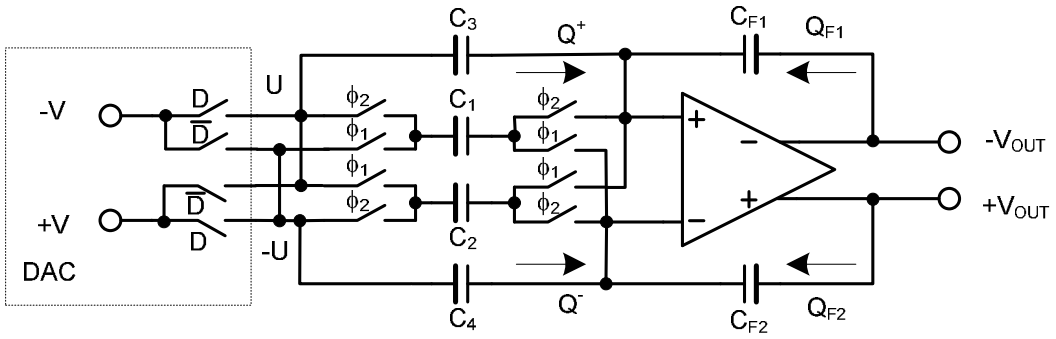


Figure 3.13: The proposed fully-floating SC integrator with a SC DAC.

The common-mode charge, $(Q^+ + Q^-)/2$, is rejected by the differential operation of the proposed integrator in the same way as the Senderowicz integrator.

3.4.1. Constant Offset Integration of The Proposed Integrator

There are two paths for the offset sampling of the proposed DS integrator. One is a pair of unswitched capacitors and the other is a pair of fully-floating capacitors. For the case of unswitched capacitors, offset sampling does not occur either with or without changing data. If the digital input data to the DAC do not change, obviously there is no switching and hence no offset integration. With changing input data from *D=1* to *D=0*, the charges integrated into C_{F1} and C_{F2} are

$$Q_{F1} = -(C(-V-\Delta/2)-C(V-\Delta/2)) = 2CV \tag{3.32}$$

$$Q_{F2} = -(C(V+\Delta/2)-C(-V+\Delta/2)) = -2CV \tag{3.33}$$

and the differential charge is

$$Q_{F2} - Q_{F1} = -4CV \tag{3.34}$$

for $C_1 = C_2 = C_3 = C_4 = C$ and same offset voltage assumption as in Figure 3.10. No offset term integrated by unswitched capacitors introduces charge transfer, because of unswitched virtual ground nodes.

For the other path, the offset voltage of opamp is always integrated by a pair of fully-floating capacitors. If the digital data do not change from *D=1*, effectively both sides of switches change, so the charges are

$$Q_{F1} = -(C(-V-\Delta/2)-C(V+\Delta/2)) = C(2V+\Delta) \quad (3.35)$$

$$Q_{F2} = -(C(V+\Delta/2)-C(-V-\Delta/2)) = -C(2V+\Delta) \quad (3.36)$$

and the differential charge is

$$Q_{F2} - Q_{F1} = -4CV-2C\cdot\Delta. \quad (3.37)$$

For changing input data from *D=1* to *D=0*, switches at inputs of opamp change and the charges which transfer into the integration capacitors are

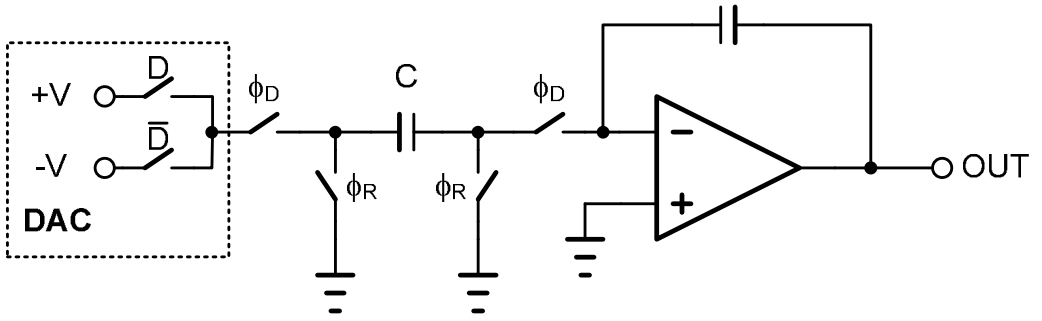
$$Q_{F1} = -(C(-V-\Delta/2)-C(-V+\Delta/2)) = C\cdot\Delta \quad (3.38)$$

$$Q_{F2} = -(C(V+\Delta/2)-C(V-\Delta/2)) = -C\cdot\Delta \quad (3.39)$$

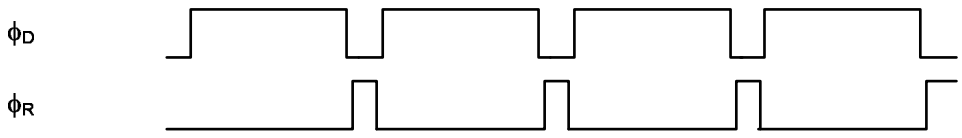
and the differential charge is

$$Q_{F2} - Q_{F1} = -2C\cdot\Delta \quad (3.40)$$

which is only offset charge. From Equation 3.37 and 3.40, a constant offset voltage is always integrated into the C_{F1} and C_{F2} regardless of changing data.



(a)



(b)

Figure 3.14: The proposed resetting SC integrator with a SC DAC (a) and (b) its timing diagram.

3.5. Proposed Double-Sampled Integrator 2

We can make another approach by thinking of the main reason of noise folding. The bad effect comes from the gain mismatch of two sets of sampling network. If we can use only one set of sampling network, this gain mismatch does not show up at the output of modulator. The integrator shown in Figure 3.14(a) uses only one capacitor which for both phase ϕ_1 and ϕ_2. Hence, this can be used for DAC feedback paths of integrator to eliminate mismatch-induced noise folding. However, it requires double-sampling phase, ϕ_D, and reset phase, ϕ_R, (Figure 3.14(b) to use this technique instead of double-sampling timing of Figure 3.1(c). Since the common-mode voltage is controllable for the switched-capacitor network, short pulse width of ϕ_R does not make huge transistor sizes of switches connected to the pulse width.

3.6. Summary

Various types of DS integrators were analyzed, and their disadvantages studied. To remedy those problems, novel DS integrators are proposed. The first one allows robust operation under path mismatch conditions, without introducing extra poles and zeros into the transfer functions. The second technique eliminates the main cause of noise folding by using only one set of sampling networks. These integrators allow a simple and efficient design method of DS ΔΣ ADCs. These modulators double the OSR. DS integrators are applicable for high speed operation without SNDR, area, and power penalties.

CHAPTER 4. WIDEBAND DESIGN TECHNIQUE 2

Timing of double-sampled integrator is examined to guarantee the stable operation of modulators. A fast data-weighted average (DWA) which has less idle tone is proposed to relax the timing of critical delay path and improve the performance of modulator.

4.1. Excess Loop Delay

Delta-sigma modulators with multi-bit quantizers often utilize DEM to filter the digital-to-analog converter (DAC) mismatch noise out of the signal band. DEM is performed by using a scrambler to shuffle the thermometer-coded quantizer outputs before they enter the feedback DAC. DWA [39] is the most popular DEM technique, because of its simple implementation. DWA achieves equal use of all DAC units over the long term. In each clock period, a scrambler cycles the thermometer-coded input bits following a rotation pointer. DAC elements which were not used in the preceding clock cycles take priority. For higher number of bits, the delay introduced by DWA gets longer, because of the increasing complexity of the thermometer-coded scrambler.

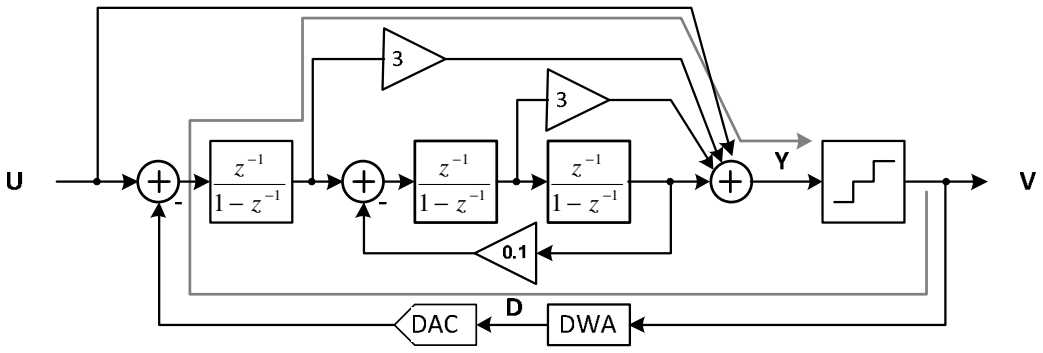


Figure 4.1: A third-order modulator with low-distortion architecture.

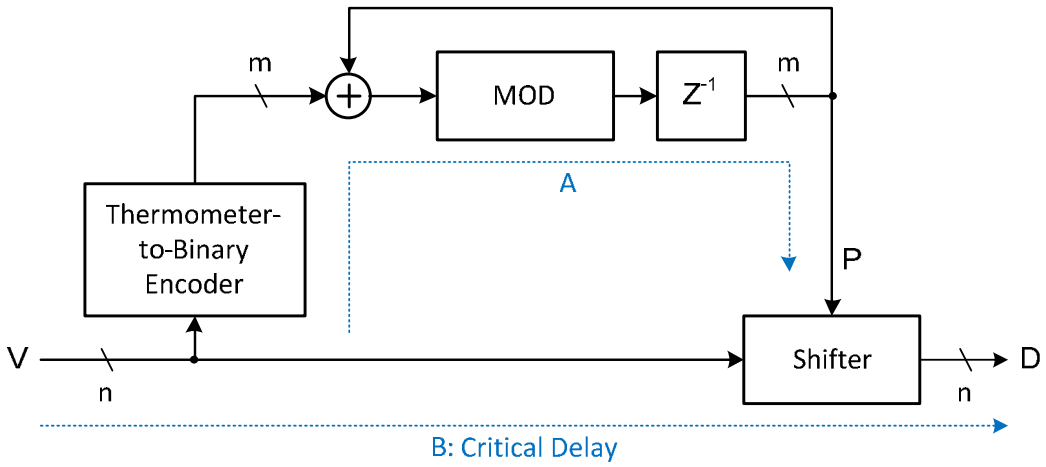


Figure 4.2: A block diagram of DWA

DS integrators have a loop which has only one delay (half-clock cycle for double sampling). For a third order modulator shown in Figure 4.1, the gray line shows the loop. Here, the delay time, z^{-1}, in the loop is used for the settling time of the integrator. It is same requirement as the integration time of single-sampled integrator but we do not have additional phase to make the whole system stable, i.e., quantizer and DEM circuits should work within the non-overlap time during low period of ϕ_D of Figure 3.14(b). This time sets up shortly to save power consumption of opamps. This is very stringent restriction when we design high-speed modulators. Wang [40] tried to use same way dealing the excess loop delay of continuous time modulators. Since it decreases the feedback factor of the adder (Chapter 2), this chapter concentrates on circuit-level treatments. A novel DEM technique which reduces the delay time is proposed here. The speed of quantizer is not going to be discussed here because it can be optimized by the dynamic operation presented in Chapter 2.

4.2. DWA Delay Estimation

DWA changes connection between thermometer-coded quantizer outputs and DAC capacitors to average the errors which come from process variation of DAC

capacitors. This DWA is placed in the feedback path of modulator (Figure 4.1). It consists of blocks for pointer-generation and a shifter as shown in Figure 4.2. The pointer-generation path (path A) has one delay, and hence the timing of this path can be relaxed. However, path B does not have any delay block but a shifter. The delay of the shifter decides the stability of modulator. Shifting function can be implemented with non-sequential logic shifters [41] such as logarithmic shifters or barrel shifters to guarantee that the delay time is less than the non-overlap time of clocks.

To find a fast shifter, we can simply compare delays between the shifters shown in Figure 4.3 and Figure 4.4 by using Elmore delay [42]. 4-bit shifters are selected to promise small swing of integrators. We need to model the switches as resistors and capacitors to use the equations of Elmore delay. Figure 4.5 shows the modeled RC networks of each shifter. We take the framed part of each shifter to simplify the RC networks. *V* and *Db* are named the same as the notation of Figure 4.3 and 4.4. We assume that the resistances of inverters (R_M) are 3 times smaller than switches (R_{SW}), $C_{S0}=C_{S1}=C_{D0}=C_{D1}=C_S=C_D=C$, the input capacitance of inverters is 6C, and the output capacitance of inverters is 3C. (These assumptions are not accurate but good enough to get intuition.) Then

$$\tau_{Log4} = 5R_MC + 4(R_M + R_{SW})C + 4(R_M + 2R_{SW})C + 4(R_M + 3R_{SW})C + 8(R_M + 4R_{SW})C = 193R_MC \quad (4.1)$$

$$\tau_{Bar4} = 17R_MC + 20(R_M + R_{SW})C = 97R_MC. \quad (4.2)$$

Equation 4.1 and 4.2 are delay times of shifters which process 15-bit thermometer-coded quantizer outputs. *C* represents the total parasitic capacitance of the switch transistor including overlap and diffusion capacitance. The barrel shifter is almost twice faster than the logarithmic shifter because of low series resistance. However, the delay of the shifter is not reduced enough for high speed DS modulator.

(This will be discussed in Chapter 6.) Partitioning DWA [7] is one way to reduce the delay time as much as the capacitance reduction of multiplexer (MUX). From Figure 4.6, we can calculate the delay time of the partitioned DWA which has 8-bit thermometer-coded inputs as

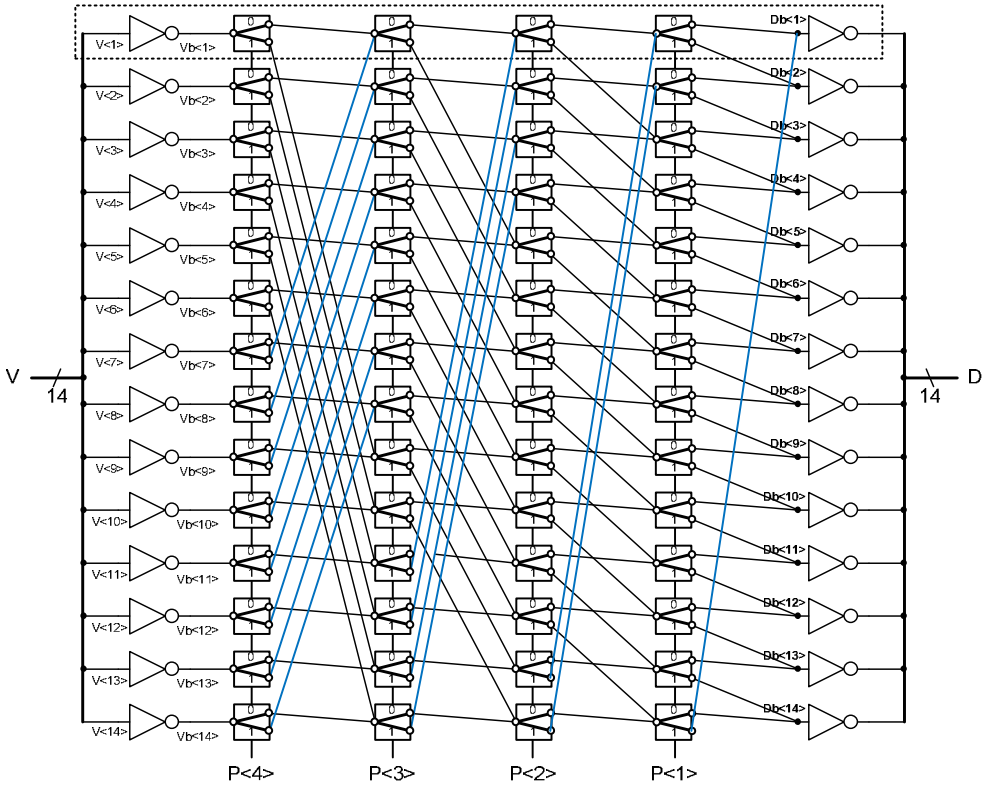
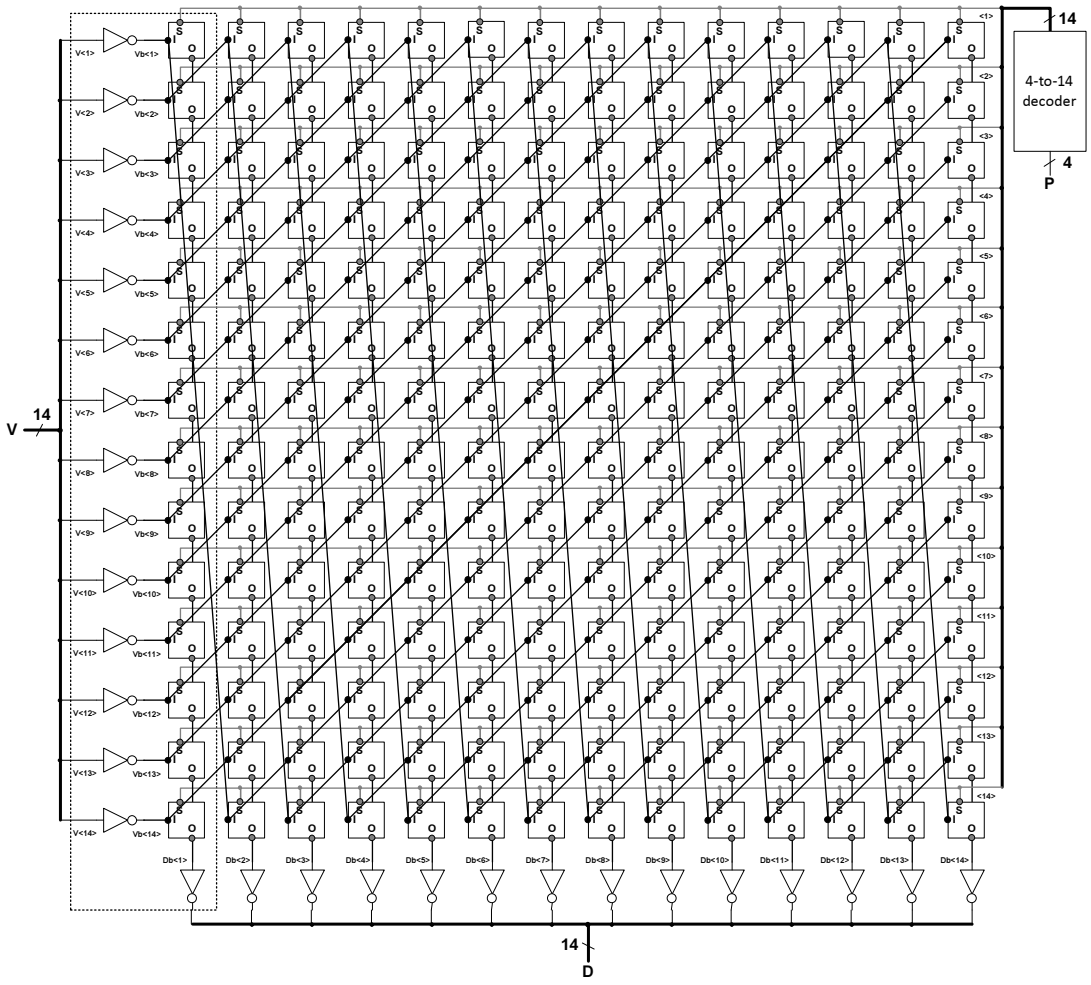
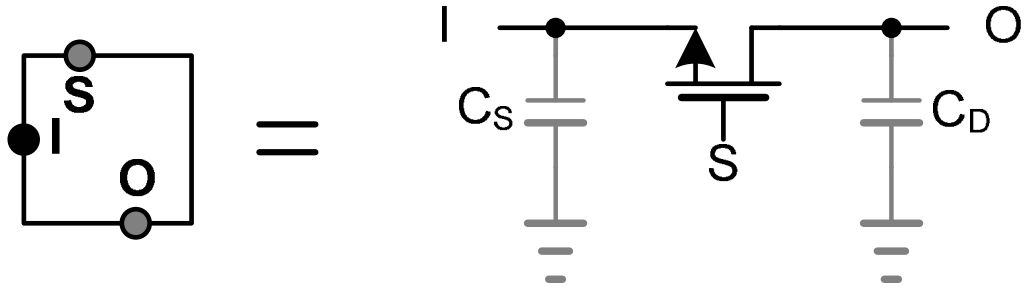


Figure 4.3: (a) A logarithmic shifter with 15-level thermometer-coded quantizer outputs and (b) the detail of the simplified block.

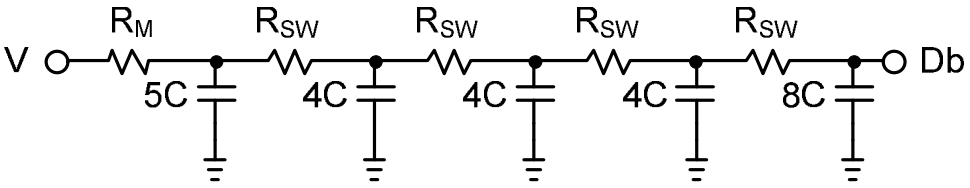


(a)

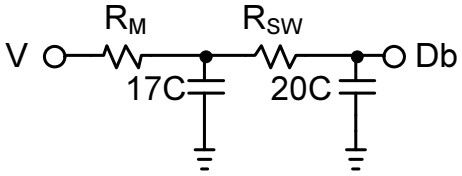


(b)

Figure 4.4: (a) A barrel shifter with 15-level thermometer-coded quantizer outputs and (b) the detail of the simplified block.

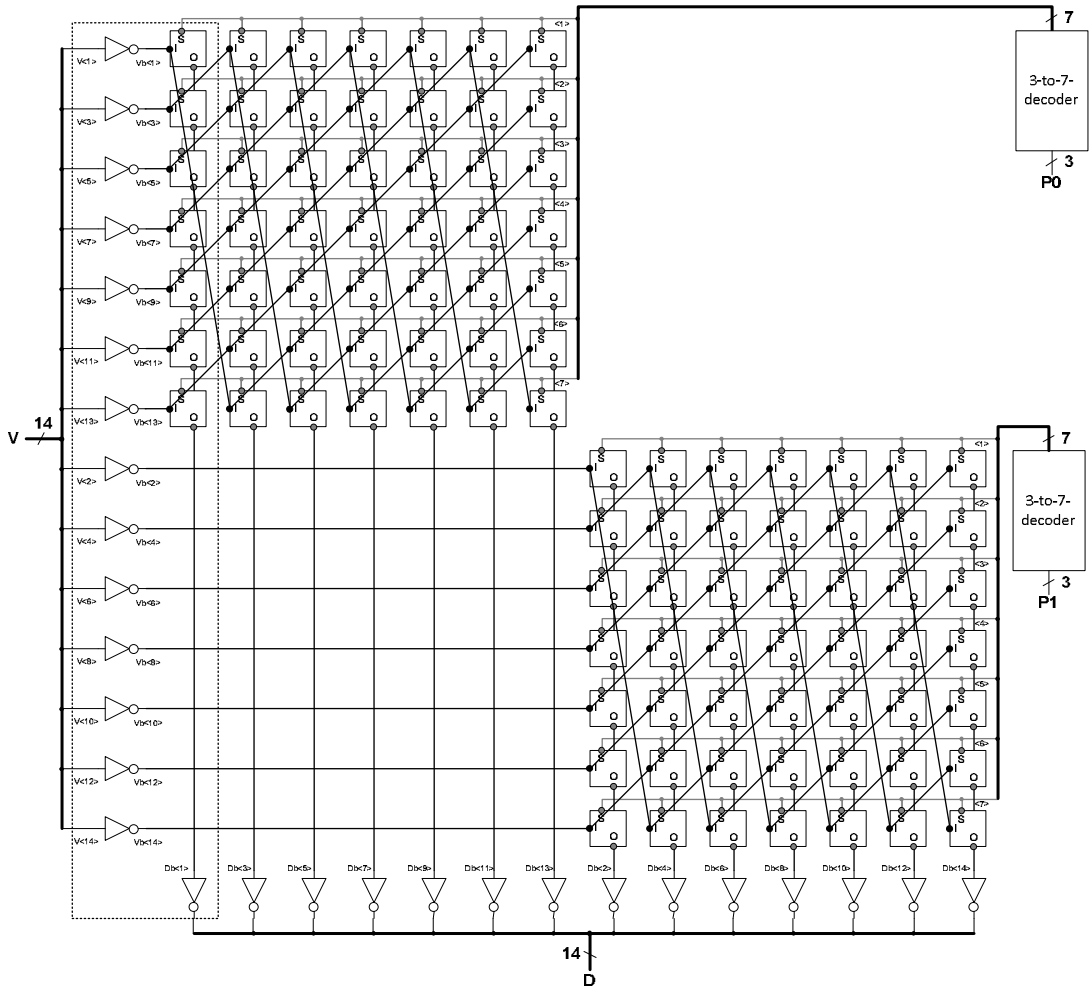


(a)

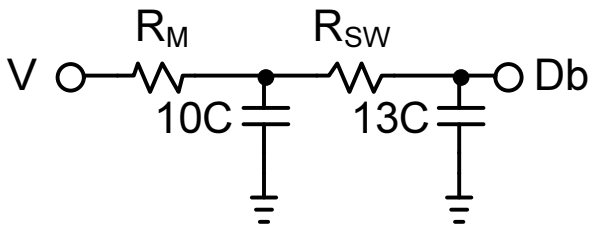


(b)

Figure 4.5: Modeled RC networks for (a) the logarithmic shifter of Figure 4.3(a) and (b) the barrel shifter of Figure 4.4(a).



(a)



(b)

Figure 4.6: An 8-level barrel shifter: (a) block diagram and (b) RC model.

$$\tau_{Bar2} = 10R_M C + 13(R_M + R_{SW})C = 62R_M C. \tag{4.3}$$

Now the delay of partitioned DWA is minimized to almost one third of Equation 4.1. However, this scheme has poor tonal behavior with small input signal.

4.3. Tonal Behavior

In P-DWA [7], the DAC is divided into odd- and even-indexed units, and the output is a combination of elements selected from the two sets. If a barrel shifter is used in the scrambler, the delay of each DWA can be cut to two thirds (this ratio depends on the buffer size at the output of DEM) by removing the half of scrambler transistors as we discussed in the previous section. However, the system will not equalize exactly the usage of the DAC elements, since the selection always starts from the odd-indexed set. The resulting error is inherent in P-DWA, and it accumulates with time. Evaluated over infinite time, it contributes a dc error. Over a finite time period, it results in a low-frequency error. Detailed analysis shows the mean-square value of the error is given by

$$\overline{E^2} = \frac{1}{N} \sum_{i=2,4,\ldots}^{N} (e_i - \bar{e})^2. \tag{4.4}$$

Here, N is the number of elements, e_i is an odd-indexed error and $\bar{e}$ is the mean value of all errors. Figure 4.7 plots the total usage of even and odd-indexed elements in P-DWA, obtained by simulation of a third-order low-distortion delta-sigma modulator (Figure 4.1). The *x* axis shows time in multiples of the sampling period *T*,

and the *y* axis represents the total number of rotations by the pointers. -55dBFS input is assigned for this simulation. Over time, the difference between the usages of even and odd pointers increases linearly, and this introduces a DC input even though no input signal is forced into the modulator. When the input signal is small, this DC portion creates idle tones with DWA because of the limit-cycle characteristic of the first-order noise-shaping [14]. Alternating the choice of the first element between the two sets can reduce the DC output of DWA circuit, as proposed in [8], which introduced SeDWA. Here, we simplify the switching scheme between segmentations from data-dependent to clock-alternating switching. MATLAB SIMULINK simulation result (Figure 4.8) with the modulator of Figure 4.1 shows that tones can be suppressed by the alternation of pools. OSR of 8 and -55dBFS input are used. However, SeDWA still needs additional switches in the critical path to alternate the connections. This increases the delay of feedback path and hence the chance of instability.

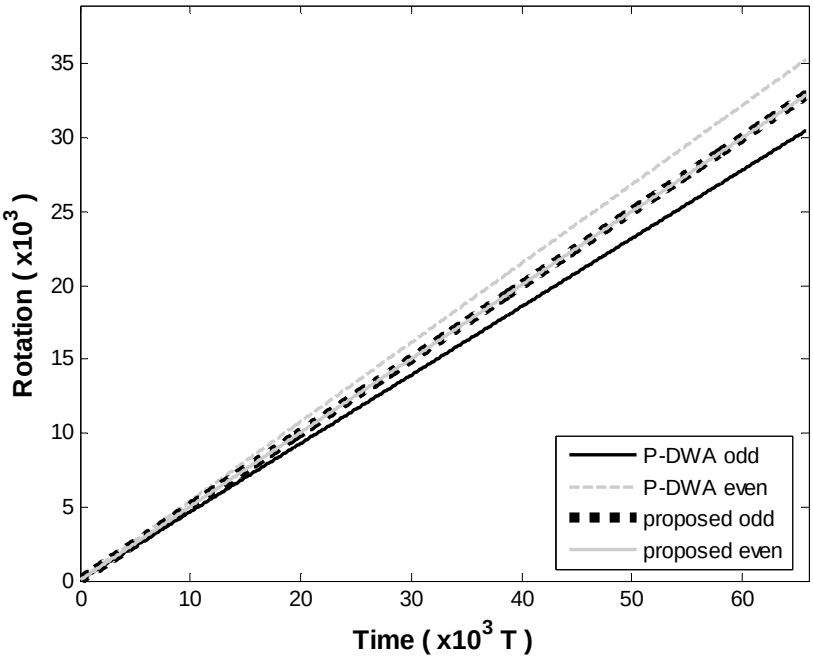


Figure 4.7: Rotations of DWA pointers

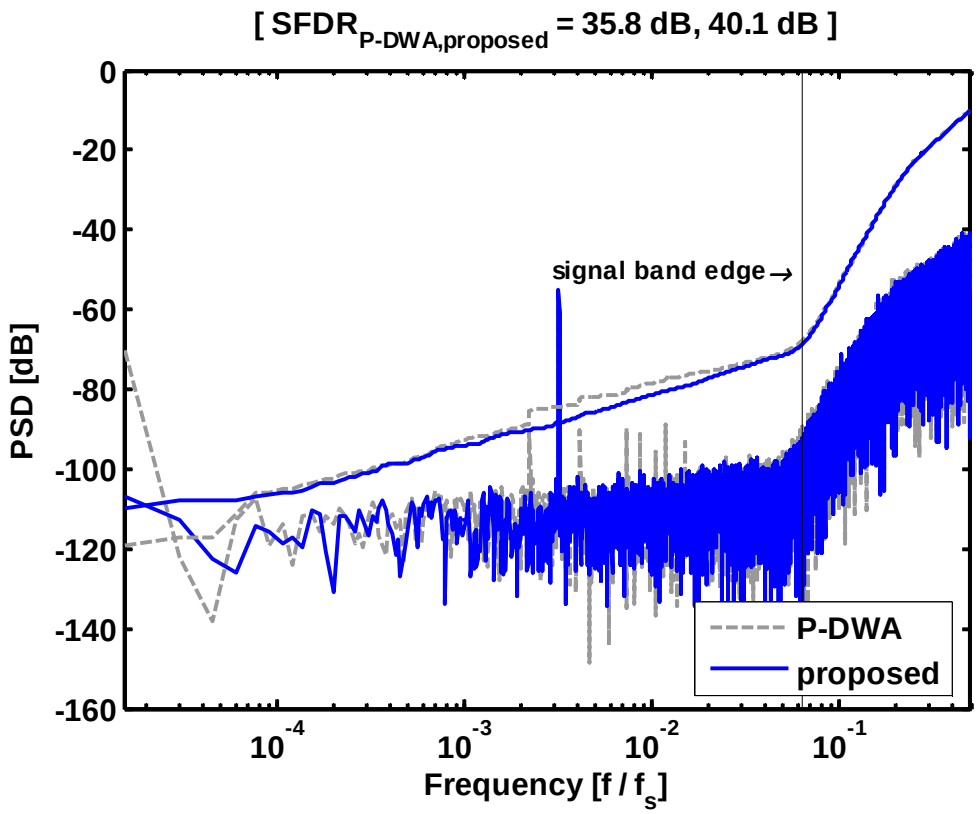


Figure 4.8: Power spectral density with P-DWA and the proposed scheme

The structure of Figure 4.9 shows a simplified implementation of the improved SeDWA for the 15-level quantizer block of Figure 4.6(a). Each of the 14 comparators has two reference inputs, which alternate between even- and odd-indexed values. By placing the alternating switches at the reference inputs of the comparators, the additional delay required for switching is avoided. These switches operate when the clock signal changes from ϕ_1 to ϕ_2 and back. Since the alternation is data independent, the switches can be operated at the beginning of the every integration cycle. Figure 4.9 shows the implementation of a barrel shifter, but the scheme is also applicable to logarithmic shifters. As shown in Figure 4.7, for the proposed scheme, the difference between the usages of even- and odd-indexed elements is minimal. Table 3 compares the performances of the four DWA algorithms.

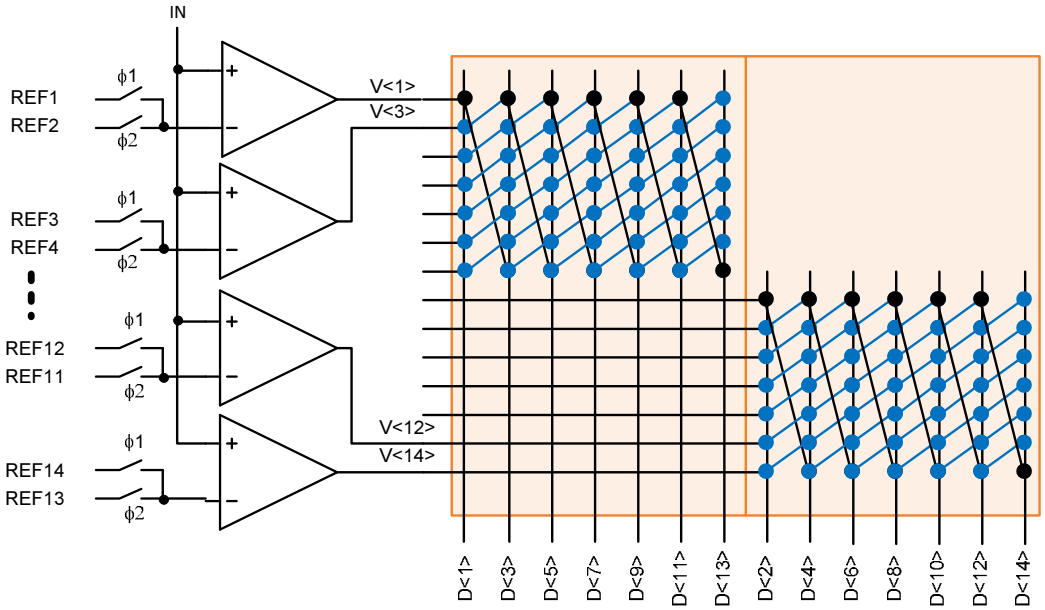


Figure 4.9: An alternation technique with two partitioned barrel shifters.

Table 4.1: Comparison of different types of DWAs

	DWA [39]	P-DWA [7]	SeDWA [8]	Proposed
Complexity	+	•	-	•
Speed	-	+	-	+
Tonal behaviour	-	-	+	+

(+ : good, • : medium, - : bad)

CHAPTER 5. SYSTEM DESIGN

The structural design of an example modulator is presented in this chapter to achieve a low-power and wideband ΔΣ ADC. Third-order, OSR of 8, and low-distortion architecture are selected for 20MHz bandwidth and 72dB SNDR. A multi-cell architecture which gives higher performance than single-cell modulator is discussed. MATLAB SIMULINK simulation results verify the system-level design.

5.1. Modulator Structure

The first step to decide the structure is assigning the noise budget for quantization noise from the target specification of Table 5.1. For audio-band and high-resolution delta-sigma ADCs, about 75 percent of noise budget [14] is assigned for thermal noise because quantization noise is cheap to filter out of the signal band with high OSR. Only 5 percent of noise is used for quantization noise. However, for wideband delta-sigma data converters, a high OSR is not applicable because of high power consumption of wideband opamps and high-speed digital circuits, even though these constraints get reduced by advanced technologies. Here, 40 percent of noise budget is set by thermal noise and 40 percent is assigned for quantization noise. The last 20 percent is used by DAC mismatch and other circuit noises. From the Table 5.1, the in-band quantization-noise can be -83dB, and the signal-to-quantization-noise-ratio (SQNR) is 79dB when we set the maximum input power at -4dBFS.

Table 5.1: Summary of target specification

Parameter	Value
Signal Bandwidth	20MHz
SNDR	72dB
Process	0.18μm 2poly-4metal

To satisfy the target SQNR, we have design choices such as architecture, OSR, quantizer bit, and the order of loop filter. Low-distortion architecture is chosen for the low power consumption of integrators and modulator as we discussed in Chapter 2. Since we use 0.18μm process, the clock frequency cannot be made too high, and hence an OSR of 8 is selected here for a 320MHz sampling frequency. The power consumption of opamps can be minimized by the increasing number of quantizer bits. However, design complexity and power of quantizer, also, increase with this number. To balance these two things, 15-level (3.9bit) is used here with the fast DWA segmented by two groups.

The order of modulator can be decided by equations from 5.1 to 5.3 [43].

$$SQNR_{\max\_2nd} = 6.02N + 1.76 - 12.9 + 50\log(OSR) \quad (5.1)$$

$$SQNR_{\max\_3rd} = 6.02N + 1.76 - 21.4 + 70\log(OSR) \quad (5.2)$$

$$SQNR_{\max\_4th} = 6.02N + 1.76 - 30.2 + 90\log(OSR) \quad (5.3)$$

They are all in dB. N is the number of quantizer bits and OSR is the oversampling ratio. First order and higher order than fifth are not considered here because of low SQNR and stability issue. By substituting for N and OSR 3.9 (i.e., 15 levels) and 8, respectively the SQNRs of equations from 5.1 to 5.3 are obtained as 57.5dB, 67dB, and 76.3dB, respectively. Third-order modulator is chosen here because of the low SQNR of second-order modulator and the stability issues of forth-order modulator.

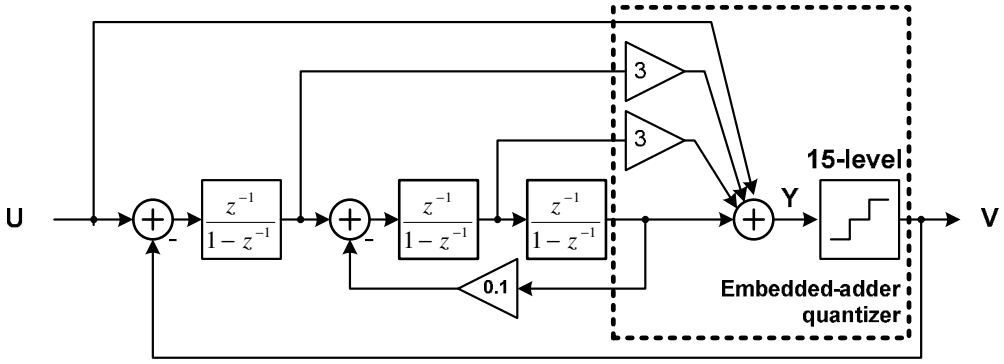


Figure 5.1: A third-order low-distortion modulator with zero optimization

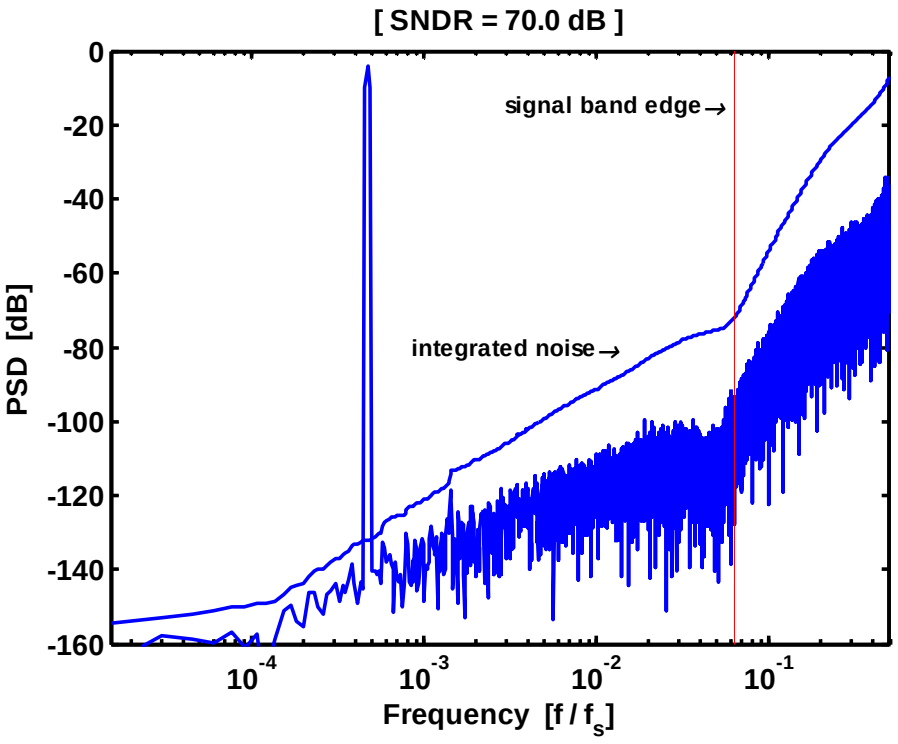


Figure 5.2: Power spectral density of Figure 5.1

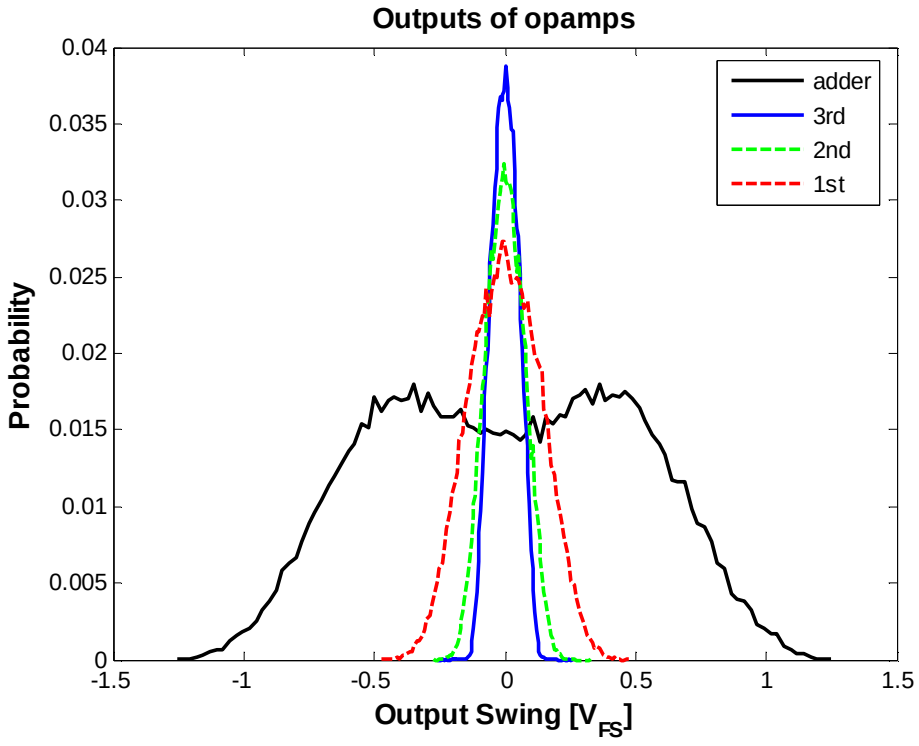


Figure 5.3: The output swing of modulator opamps

Third-order modulator, also, has the possibility of unstable operation. However, this can be managed by the embedded-adder quantizer of Chapter 2. Pole optimization which increases the stability of modulators is not applied here because it degrades the SNQR by decreasing the out-of-band gain of the NTF [14]. To mitigate the lack of SNR requirement, zero optimization of loop filter is adopted. SQNR can be improved by 8 dB and becomes 75dB. Since 75dB SNR is calculated assuming a 0dBFS input signal, it should be adjusted to 71dB with -4dBFS input signal. Figures 5.1 and 5.2 show a designed modulator and the power spectral density (PSD) of this modulator. Output swings of opamps are plotted in Figure 5.3. Since the swings are not large, telescopic opamps can be adopted. We will be back to this issue when circuit-level design is presented.

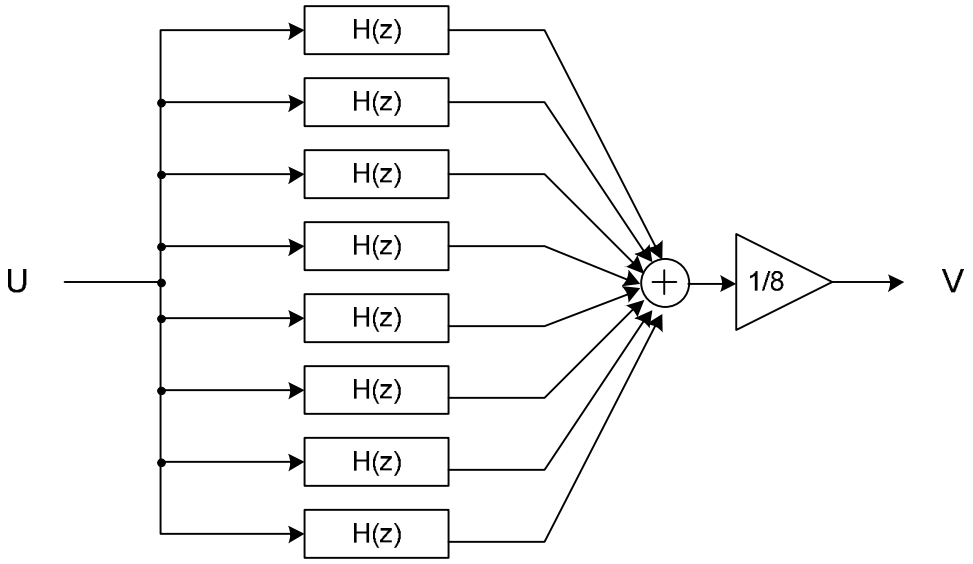


Figure 5.4: The block diagram of the proposed 8-cell modulator.

5.2. Multi-cell Architecture

From the previous design, the performance of modulator needs to be improved by 8dB to meet the target specification. This requirement can be satisfied by the multi-cell architecture [44-45] shown in Figure 5.4 without redesigning single-cell modulators. In this structure, *H(z)* is the third-order low-distortion modulator of Figure 5.1. Eight-cell architecture can be adopted providing robust performance and easy programmability. The gain block of 1/8 has the same output power as input signal, but less noise power because the noises are not correlated with each other. Hence doubling the number of cells improves the SQNR by 3 dB and the overall modulator performance achieves a 9 dB SQNR improvement over that of a single cell. The simulation results for 1-cell and 8-cell are shown in Figure 5.5. 9dB improvement is clearly shown in this figure.

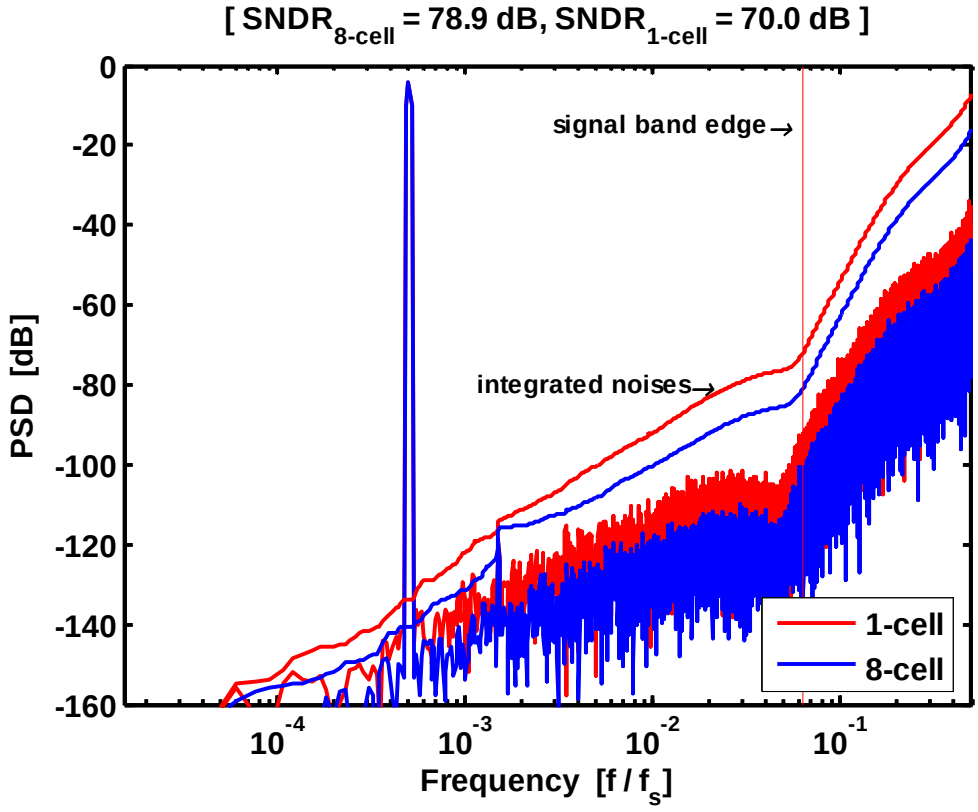


Figure 5.5: Power spectral densities of 1-cell and 8-cell ADCs

To demonstrate the programmability, simulation results are summarized in Table 5.2 with various numbers of activated cells. It shows negligible performance degradation with few disabled cells for MATLAB simulation. The gain of whole modulator after summation block is kept to 1/8 to check the robustness of modualtor.

Table 5.2: SQNR vs. number of activated cells

Number of activated cells	SQNR [dB]
8	78.9
7	78.3
6	77.7
5	76.9
4	75.8
3	74.8
2	73.1
1	70.0

CHAPTER 6. CIRCUIT DESIGN

In this chapter, we design a single-cell modulator because the multi-cell architecture was proven by the previous work [46]. Figure 6.1 shows a single-ended circuit-level implementation of the modulator presented in Figure 5.1. The double-sampled integrator proposed in Chapter 3 is applied for the first integrator. Other integrators and zero optimization have two sets of sampling capacitor to relax the sampling time. Embedded-adder quantizer proposed in Chapter 2 is used to achieve fast and low-power operation and hence separate adder does not required. Improved SeDWA is implemented to promise the smallest delay of the critical path and harmonics of DEM mismatch. SPECTRE simulation verifies the proposed ideas.

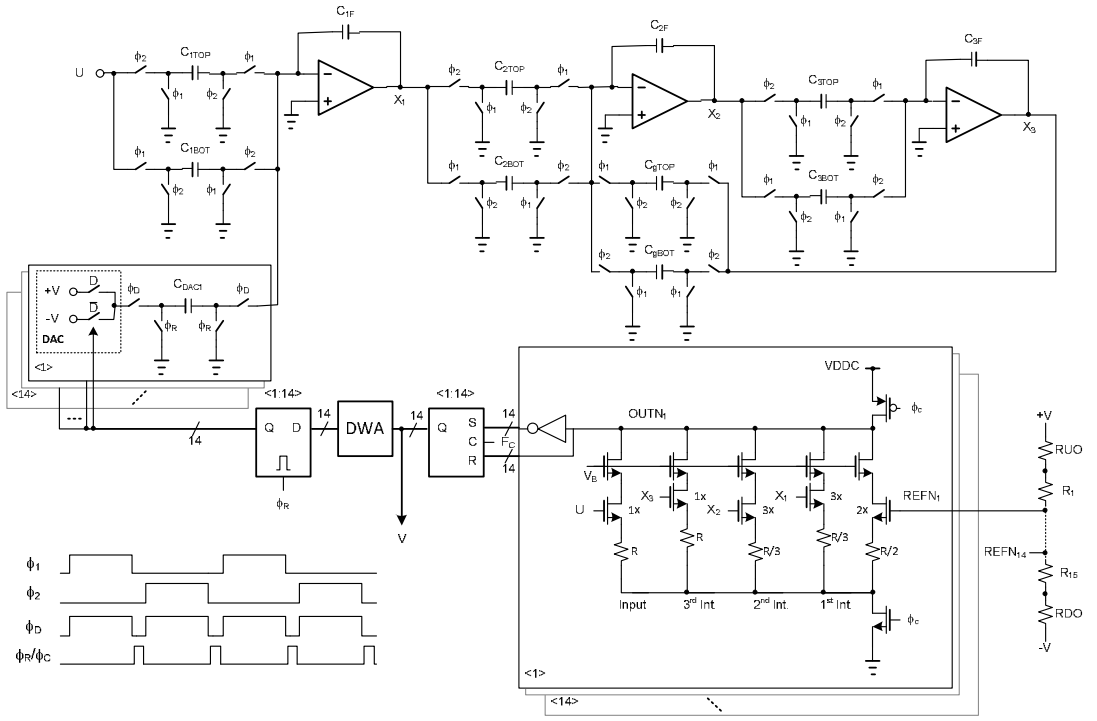


Figure 6.1: A single-ended version of the whole modulator shown in Figure 5.1

6.1. Opamp Design

Most power-efficient opamps are single-stage opamps which do not have folding and gain-boosting techniques [19]. They have the minimum swing ranges at the input and output. For switched-capacitor networks, input voltages of opamps are not problematic because they are fixed by the common-mode voltage of switched-capacitor networks and do not change a lot. For the low-distortion architecture of Figure 5.1, output swings are also reduced by the input feedforward path and hence the single-stage opamps are good enough to achieve the minimum power consumption.

To simulate the gain requirement of opamps, the ideal integrators of Figure 5.1 are replaced by the realistic model of Figure 6.2 [47] when the gains of integrators are set to one. A_0 represents the DC gain of opamp. The gain of each opamp is estimated after setting the gains of other opamps to 100dB. In Figure 6.3, SNDRs are plotted by sweeping opamp gains.

For the first and the second integrators, 30dB gain is acceptable, but 40dB is selected here to prepare gain degradation which comes from the P.V.T variation. The telescopic opamp shown in Figure 6.4 has enough gain to satisfy this requirement. For the third integrator, the 30dB opamp of Figure 6.5 is selected to minimize opamp bias current.

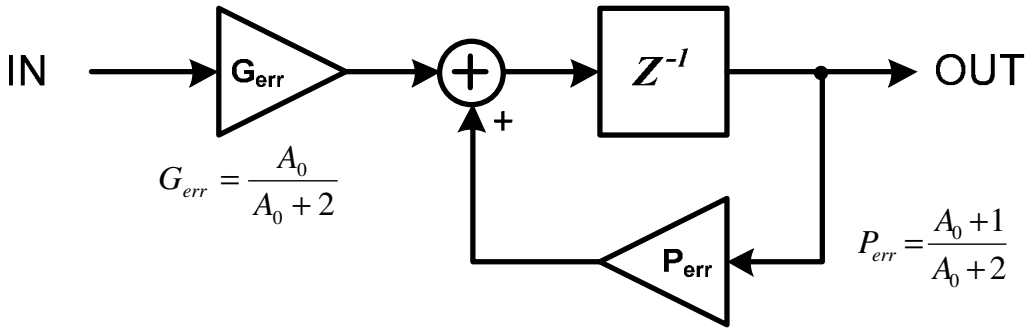


Figure 6.2: An integrator model with the finite gain error of opamp

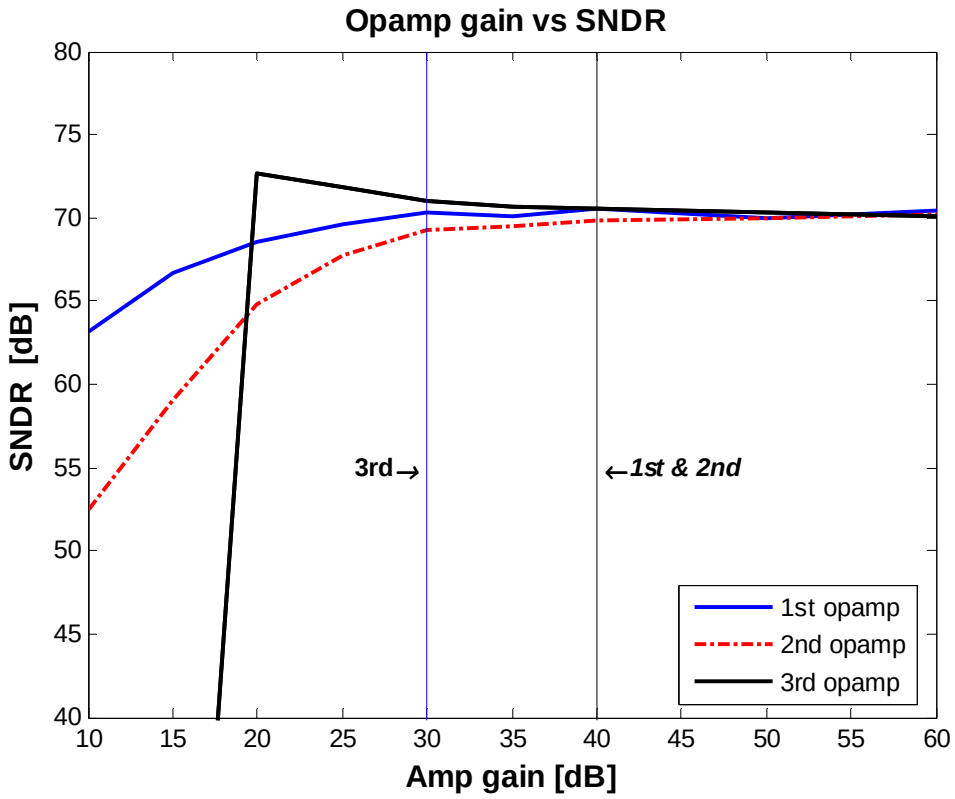


Figure 6.3: Simulated SNDR of the modulator of Figure 5.1 when sweeping opamp gains

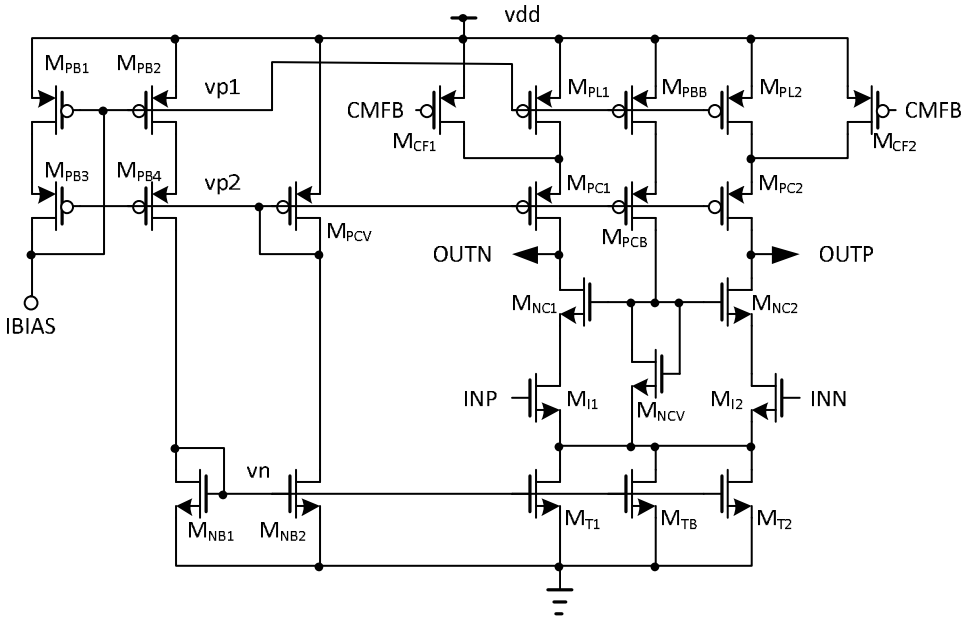


Figure 6.4: A single-stage telescopic opamp

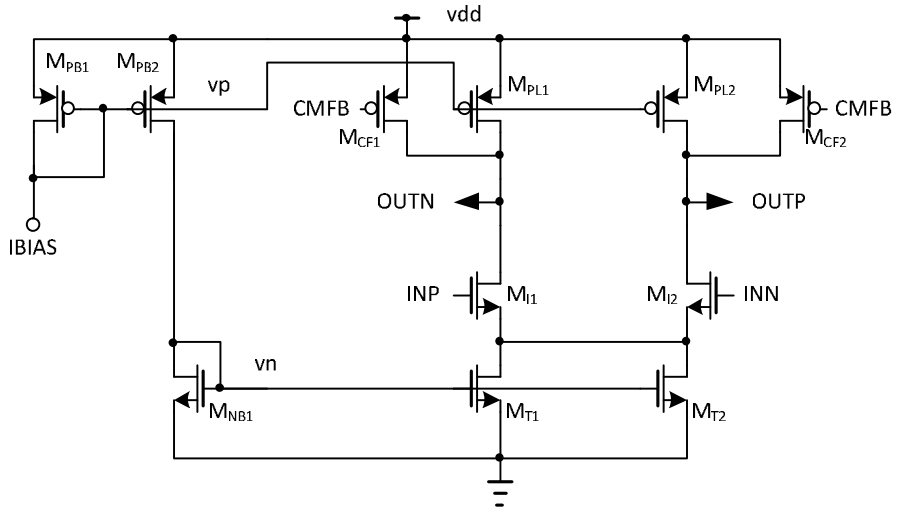


Figure 6.5: A single-stage opamp

The capacitor sizes are decided by the noise budget discussed in Chapter 5. The allowable thermal noise is 40 percent of total noise. The calculated noise power is

$$v_n = \sqrt{\frac{0.20}{10^{(SNR+4)/10} \times 0.4}} = 141\mu V_{rms} \tag{6.1}$$

when -4dBFS of input signal power is assumed. The noise voltage of Equation 6.1 is used to calculate the sampling capacitor size of the first stage. From the noise analysis of [48], the input sampling capacitor of the first stage is

$$Cs = \frac{2kT}{v_n^2 OSR} \tag{6.2}$$

when we assume the transconductance of opamp input transistors is much higher than the inverse of switch resistances. Since the proposed double-sampled integrator has two separate sampling capacitors and differential inputs and output, the recalculated input sampling capacitor is

$$Cs = \frac{8kT}{v_n^2 OSR} = 208\,fF \tag{6.2}$$

where k is 1.38×10^{-23} J·K^{-1}, Temp is 300K, and OSR equals 8. To leave a design margin, the capacitance is set to 280fF. Capacitor ratios of first to second and second

to third stages are set to 2.8 and 2, respectably to make small contribution of *kT/C* noises.

Table 6.1 shows the summarized opamp design parameters. C_s is the sampling capacitance of each stage. β is the feedback factor of integrators when we ignore the parasitics of opamp inputs and g_m is the transconductance of input transistors, M_{I1} and M_{I2}, shown in Figure 6.4 and 6.5. Now, we are ready to calculate opamp bias current with the transconductances of opamps. The equation for the bandwidth calculation is

$$\omega = \frac{1}{\tau} = \frac{g_m \beta}{C_L} \tag{6.3}$$

where C_L is the load capacitance of opamp.

Table 6.1: Summary of opamp design

Stage	C_S[fF]		β	DC gain [dB]	UGBW [MHz]	g_m [mS]	Current [uA]	Input-referred noise [V]
First	Input	280	0.33	62.2	404	4.04	600	3.98E-05
	DAC	20x14						
Second	Input	100	0.50	60.6	348	1.34	240	6.31E-05
	Zero	10						
Third	Input	50	0.50	30.1	474	0.59	90	8.91E-05

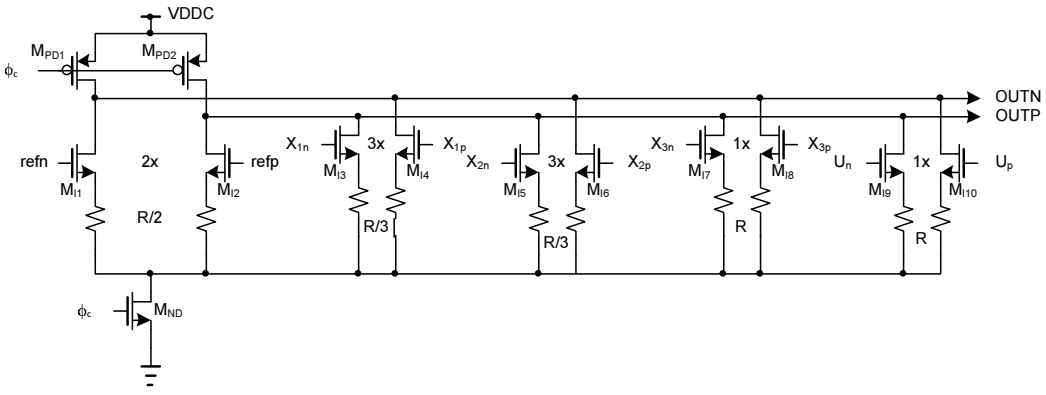


Figure 6.6: An embedded-adder quantizer without cascode stages

6.2. Embedded-Adder Quantizer

Even though the proposed embedded-adder quantizer was presented in Chapter 2, three things should be considered to complete the circuit-level design. First is the kickback noise of adder. Figure 6.6 shows an embedded adder without cascode stages. Since the output swings of preamplifiers change from *VDDC* to *GND* and the number comparators is 14, the kickback noise coming through the transistors M_{I1} to M_{I10} is not negligible. They make common-mode pulses which give stringent timing requirement to the common-mode feedback circuit of opamp. These errors are sampled by the sampling capacitors of Figure 6.7. This figure has the first integrator, the second-stage sampling capacitors, and the part of the embedded-adder quantizer. Figure 6.8 shows SPECTRE simulation result of Figure 6.1. The noise floor rises up and degrades the performance of modulator. By using cascode stages (Figure 2.8) and series input resistors, the kickback noises are reduced and their effects are negligible. Figure 6.9 shows simulation result with the kickback reduction techniques.

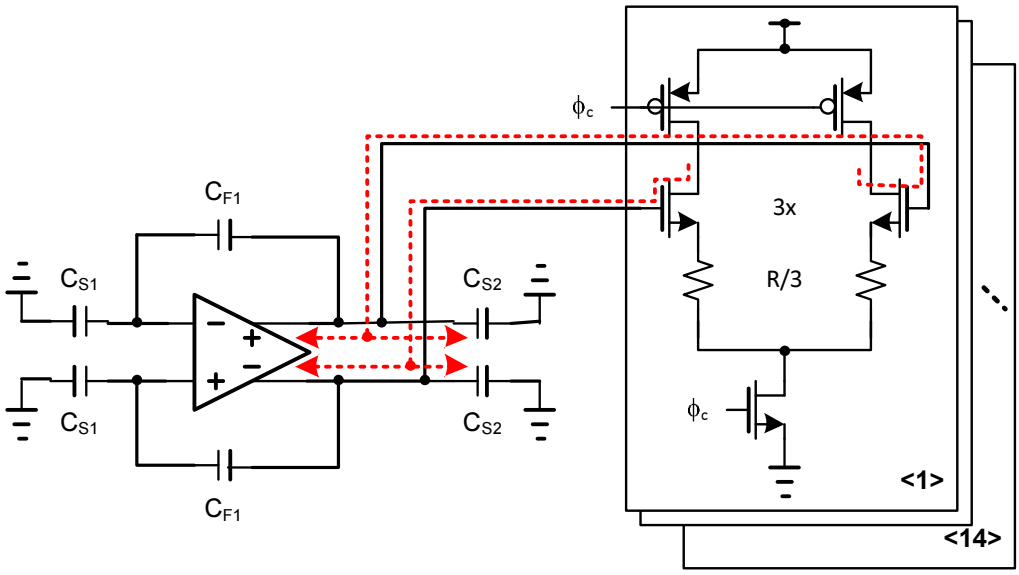


Figure 6.7: Kickback noise from quantizer to the first integrator and the sampling capacitors of second stage

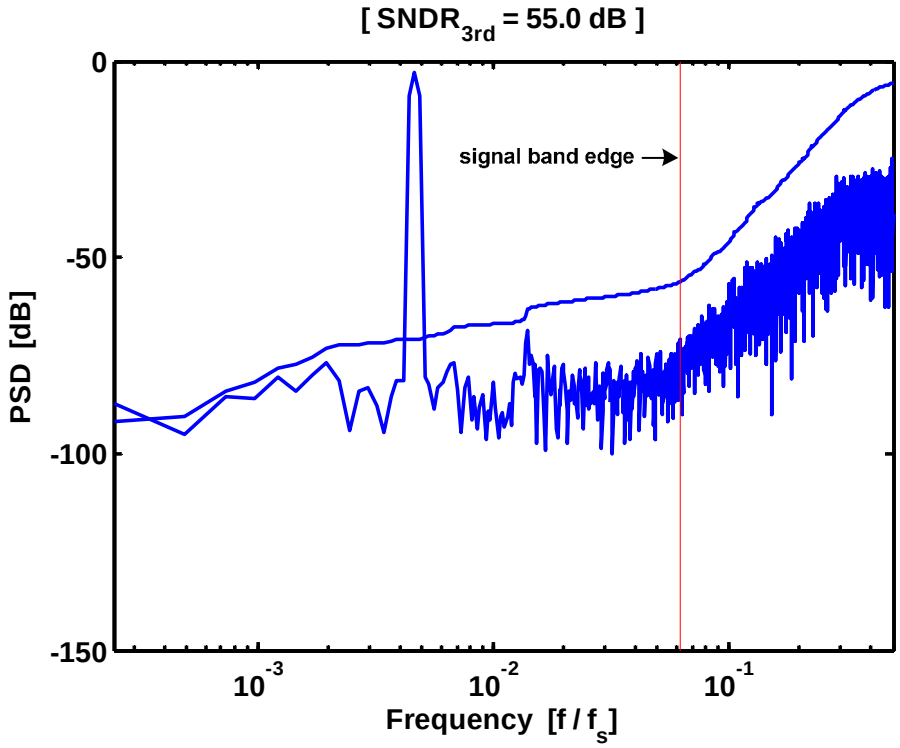


Figure 6.8: PSD of the modulator with the quantizer of Figure 6.6

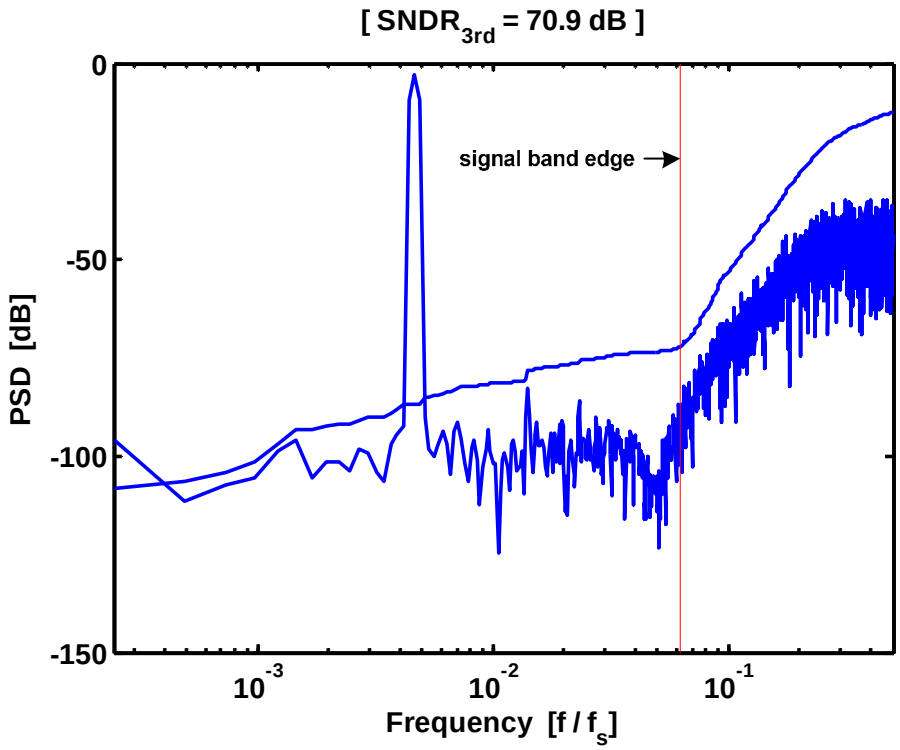


Figure 6.9: PSD of the modulator with the kickback reduction techniques

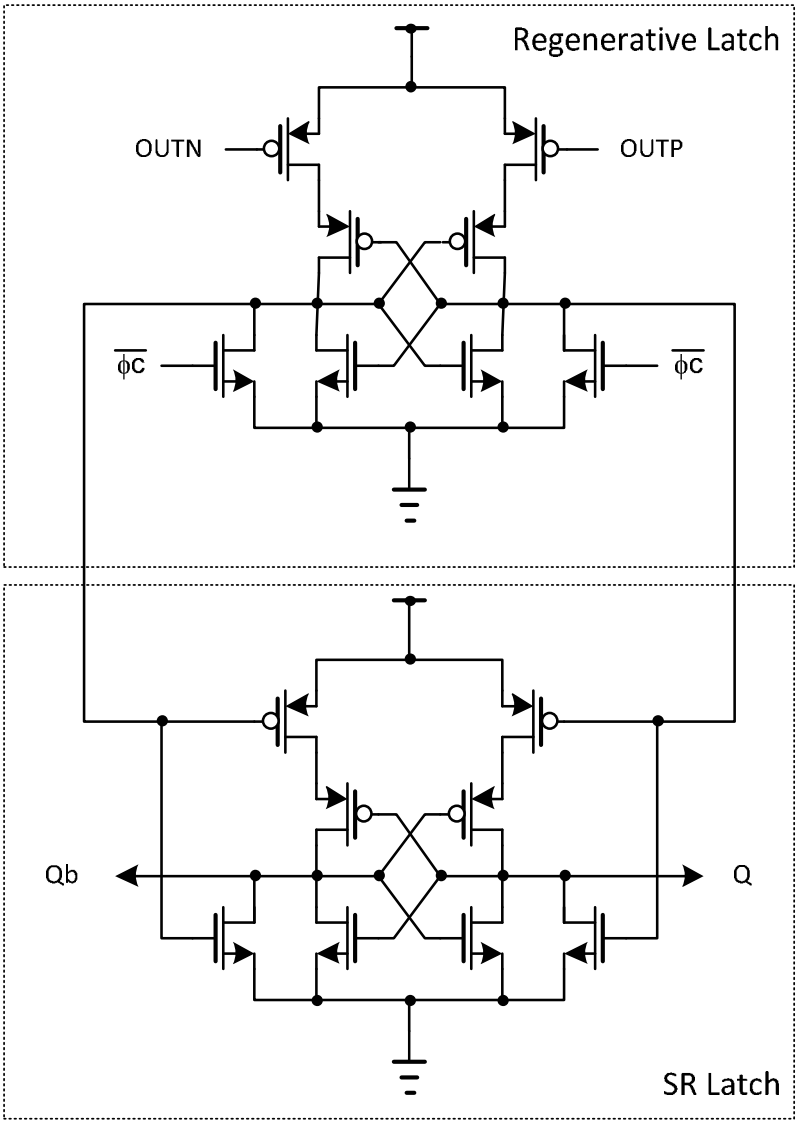


Figure 6.10: A latch follows the embedded-adder quantizer

Secondly, the latch which is the part of the proposed quantizer consists of two blocks as shown in Figure 6.10. The outputs of embedded-adder quantizer are connected to the inputs of the regenerative latches which evaluate the polarity of outputs, and the regenerative latches transfer data to the SR latches which sample the evaluated data when ϕ_C becomes “LOW”.

The last thing we need to consider is the offset voltages of the quantizer because the offset sampling phases are not allowable for the proposed quantizer to double the

sampling rate. Since the precharge transistors M_{PD1} and M_{PD2}, turn off during the evaluation phase (ϕ_c="HIGH"), the offsets of comparators are only decided by the current differences of input pairs. The circuit of Figure 2.8 was used to simulate the offset voltage. Common-mode voltages are forced on the input transistors, M_{I1} to M_{I8}, except the transistors connected U_p and U_n. After the output polarity of adder is set to one side, it does not change a lot because the outputs drop to ground together within very short time. Hence, DC simulation was done even though the proposed scheme has dynamic operation. Since the input voltages are applied to the smallest transistors, the Monte-Carlo simulation result of Figure 6.11 shows the worst-case offset voltage of the adder. 3σ threshold variation is assumed for all transistors, and hence the standard deviation 13.4mV represents 95-percent probability. This value is smaller than one half of least significant bit voltage, and hence comparators do not require debubbler circuits which increase the delay of the feedback path.

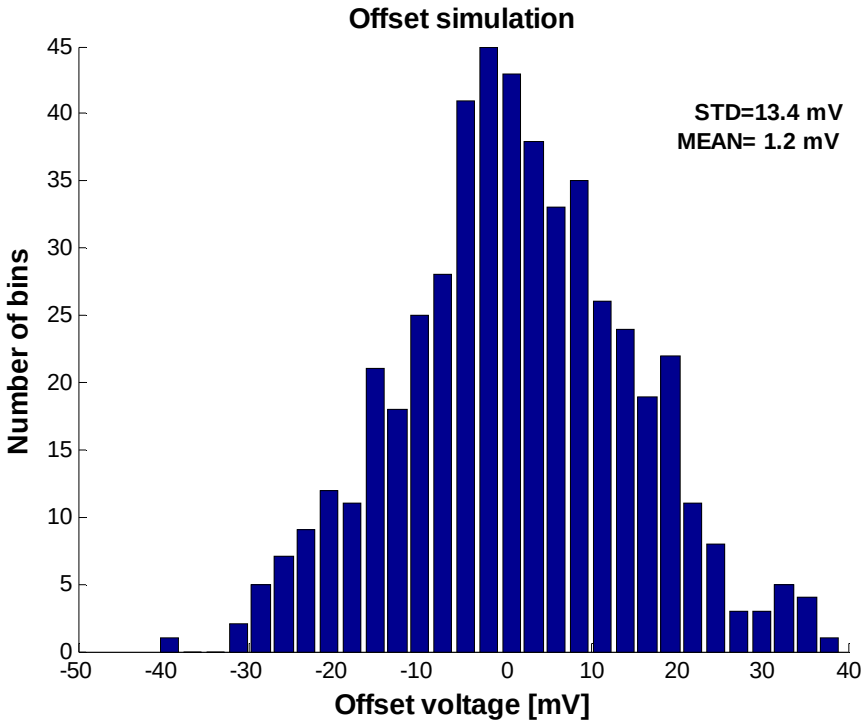


Figure 6.11: Monte-Carlo simulation result of Figure 2.8

6.3. Scrambler

The main issue of scrambler design is the minimization of the delay time between the output of quantizer and the input of DAC. Four blocks which increase the critical delay are shown in Figure 6.12. They are the comparator, the buffer, D-flip-flop (D-FF), and the DEM. Since an embedded-adder quantizer is used for the comparator to minimize power, the circuit delay is fixed by the process, and it cannot be changed a lot. The buffer delay can be optimized by increasing sizes of the transistors, and hence this delay is only process-dependent. However, the D-FFs and the DEM have structural choice to achieve minimum delay. The D-FF can be replaced by a latch, which eliminates the propagation delay of the slave-latch of D-FF. The DEM delay is minimized by selecting the appropriate structure which was presented in Chapter 4. SPECTRE simulation results are summarized in Table 6.2 with the delay reduction techniques. The propagation delay of the synthesized DEM [49] is 900ps. It is reduced to 52ps by using improved SeDWA. A simple latch circuit reduces the 52ps delay. With these two techniques, the integration time is increased by 900ps, which is almost 30 percent of the one sampling period. These delays were simulated without metal parasitics, and will be increased after parasitic extraction.

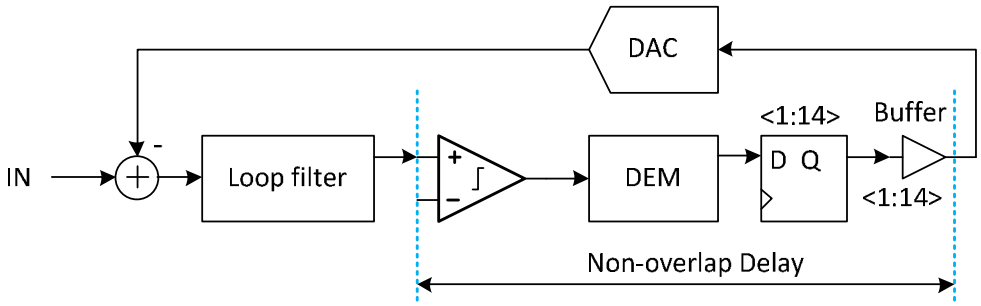


Figure 6.12: A modulator block diagram with the detailed blocks placed at the critical delay path

Table 6.2: Summary of critical path delays

Special Technique	Delay [ns]				Time [ns]	
	Comparator	DEM	D-FF/latch	Buffer	Total Delay	Integration
Synthesized DEM	0.648	0.900	0.215	0.035	1.798	1.327
Improved SeDWA	0.648	0.052	0.215	0.035	0.950	2.175
Improved SeDWA and latch	0.648	0.052	0.163	0.035	0.898	2.227

6.4. Clock Generator

Figure 6.13 shows the timing diagram of the implemented ADC. The clock phases of sampling networks are ϕ_1, ϕ_2, ϕ_{1d}, and ϕ_{2d}. The non-delayed clocks ϕ_1 and ϕ_2 sample the input data in 0.1ns advance of the delayed-clock falling edge. Integration and sampling times are assigned as 2.225ns. ϕ_C is the clock of comparators (adders). The comparators quantize the input data when ϕc goes "HIGH", which is 0.9ns ahead of sampling-clock rising edge. The resetting clock is ϕ_R which discharges DAC capacitors. The nonoverlap times between ϕ_R and delayed sampling clocks are set to 0.1ns. ϕ_D and ϕ_{Dd} are the double-sampling clock and its delayed version, respectively. Their high durations are same as at the sampling clocks'.

These clocks and timing requirements can be realized with the schematic of Figure 6.14, which is a SR-latch-based clock generator [14]. Inverting and noninverting digital delays are used to program sampling time, comparator clock width, delayed sampling clock, nonoverlap time, and reset pulse width. The clock buffers follow the outputs of clock generator to drive the loaded transistors and the parasitic capacitors.

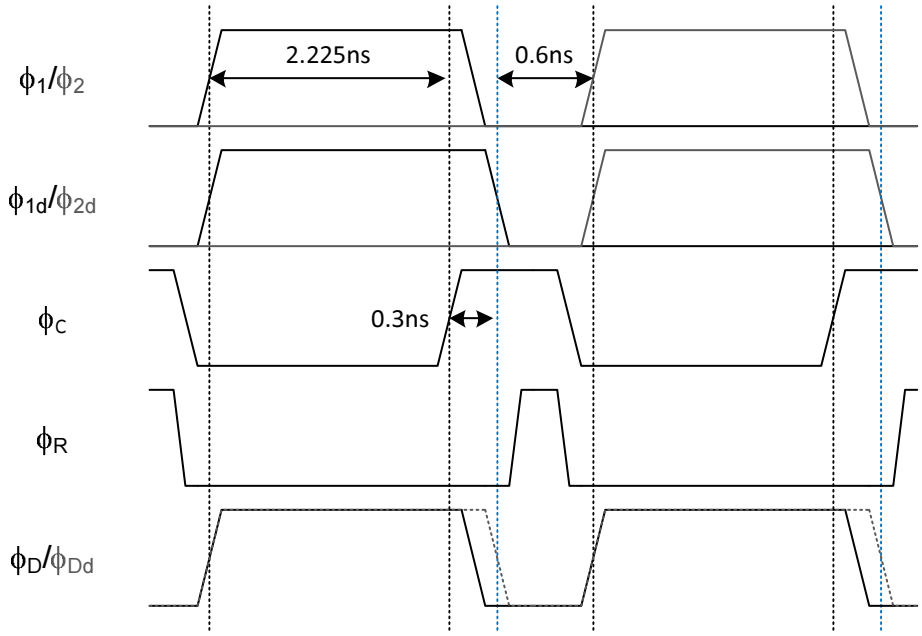


Figure 6.13: Timing diagram of the implemented ADC

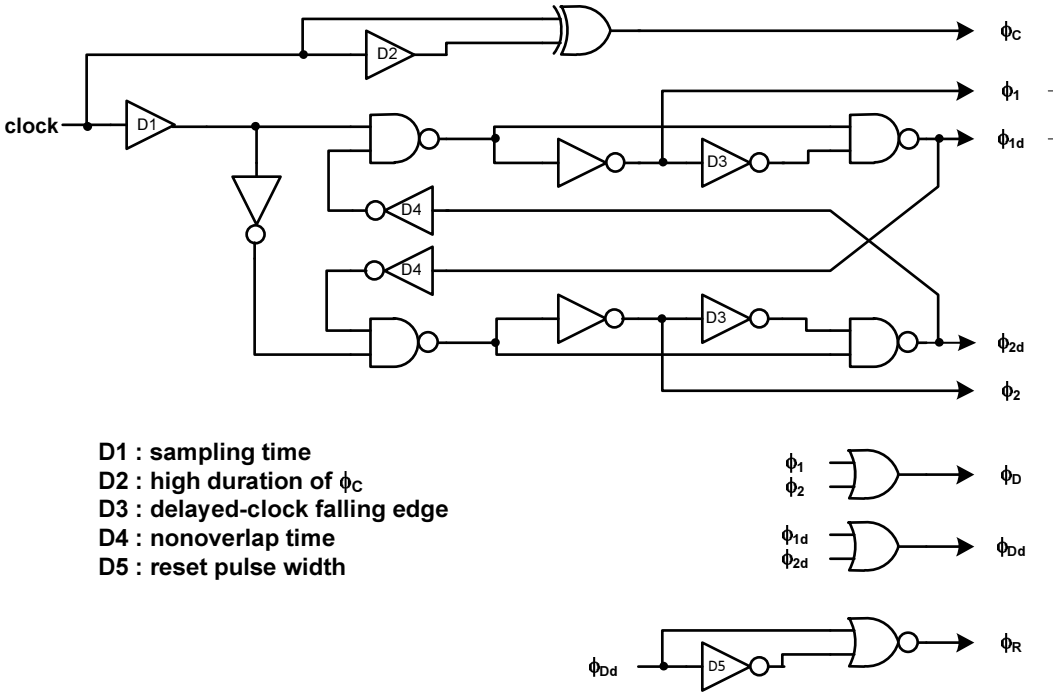


Figure 6.14: Schematic of clock generator

6.5. Bonding Wire Parasitics

Since we are dealing with high frequency operation, any clock noise can be a cause of performance degradation due to the bonding wire inductance. The estimated

length of the bonding wires is around 5mm. This can be simply modeled as a series connection of inductance and resistance, as shown in Figure 6.15. The 35 ohm resistor comes from on-chip metal routing from the pad to the ADC input. Figure 6.16 shows SPECTRE simulation result with the model of Figure 6.15 and a differential version of Figure 6.1. This result shows 2.4dB SNDR degradation compared with the result of Figure 6.9.

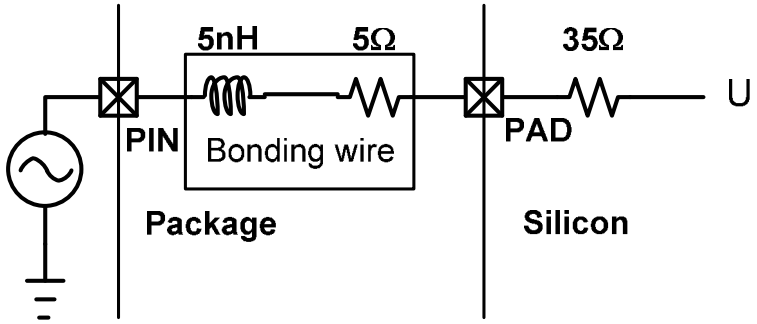


Figure 6.15: Parasitic modeling of input signal path

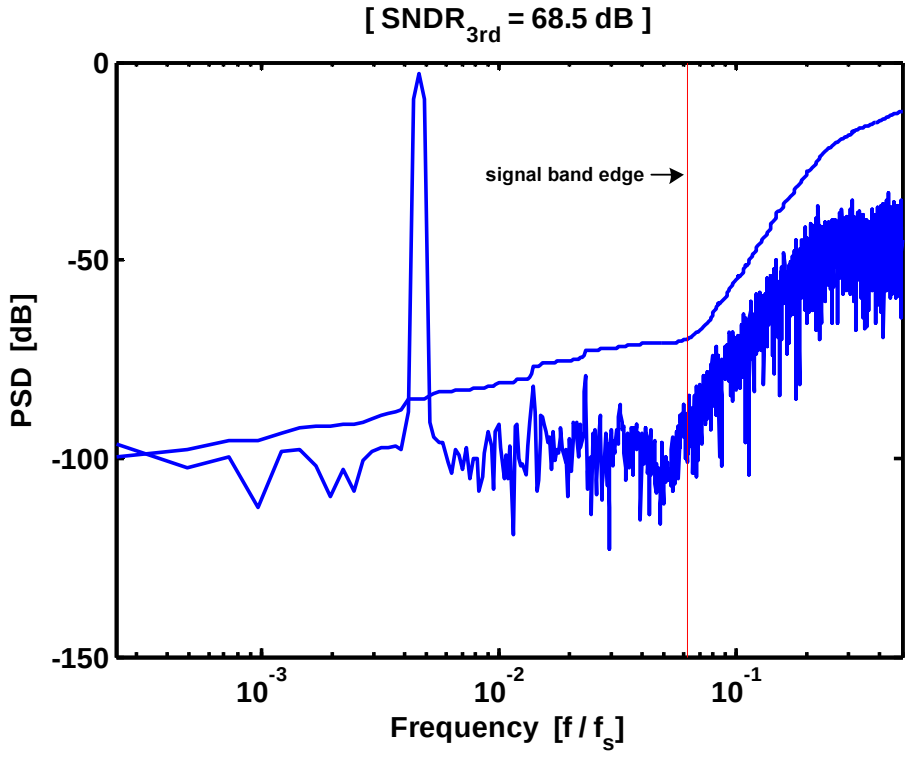


Figure 6.16: SPECTRE simulation result with the circuits of Figure 6.1 and 6.14

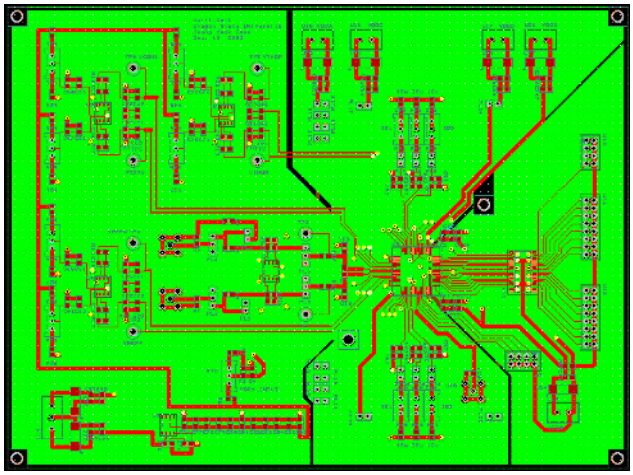
CHAPTER 7. EXPERIMENTAL RESULTS

The test environment and the board design are presented in this chapter. The layout problems of small sampling capacitors are studied here by example layout cases. The measured result and the comparison with previous works are also shown in this chapter.

7.1. Test Environment

The test board was designed as shown in Figure 7.1. The top layer does not have metal fill, to reduce the parasitic capacitance. Second and bottom layers are filled by ground potential metal, and the third layer is filled by VDD potential metal. All important signals run in the top and bottom layers to guarantee programmability. Power decoupling capacitors of 0.1μF and 1μF are placed nearby the device-under-test (DUT). The power connections on the board have 47μF, 1μF, and 0.1μF capacitors to decouple power supply noise. The left side has reference generators with buffers and input signal buffers. The power supply connections and opamp bias controls are placed at the top. Clock and opamp bias controls are placed at the bottom. Digital output powers and signal connections are on the right side of the board. DUT is placed at the slightly right side of center.

Figure 7.2 shows the test setup. Figure 7.3 represents the block diagram of the test setup. RF signal generator is used to clock the DUT and an Audio Precision instrument was used for input signal sources. A logic analyzer captures the outputs of DUT. Power supplies have the potential of ±5V, GND, and 1.8V.



Fill	
Top	No fill
2nd	GND
3rd	VDD
Bottom	GND

Figure 7.1: The top view of PCB layout design

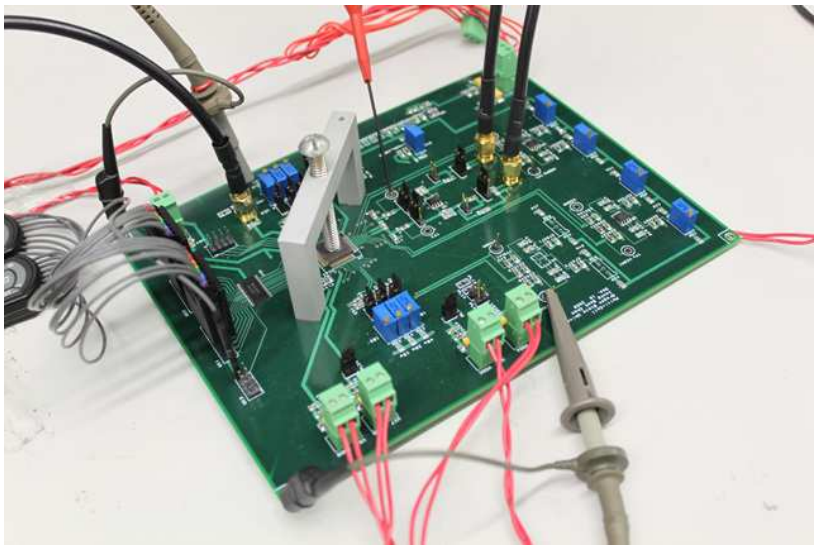


Figure 7.2: Test setup

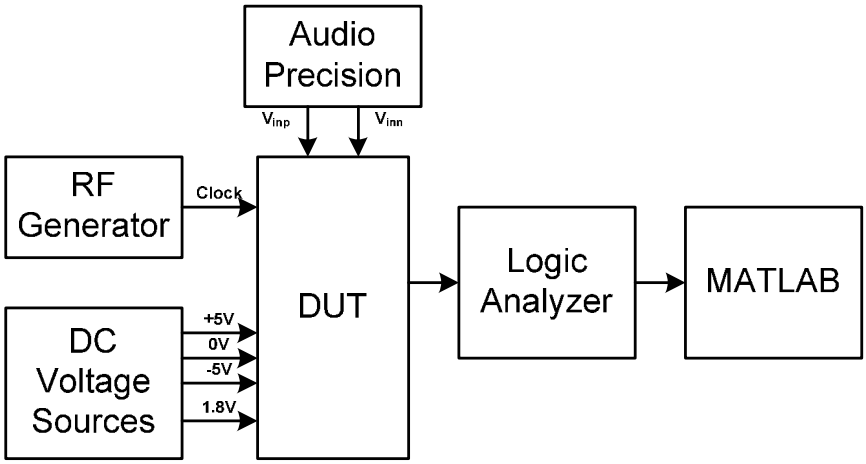


Figure 7.3: The block diagram of test setup shown in Figure 7.2

7.2. DAC Routing Mismatch

For the first implementation, the post-layout simulation was skipped to catch up the shuttle schedule. It brought a problem which increases noise floor. Parasitic extractions with STAR-RC and post layout simulations with HSIM were executed to find the main cause of high noise floor. These simulation results indicate that the layout mismatch of the first stage DAC degrades the performance of whole modulator. Thick black lines of Figure 7.4 are the metal connections between DAC capacitors and switches. All connections have different lengths. The schematic of the first integrator with DAC parasitics is presented in Figure 7.5. The DAC capacitors connected to positive opamp input are omitted.

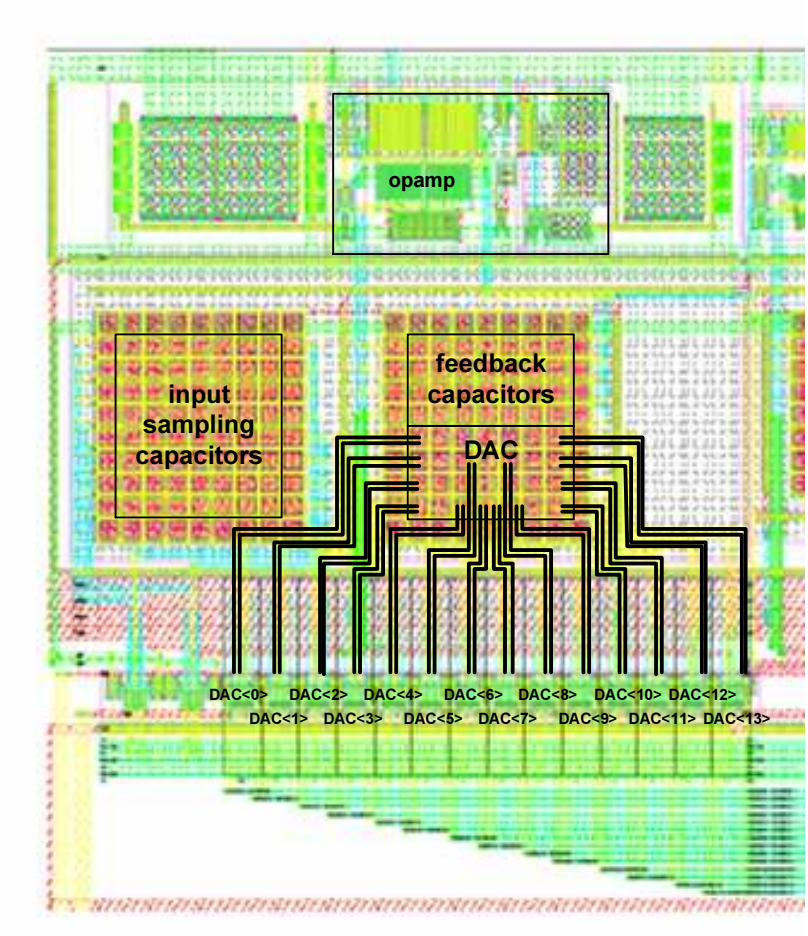


Figure 7.4: First stage layout of the modulator

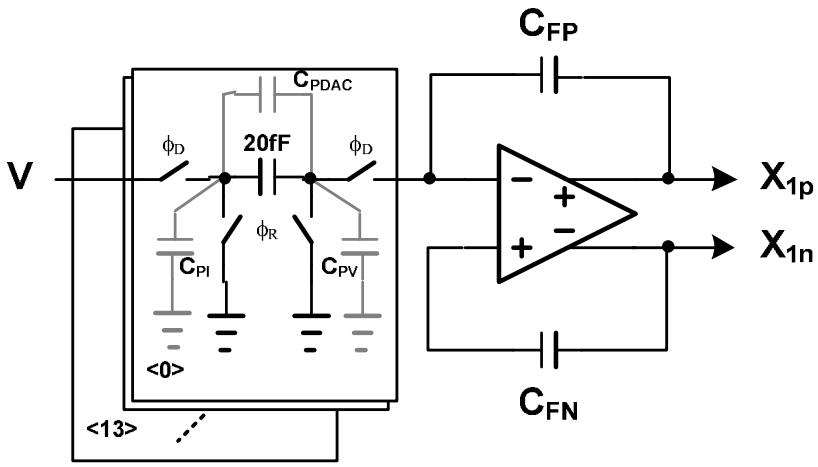


Figure 7.5: First stage integrator with DAC parasitic capacitors.

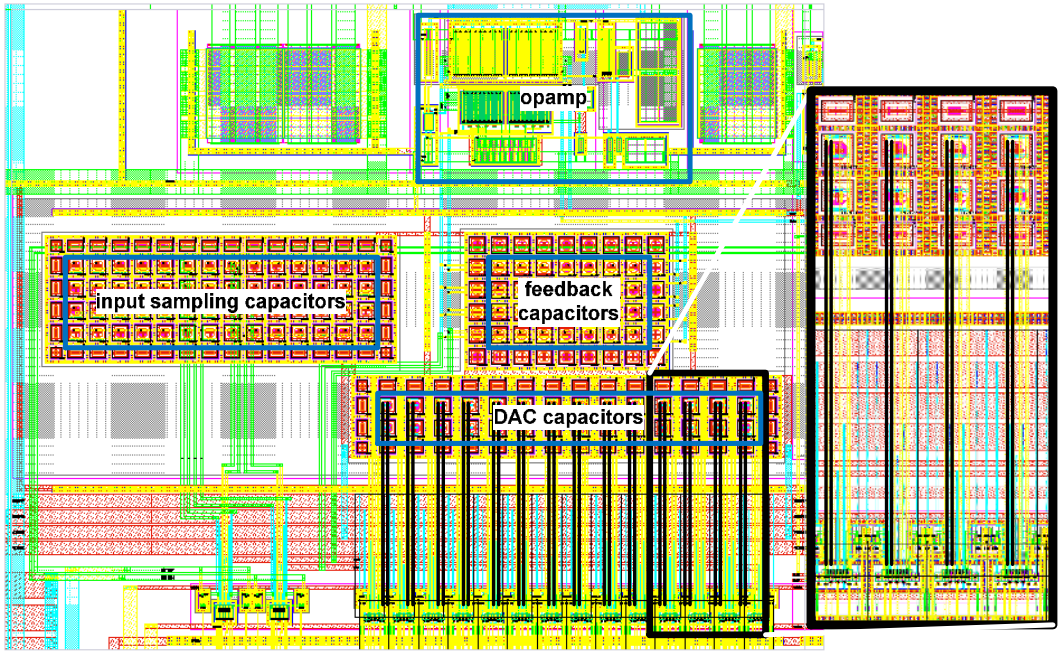


Figure 7.6: First stage layout of revised DAC

For the high-resolution modulator design, these parasitics are very small compared with the unit capacitors, and hence it works like the mismatch of DAC capacitors which can be shaped by DWA. However, this is not true with 20fF DAC unit capacitors of low resolution wide bandwidth design. Parasitic capacitances vary

with the routing distance and the ranges of C_{PDAC}, C_{PI}, and C_{PV} are 4~6.9fF, 8.4~14.6fF, and 11.1~15.8fF respectively. The maximum capacitance of C_{PDAC} is around one third of DAC unit capacitor, and it has big difference from the minimum capacitance to the maximum capacitance. Figure 7.6 shows the revised layout of Figure 7.4. It presents matched connections between all DAC capacitors and switches and the distances of traces become short to reduce the parasitic capacitance. The values of C_{PDAC}, C_{PI}, and C_{PV} are reduced to 5.3~5.5fF, 7.7~8.0fF, and 10.4~10.8fF, respectively. Since the layout patterns are matched perfectly, the parastics need to be matched well. However, they have a small variance because of the accuracy of extraction tool. The post-layout simulation shown in Figure 7.7 is done by HSIM with cross-coupled parasitic capacitors. The SNDR degrades compared with the circuit simulation result of Figure 6.16, but 34dB improvement achieves from the previous layout of Figure 7.4.

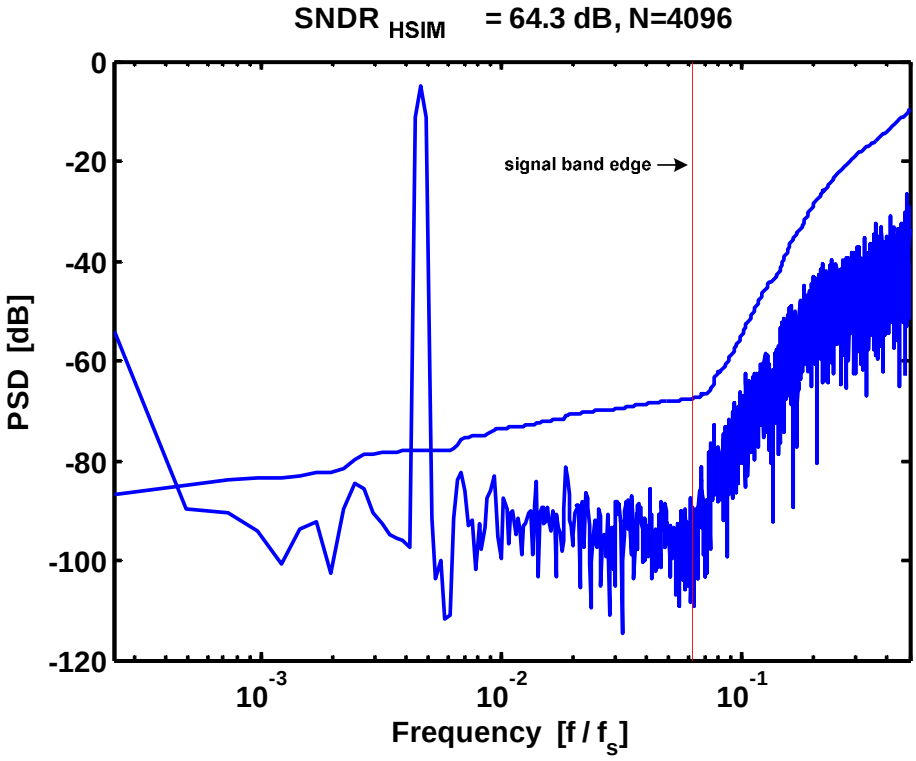
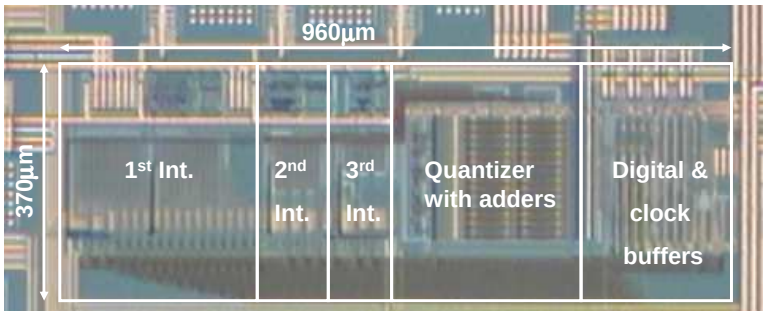


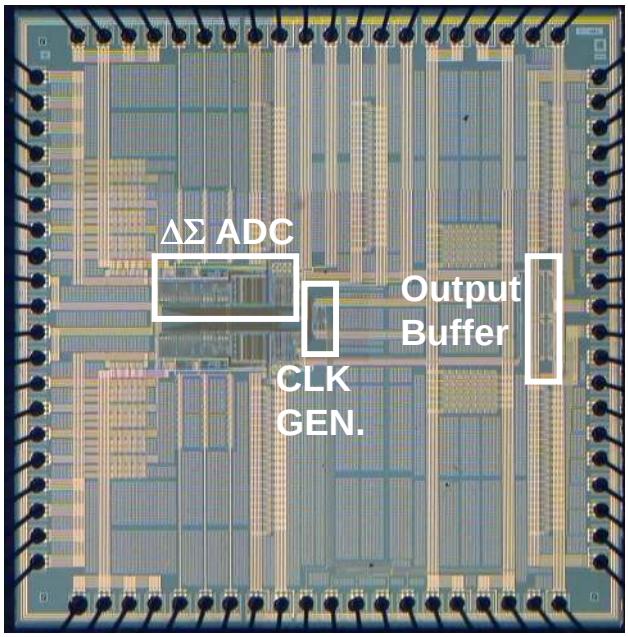
Figure 7.7: HSIM simulation result with cross-coupled parasitic extraction

7.3. Measurement Results

The prototype ADC, fabricated in a double-poly/4-metal 0.18 μm CMOS technology, occupies 0.36 mm^2 of ADC core area. The die photo is shown in Figure 7.8. Figure 7.9 shows the measured output spectrum with a -3.3 dBFS 151.4 kHz input tone. Figure 7.10 shows the measured SNDR and SNR. Unfortunately, the DEM had to be disabled to reduce the loop delay of the modulator, and hence tones of Figure 7.9 are generated by mismatch of DAC capacitors. To increase the speed of digital circuit, 1.85V digital power source is used.



(a)



(b)

Figure 7.8: Die micrograph of (a) ADC core and (b) implemented IC

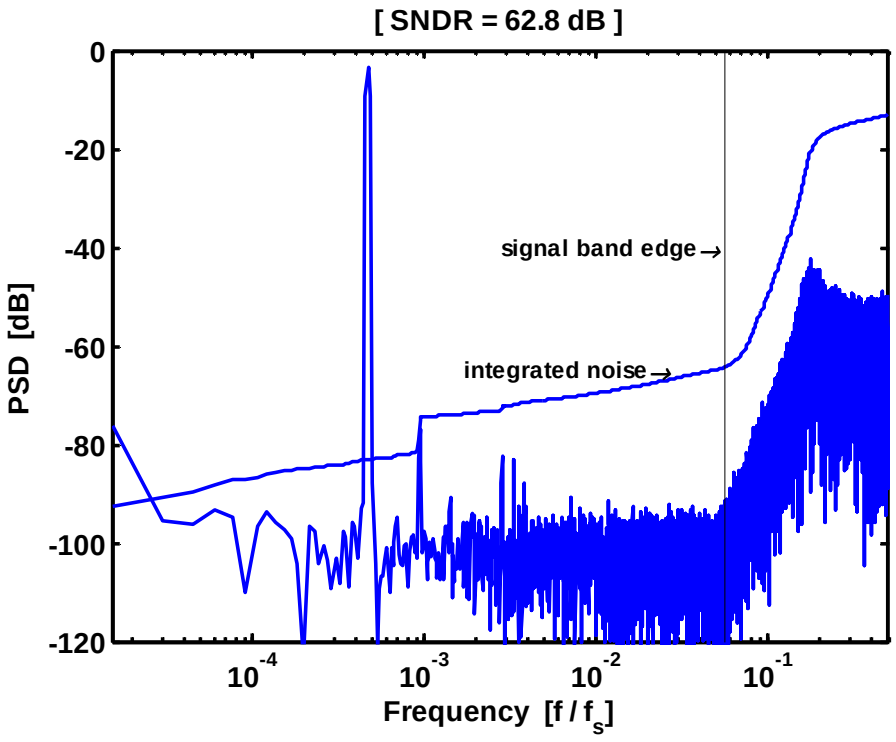


Figure 7.9: Power spectral density with a -3.3dBFS sine wave input.

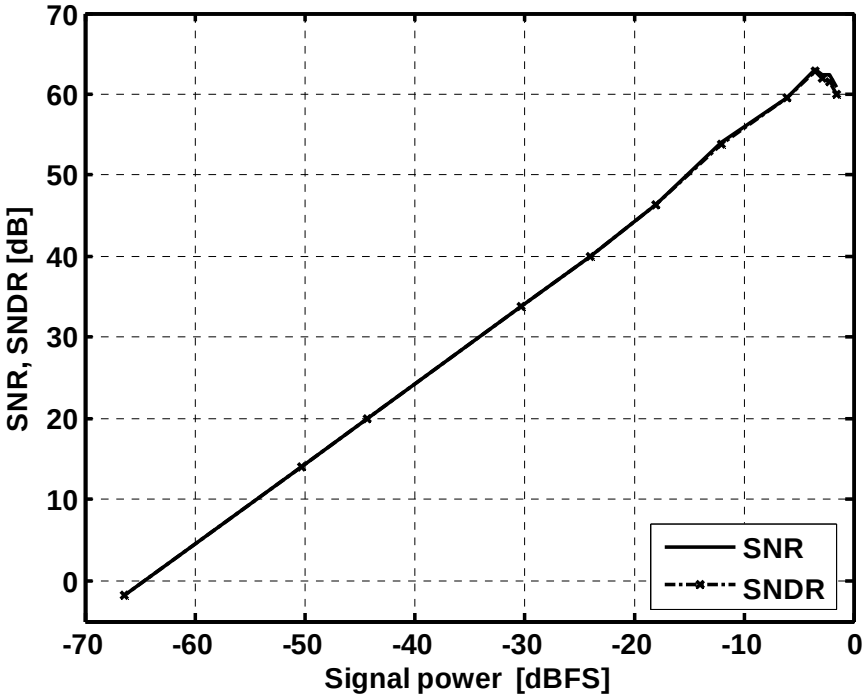


Figure 7.10: Measured SNR and SNDR versus input amplitude.

The test results are summarized in Table 7.1. The peak SNDR is 63 dB with a signal bandwidth of 20 MHz and the measured power consumption is 16 mW. The figure-of-merit FoM = $P/(2*BW*2^{ENOB})$ is 0.35 pJ/conv. step. Table 7.2 shows the comparison with delta-sigma ADCs which have 20 MHz bandwidth. Although the FoM number is little higher than the state of the art, the power of the implemented IC can be reduced by technology scaling, because more than 70 percent of power consumption is in the dynamic circuitry.

Table 7.1: Summary of measured performance

Clock frequency	160MHz
Sampling frequency (DS)	320MHz
Signal bandwidth	20MHz
OSR	8
Dynamic range	64dB
Peak SNR, SNDR	63dB, 63dB (-3.3dBFS)
Power consumption	16mW 8mW (A)/8mW (D)
Power supply	1.8V (A)/1.85V (D)
Process	0.18 μm 2P4M CMOS
FoM	0.35 pJ/conv. step

Table 7.2: Performance Comparison between 20MHz-bandwidth ADCs

Author/year	Type	Process [μm]	FoM [pJ/conv. Step]
Xuefeng/07 [50]	CT	0.18	0.87
Dhanasekaran/09 [51]	CT	0.065	0.34
Park/09 [52]	CT	0.13	0.34
Mitteregger/06 [53]	CT	0.13	0.12
Malla/08 [54]	DT	0.09	0.27
Paramesh/06 [55]	DT	0.09	1.60
Proposed/10	DT	0.18	0.35

CHAPTER 8. NOISE-COUPLED DELTA-SIGMA ADC WITH ZERO OPTIMIZATION

A zero optimization technique with noise coupling is proposed in this chapter. It uses a first-order modulator, second-order noise coupling and a resonator to increase the SQNR. MATLAB simulations verify that the performance of the proposed scheme is comparable to that of a third-order modulator which has zero optimization, but the proposed system is smaller to implement. It also has lower power consumption.

8.1. Introduction

Wideband delta-sigma modulators have difficulty for high SQNR because of low OSR requirement which comes from the high clock frequency and given process, as discussed in the previous chapters. Zero optimization [14] is one of the best ways to increase the SQNR without having any major disadvantage. However, there is a problem which comes from small value of the coefficient of the resonator. For the third-order modulator shown in Figure 8.1 and an OSR of 16, the coefficient required to place zeros at the optimal points is 0.022. Such small value requires additional power consumption and large area compared with the case without zero optimization, because we scale down the capacitor value from the first integrator, which is connected to input signal to following integrators. If we change the coefficient as the part of any branch, small size problems will not be a concern any more. This can be done with noise-coupled modulator [56].

8.2. The Proposed Scheme

Noise coupling is an efficient technique to increase the order of the modulator by adding and/or subtracting delayed quantization noises which make shaped noise

instead of quantization noise itself at the output of quantizer without any additional opamp. Previous work [56] shows first-order coupling with a second-order modulator. However, for [56], it is hard to use zero optimization, because the resonator requires at least second-order block and a local feedback branch of zero placement which should go to the first integrator. Hence, the total power consumption is increased by the small resonator coefficient. We need larger area and more power consumption by increasing capacitor sizes. To remedy this problem, we use a first-order low-distortion modulator [4] with second-order noise coupling. The proposed scheme is shown in Figure 8.2. Noise coupling branches which have the transfer function of $(-2z^{-1}+z^{-2})$ go to the input of the adder. For this case, we can simply put the resonator coefficient in parallel with the feedback branches, and merge them as shown in Figure 8.3. Now, there is no small coefficient, i.e. capacitor which increases thermal noise. The NTF of Figure 8.3 is

$$(1-z^{-1})(1-1.978z^{-1}+z^{-2}) \qquad (1).$$

The first term comes from the modulator itself, and the second term which moves the zeros from low frequency to the edge of the signal band, is obtained by noise coupling.

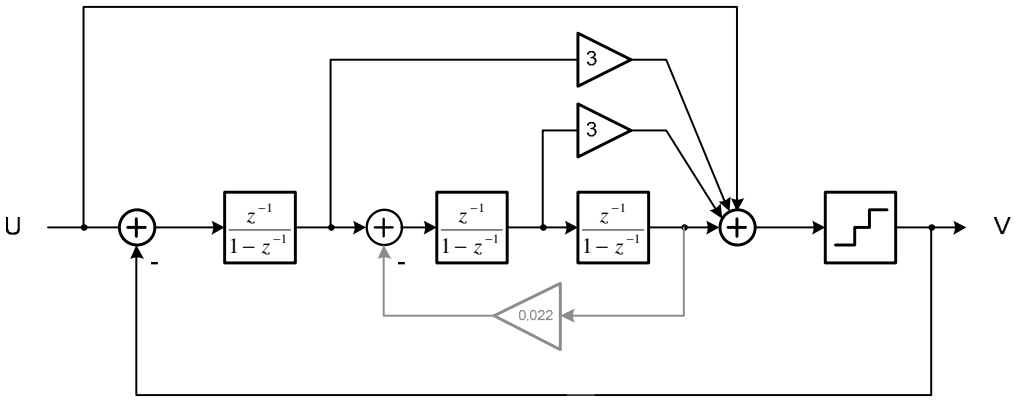


Figure 8.1: A third-order low-distortion delta-sigma modulator with zero optimization when OSR is 16

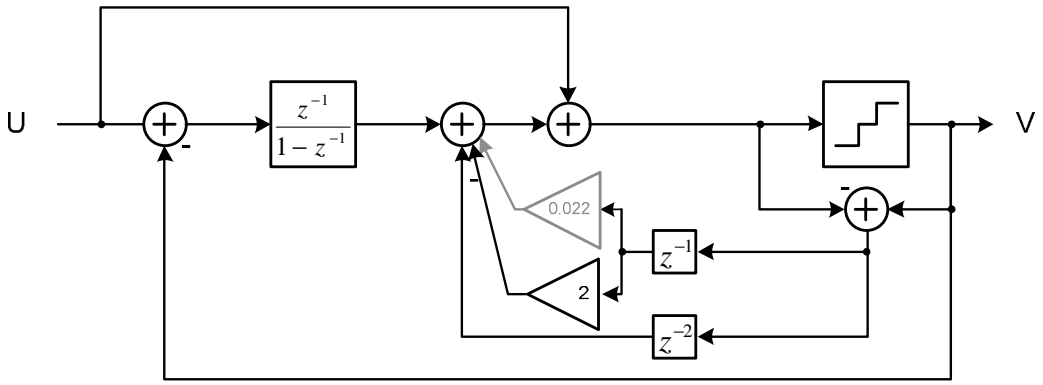


Figure 8.2: A proposed third-order ΔΣ modulator which has zero optimization at the noise-coupled branches

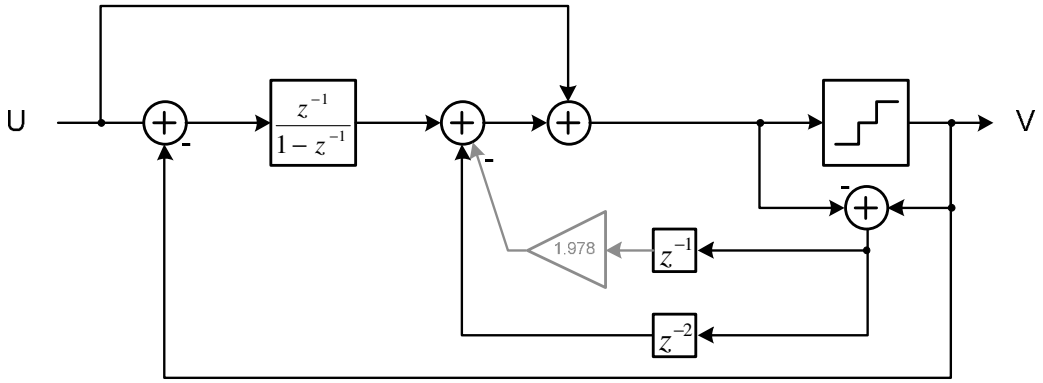


Figure 8.3: A proposed third-order delta-sigma modulator which has zero optimization with the merged branches

8.3. Branch Optimization

By transforming the noise coupling branches of Figure 8.3, we can increase the feedback factor of the adder which will be merged to second integrator later on. Hence, the power consumption can be optimized. First, we can separate the analog paths and digital paths of noise coupling branches, as shown in Figure 8.4. One of z^{-1} branches of analog paths can be used to build an integrator. However, by doing this, coefficients of branches are not matched between analog and digital paths. To match the number of braches, digital subtraction is done before the adder input. This digital subtraction of z^{-1} branch from z^{-2} branch is shown in Figure 8.5. When we

design real circuit, we can increase the feedback factor of the second integrator and reduce the power consumption, by sharing sampling capacitors between the branches with dashed lines and thick lines. There is additional power saving for noise-coupled modulators, because the number of opamps can be reduced [56]. Figure 8.5 has two fewer opamps than the modulator of Figure 8.1.

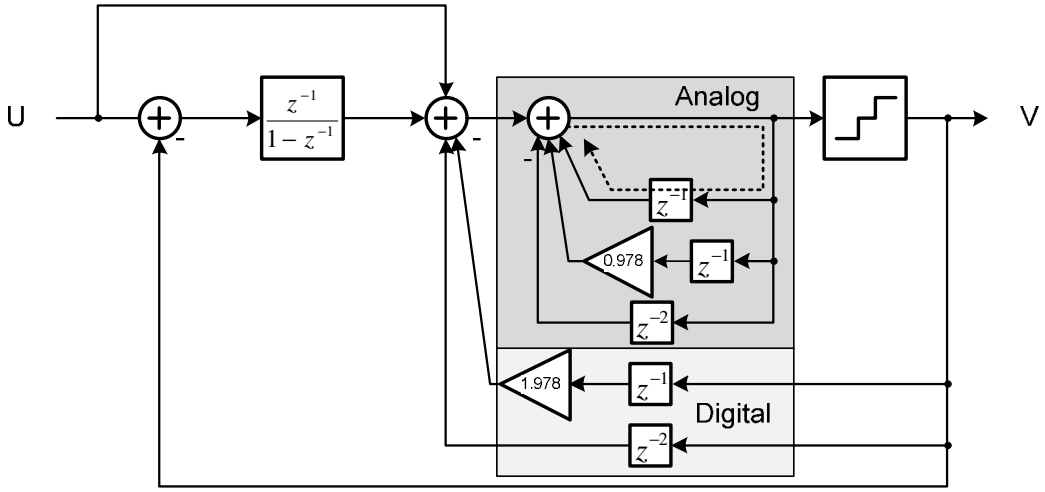


Figure 8.4: A proposed third-order ΔΣ modulator with path separation of analog and digital branches

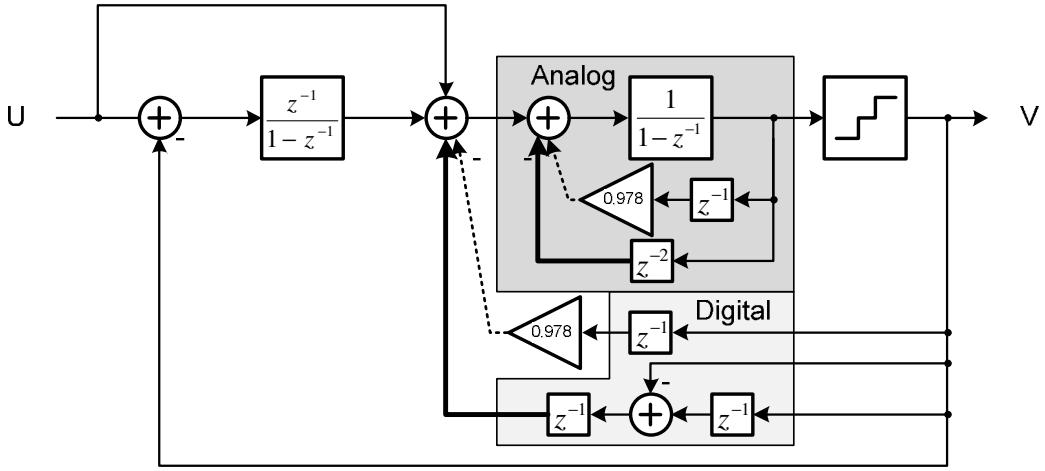


Figure 8.5: A proposed third-order ΔΣ modulator with path separation with optimized analog and digital branches

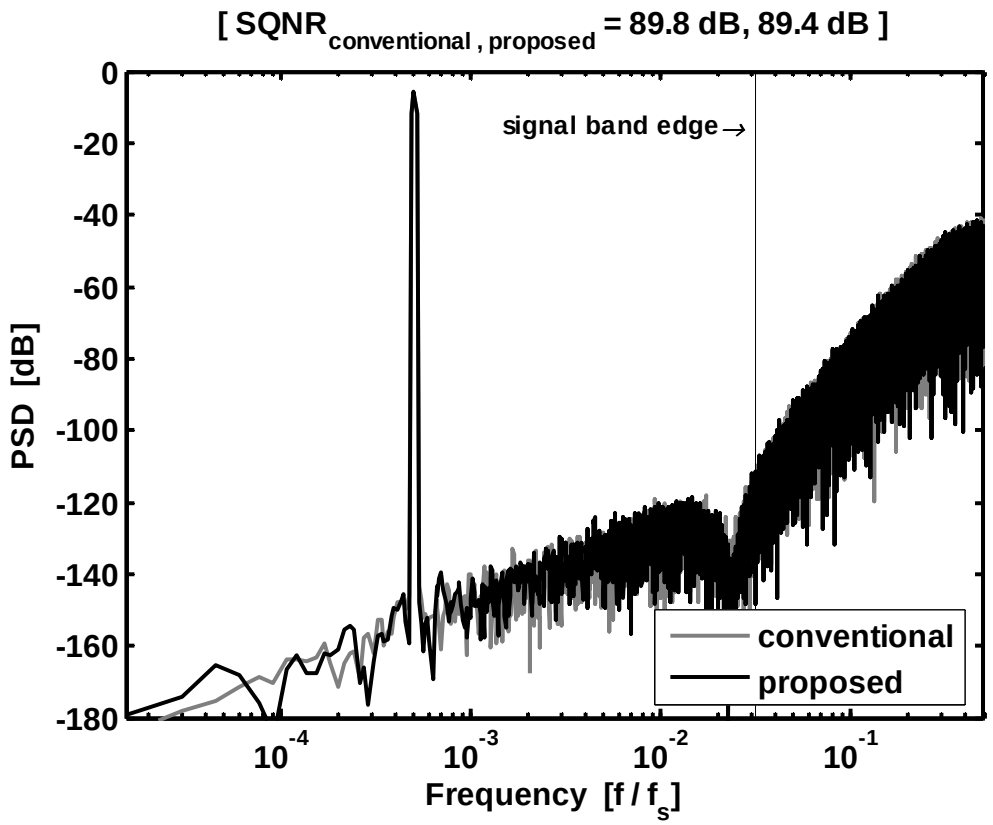


Figure 8.6: PSDs at the output of the ΔΣ ADC of Figure 8.1 and 8.5

8.4. Simulation Results

Third-order modulators were simulated using MATLAB, with a -6dB input sine wave, an OSR of 16, and a 15-level quantizer. 65,536 data points were used. Figure 8.6 shows the power spectral densities of modulators shown in Figure 8.1 and Figure 8.5. Their SQNR was comparable. Capacitor sizes are summarized in Table 8.1. The conventional modulator is the modulator of Figure 8.1, and the proposed modulator is the modulator shown in Figure 8.5. For the case of same-sized input sampling capacitors, the conventional scheme has very small capacitors which are not allowed for most CMOS processes. If we use the proposed scheme, the small capacitor is a part of transfer function and is easy to implement.

Table 8.1: Comparison of different types of zero optimization schemes with second integrator's sampling and resonator capacitors

	sampling capacitor [fF]	resonator capacitor [fF]
conventional	170	3.7
proposed	170	166.3

8.5. Summary

A novel zero-optimization technique for noise-coupled modulators was proposed. It has lower power consumption than earlier zero-optimization schemes; also, the resulting circuit is smaller than the conventional one.

CHAPTER 9. CONCLUSIONS

Low-power and wide-band techniques were proposed in this dissertation. An embedded-adder quantizer which merges the adder of the modulator and the preamplifier of the quantizer were proposed to achieve low power consumption. Numerous double-sampling schemes were studied, and novel schemes were proposed to double the bandwidth of modulators without noise folding effect. A high speed DEM which alternates two sets of reference inputs of comparators was proposed to reduce the timing delay without idle tones. The multi-cell architecture was studied for low OSR modulators to achieve higher performance than the single-cell approach.

A prototype IC was implemented with 0.18 μm double-poly/4-metal CMOS process. The peak SNDR is 63 dB with 20 MHz signal bandwidth and 320 MHz sampling clock. The measured power consumption is 16 mW, and the figure-of-merit FoM = $P/(2*BW*2^{ENOB})$ is 0.35 pJ/conv. step. 71 dB of SNDR is achievable by applying an 8-cell architecture with the implemented single-cells. Since more than 70 percent of power is in the dynamic circuitry, the power consumption can be reduced further with the advanced processes. Measurement results show that the proposed ideas are suitable for low-power and wideband delta-sigma modulators which have low OSR.

For future research work, a second-order noise-coupled modulator with zero optimization is proposed to eliminate integrators and hence to reduce power consumption. This architecture makes easier implementation of small feedback capacitors for high OSR modulators.

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