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Novel Ternary Adder and Multiplier Designs Without Using Decoders or Encoders

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ABSTRACT Multiple-Valued Logic systems present significant improvements in terms of energy consumption over binary logic systems. This paper proposes new ternary combinational digital circuits that reduce energy consumption in low-power nano-scale embedded systems and Internet of Thing (IoT) devices to save their battery consumption. The 32 nm CNTFET-based ternary half adder (THA) and multiplier (TMUL) circuits use novel ternary unary operator circuits and implement two power supplies Vdd and Vdd/2 without using any ternary decoders, basic logic gates, or encoders to minimize the number of used transistors and improve the energy efficiency. Extensive simulations (over 160) of the proposed designs in terms of PVT (Process, Voltage, Temperature) variations, noise effect, and scalability studies, along with several benchmark designs using HSPICE simulator, prove the significance of the proposed circuits to decrease the power-delay product (PDP), improve the robustness to process variations, and the noise tolerance. The obtained results show the superiority of the designs in a reduction between 32% and 74% in transistors count and between 18% and 99% in PDP compared to the most recent works.

INDEX TERMS Carbon nano-tube field effect transistors (CNTFET), Noise immunity curve (NIC), PVT variations, ternary logic circuits, unary operators.

I. INTRODUCTION

Two major problems are facing the embedded systems and nano-scale circuits currently, which are (1) the CMOS (Complementary Metal Oxide Semiconductor) transistor, and (2) the binary circuits. Solutions can be done by using CNTFET (Carbon Nano-Tube Field Effect Transistor) instead of CMOS transistor and using MVL (Multiple-Valued Logic) circuits instead of binary circuits.

(1) The CMOS faces significant complications in nanotechnology circuits such as tight channel-effects and high current leakage [1]. Therefore, many scientists proposed various alternative solutions in the transistor technologies like FinFET (Fin Field-Effect Transistor), Spin-wave, Single-electron devices, CNTFET. Among all different transistor technologies, CNTFET has a higher performance [2].

(2) The binary circuits require high energy consumption. Whereas, MVL circuits reduce the consumption of energy because the MVL digit can hold over two states of data.

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The ternary system (Low: 0 (0V), Middle: 1 (Vdd/2), and High: 2 (Vdd)), which is designed and implemented in this work, has a higher performance system among all known base systems [3].

Many researchers implement MVL in several applications like Machine learning and IoT [4], Algorithm [5], Data transmission [6], Healthcare [7], Combined with binary circuits [8], Resistive RAM or Memristor [9], [10], Ternary Converters [11], and ternary circuits [12], [13].

However, the challenge in the ternary circuit is: How to obtain the logical state 1 (Vdd/2) from one power supply (Vdd)?

Many researchers inserted two resistors (which increase the size of the circuit and are not recommended in VLSI circuits) and others inserted two diode-connected transistors acting like resistors to solve the problem size in VLSI.

These two resistors or two diode-connected transistors are necessary to create a voltage divider to generate logic 1 (Vdd/2). But the results showed a huge rise in the power dissipation because of the direct current path from the power supply (Vdd) to the ground [14]. Therefore, one of the advantages of this paper is the use of (Vdd/2)

TABLE 1. Summary of literature review.

Techniques	Ref.	Year	Details	Transistor count THA	Transistor count TMUL	Limitation
Conventional Design	[15]	2011	- TDecoder (16 transistors) - Binary logic gates - Ternary encoder	136	100	- High Transistors count - High PDP
	[16]	2016	- TDecoder (10 transistors) - Binary logic gates - Ternary encoder	112	86	
	[17]	2017	- TDecoder (10 transistors) - Binary logic gates - Ternary NAND	112	76	
	[18]	2020	- TDecoder (16 transistors) - Binary logic gates - Ternary encoder	108	-	
	[19]	2019	- TDecoder (9 transistors) - Basic logic gates - Two power supplies (Vdd and Vdd/2)	85	61	- High Transistors count - Medium PDP
Cascading TMUXs	[20]	2018	- TMUX (28 transistors)	168	112	- High Transistors count - High PDP
	[21]	2020	- TMUX (15 transistors) - Two power supplies (Vdd and Vdd/2)	90	-	- High Transistors count - Medium PDP
Unary Operators & TMUXs	[22]	2016	- Unary Operators - TMUX (15 transistors)	39	26	- Medium Transistors count - Medium PDP
	[23]	2017	- Unary Operators - TMUX (18 transistors)	64	58	
	[14]	2018	- Unary Operators - TMUX (22 transistors) - Two power supplies (Vdd and Vdd/2)	54	23	
	[24]	2019	- Unary Operators using Binary NAND - TMUX (18 transistors)	76	-	
	[25]	2020	- Unary Operators using cascading TMUX - TMUX (12 transistors)	48	30	
	[26]	2020	- Unary Operators - Two power supplies (Vdd and Vdd/2)	-	60	
Synthesis	[27]	2020	- Modified Quine-McCluskey Algorithm	48	-	- High PDP
Cascading TGs	[28]	2017	- Lot of cascading Transmission Gates	39	34	- Medium Transistors count
	[29]	2020	- Lot of cascading Transmission Gates	50	38	- Medium PDP
RRAM	[30]	2020	- RRAM	90	62	- High PDP
Mixed	[31]	2017	- TDecoder (8 transistors) - Special transistors arrangements - Ternary encoder	94[1] 66[2]	-	- Medium Transistors count - Medium PDP
	[32]	2018	- TDecoder (10 transistors) - Special transistors arrangements	64	-	
	[33]	2021	- Ternary encoder - Special transistors arrangements	60	-	
Unary Operators & TGs	[34]	2020	- Two power supplies (Vdd and Vdd/2) - Special transistors arrangements	34	-	- Low Transistors count - Low PDP

in the designs to eliminate these two diode-connected transistors.

This paper utilizes the ternary unary operators (see Section II), CNTFET transistor, transmission gates and applies dual-voltages (Vdd, Vdd/2) in the designs to decrease the PDP of the proposed THA and TMUL. This technique is used to save battery consumption of the nano-scale embedded systems and Internet of Thing (IoT) devices.

A. LITERATURE REVIEW

There are a large number of publications that presented different THAs and TMULs based on CNTFET. This paper describes the importance and the latest ones, as summarized in Table 1.

Different methodologies have been proposed to design ternary logic circuits, which are described as follows:

(1) Use of the ternary conventional design by utilizing the Ternary Decoders (TDecoder) to make the conversion from the ternary inputs to intermediate binary bits, then using binary logic gates, and finally using the ternary encoders to get the final ternary outputs such as:

Authors of [15]–[18] designed THAs with (136, 112, 112 CNTFETs, and 108 GNRFET (Graphene Nano Ribbon FET, which is derived from CNTFET)) and TMULs with (100, 86, and 76 CNTFETs), respectively, using the conventional design. Whereas in [19], the authors proposed a THA with 85 CNTFETs and TMUL with 61 CNFTFETs without using ternary encoders by using dual-voltages (Vdd and Vdd/2).

(2) Use cascading Ternary Multiplexers (TMUXs) without using the binary logic gates, and encoders such as:

Authors of [20], [21] represented THAs with (168, 90 CNTFETs) and TMUL with 112 CNTFETs, respectively.

(3) Use ternary unary operators (see Section II) with TMUXs to reduce the transistors count used such as:

Authors of [14], [22]–[26] designed THAs with (39, 64, 54, 48, and 76 CNTFETs) and TMULs with (26, 58, 23, 30, and 60 CNTFETs), respectively, using different designs of unary operators and TMUXs.

(4) Use an algorithm for a logic synthesis but this method will generate a large number of transistors in series, which produced high propagation delays and PDP, such as:

Authors of [27] designed a THA with 48 CNTFETs using a modified Quine-McCluskey and post-optimization algorithms.

(5) Use transmission gates (TGs) in series, special transistors arrangements, or Resistive Random Access Memory (RRAM) such as:

Authors of [28], [29] proposed THAs with (39 and 50 CNTFETs) and TMULs with (34 and 38 CNTFETs) using cascading TGs, which produced higher propagation delays and PDP. In [30], the authors proposed THA with 90 CNTFETs and TMUL with 62 CNTEFTs using RRAM. The authors of [31] proposed two THAs with 94 and 66 CNTFETs and the authors of [32] proposed THA with 64 CNTFETs using TDecoders and special transistors arrangements. Whereas in [33], the authors proposed a THA with 60 CNTFETs using ternary encoders and special transistors arrangments.

Finally, the authors of [34] proposed the lowest energy consumption THA with 34 CNTFETs compared to the designs mentioned above using only unary operators and transmission gates, which is adopted in this paper.

B. CONTRIBUTIONS

The previous designs suffer from a large number of transistors used, high PDP, low robustness to process variations, and/or low noise tolerance.

This paper proposes efficient circuit implementation of THA and TMUL with 35 and 26 CNTFETs using unary operators, transmission gates, and dual-voltages (Vdd, Vdd/2) to get the lowest PDP for saving battery consumption of the embedded systems and IoT devices.

The main contributions of this paper are as follow:

1) The proposed designs do not utilize basic logic gates, TDecoders, and encoders that lead to high transistors count and PDP (compared to [15]–[21]).
2) Use dual-voltages (Vdd and Vdd/2) to disconnect the direct current path from Vdd to the ground that leads to high energy consumption (like [15]–[17], [22], [27]).
3) Use ternary unary operators that can replace the basic logic gates, which significantly reduce the number of used transistors and energy consumption.

So, we reduce the transistors count, decrease the energy consumption, improve the robustness to process variations, and noise tolerance.

II. THE PROPOSED UNARY OPERATORS

This paper uses the Stanford CNTFET model, as shown in Fig.1, which can be found in [35]. However, it is worth to mention that the threshold voltage depends on the carbon nano-tube (CNT) diameter by the following equation (1):

$$V_{\text{th}} = \frac{0.43}{Dcnt} \tag{1}$$

where $Dcnt$ is the CNT diameter.

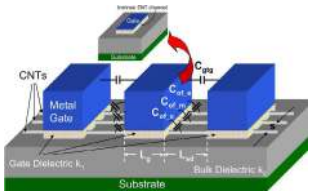


FIGURE 1. Stanford CNFET Model [35].

Table 2 describes the operation of the CNTFET transistor, and the relation between the threshold voltage and the CNT diameter.

TABLE 2. CNTFET Operation with D1 = 1.487 nm and D2 = 0.783 nm.

Type	Diameter	Threshold voltage	Voltage Gate 0V	0.45V	0.9V
P-CNTFET	D1	- 0.289 V	ON	ON	OFF
	D2	- 0.559 V	ON	OFF	OFF
N-CNTFET	D1	0.289 V	OFF	ON	ON
	D2	0.559 V	OFF	OFF	ON

Unary operators of m-valued system are one-input and one-output logic gates [36].

In the binary systems ($m = 2$), there are four (2^2) unary functions (“00”, “01”, “10”, “11”). Whereas in the ternary systems ($m = 3$), there are twenty-seven (3^3) unary functions (“000”, “001”, “002”, . . .,“222”).

To design new THA and TMUL (next section), eight unary functions are needed which are shown in Table 3: Where A is the ternary input, the first unary function A_p is a Positive Ternary Inverter (PTI), the second A_n is a Negative Ternary

TABLE 3. Selected Unary Operators.

Ternary Input A	PTI A_p	NTI A_n	Cycle Operators A^1	A^2	$\bar{A^2}$	Decisive literal A_1	$1 \cdot \bar{A_n}$	$1 \cdot \bar{A_p}$
0	2	2	1	2	0	0	0	0
1	2	0	2	0	2	2	1	0
2	0	0	0	1	1	0	1	1

Inverter (NTI), the third and the fourth functions are the cycle operators, A^1 is $A+1$ and A^2 is $A+2$, whereas the fifth function $\bar{A^2}$ is the complement of A^2. The sixth function A_1 is the decisive literal, and the last two unary functions are $1 \cdot \bar{A_n}$ and $1 \cdot \bar{A_p}$.

We propose novel designs for two unary operators: B_1 is shown in Fig. 2(g) and in Fig. 3(d), and $\bar{A^2}$ is shown in Fig. 3(c). The other six unary operators are presented in [34].

The transistors count comparison of the proposed unary operators to those in [14], [23]–[25] are shown in Table 4.

TABLE 4. Unary Operators transistors count comparison.

	[23]	[14]	[24]	[25]	Proposed	Improvement w.r.t [23]
$\bar{A^2}$	13	-	-	12	4	69.23%
A_1	6	10	12	-	3	50%

III. THE PROPOSED TERNARY COMBINATIONAL CIRCUITS

We propose a THA and a TMUL with 35 and 26 CNTFETs using unary operators and transmission gates.

A. THE PROPOSED TERNARY HALF-ADDER

1-trit THA can add two ternary inputs (A, B) and produces two outputs: the Sum and the Carry, as described in truth Table 5.

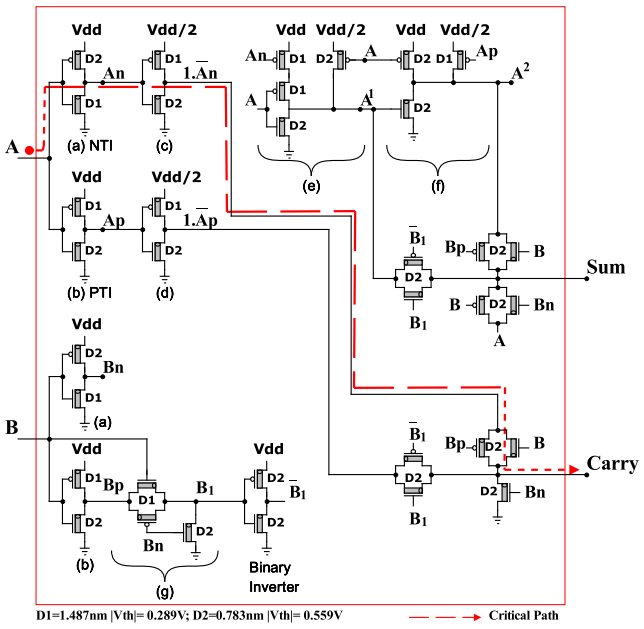


FIGURE 2. The proposed THA with 35 CNTFETs: (a) NTI, (b) PTI, (c) $1 \cdot \bar{A_n}$, (d) $1 \cdot \bar{A_p}$, (e) A^1, (f) A^2, and (g) the proposed B_1. Using Unary operators-based design in Eq. (4).

TABLE 5. The truth table of THA.

Sum

A/B	B_0 (0)	B_1 (1)	B_2 (2)
A_0 (0)	0	1	2
A_1 (1)	1 } **A**	2 } $\mathbf{A^1}$	0 } $\mathbf{A^2}$
A_2 (2)	2	0	1

Carry

A/B	B_0 (0)	B_1 (1)	B_2 (2)
A_0 (0)	0	0	0
A_1 (1)	0 } **0**	0 } $\mathbf{1 \cdot \overline{A_p}}$	1 } $\mathbf{1 \cdot \overline{A_n}}$
A_2 (2)	0	1	1

The equations of the Sum and the Carry can be obtained from Table 5 to lead three different designs:

1) Conventional design in [15]–[17], [19], which uses Eq. (2).
2) Cascading TMUXs design in [20], [21], which uses Eq. (3).
3) Unary operators-based design in [14], [22]–[25], [34] and adopted in this paper, which uses Eq. (4).

$$\begin{aligned} Sum &= 2 \cdot (A_0B_2 + A_1B_1 + A_2B_0) \\ &\quad +1 \cdot (A_0B_1 + A_1B_0 + A_2B_2) \\ Carry &= 1 \cdot (A_1B_2 + A_2B_1 + A_2B_2) \end{aligned} \tag{2}$$

$$\begin{aligned} Sum &= A.B_0 + (1.A_0 + 2.A_1 + 0.A_2).B_1 \\ &\quad +(2.A_0 + 0.A_1 + 1.A_2).B_2 \\ Carry &= 0.B_0 + (0.A_0 + 0.A_1 + 1.A_2).B_1 \\ &\quad +(0.A_0 + 1.A_1 + 1.A_2).B_2 \end{aligned} \tag{3}$$

$$Sum = A.B_0 + A^1.B_1 + A^2.B_2$$

$$Carry = 0.B_0 + (1 \cdot \bar{A_p}).B_1 + (1 \cdot \bar{A_n}).B_2 \tag{4}$$

where A_i and B_i, $i \in \{0,1,2\}$.

Figure 2 shows the proposed THA with 35 CNTFETs using eight unary operators, transmission gates (TGs), and dual-voltages (Vdd, Vdd/2). Without using cascading TGs, which is the advantage compared to THA with 34 CNTFETs in [34] that used cascading TGs. Because cascading TGs provide higher propagation delays and energy consumption.

When the voltage supply (Vdd) decreases in a transistor then the propagation delay will increase. Therefore, any path from inputs to outputs contains transistors that have voltage supply equal to Vdd/2, that path will have higher propagation than other paths that have voltage supply equal Vdd.

The dotted red line is the critical path which is the maximum propagation delay 7.74 ps (we got that value from the simulation results) from the input A to the output Carry via (A, An, $1 \cdot \bar{A_n}$, TG (B, Bp), then Carry), when A changes from 0 to 1, B = 2, and Carry from 0 to 1.

B. THE PROPOSED TERNARY MULTIPLIER

The 1-trit ternary multiplier (TMUL) can multiply two ternary inputs (A and B) and produces two outputs: the Product and the Carry, as described in truth Table 6.

TABLE 6. The truth table of TMUL.

Product

A/B	B_0 (0)	B_1 (1)	B_2 (2)
A_0 (0)	0	0	0
A_1 (1)	0	1	2
A_2 (2)	0	2	1

A | $\overline{A^2}$

Carry

A/B	B_0 (0)	B_1 (1)	B_2 (2)
A_0 (0)	0	0	0
A_1 (1)	0	0	0
A_2 (2)	0	0	1

The equations of the Product and Carry can be obtained from Table 6 to lead three designs:

1) Conventional design in [15]–[17], [19], which uses Eq. (5).
2) Cascading TMUXs design in [20], [21], which uses Eq. (6).
3) Unary operators-based design in [14], [22]–[25] and adopted in this paper, which uses Eq. (7).

$$\begin{aligned} Product &= 2 \cdot (A_1B_2 + A_2B_1) \\ &\quad +1 \cdot (A_1B_1 + A_2B_2) \\ Carry &= 1 \cdot A_2B_2 \end{aligned} \tag{5}$$

$$\begin{aligned} Product &= 0.B_0 + A.B_1 + (0.A_0 + 2.A_1 + 1.A_2).B_2 \\ Carry &= 0.B_0 + 0.B_1 + (0.A_0 + 0.A_1 + 1.A_2).B_2 \end{aligned} \tag{6}$$

$$\begin{aligned} Product &= 0 \cdot B_0 + A \cdot B_1 A + \bar{A^2}B_2 \\ Carry &= 0 \cdot B_0 + 0 \cdot B_1 + (1 \cdot \bar{A_p})B_2 \end{aligned} \tag{7}$$

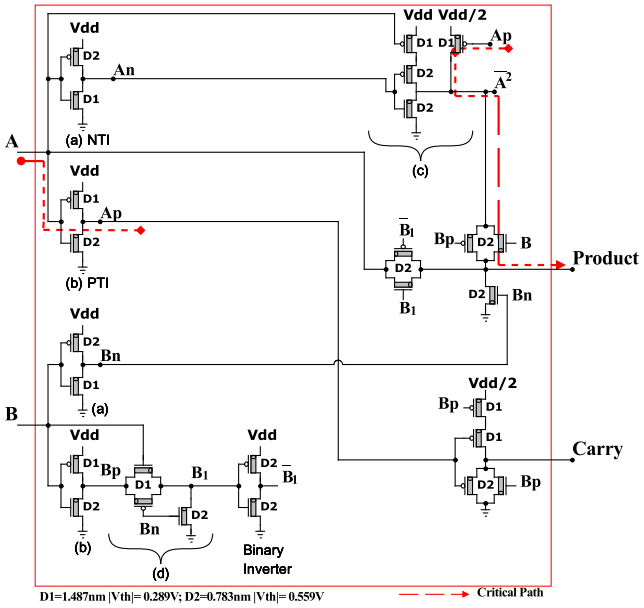


FIGURE 3. The proposed TMUL with 26 CNTFETs: (a) NTI, (b) PTI, the proposed (c) A^2, and (d) B_1. Using Unary operators-based design in Eq. (7).

Figure 3 shows the proposed TMUL with 26 CNTFETs using four unary operators, transmission gates (TGs), and dual-voltages (Vdd, Vdd/2).

The dotted red line is the critical path which is the maximum propagation delay 9.33 ps from the input A to the output Product via (A, Ap, $\bar{A^2}$, TG (B, Bp), then Product), when A changes from 1 to 2, B = 2, and Product from 2 to 1.

IV. SIMULATION RESULTS AND COMPARISONS

The proposed ternary unary operators, THA, and TMUL are validated, simulated, and compared to 32 nm channel CNTFET-Based ternary circuits in [15]–[23], [25], [27], [29], [31]–[34] using the HSPICE simulator.

Figures 4 and 5 show the transient analysis of the proposed THA, and TMUL with power supply at 0.9 V, the temperature at 27°C, and the frequency at 1 GHz. All input signals have a fall and rise time of 20 ps.

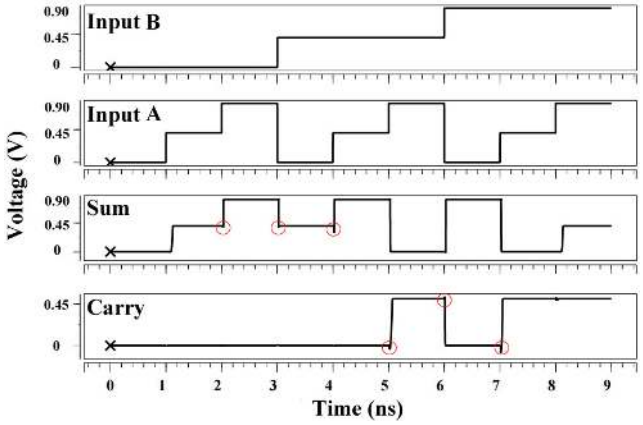


FIGURE 4. Proposed THA transient analysis.

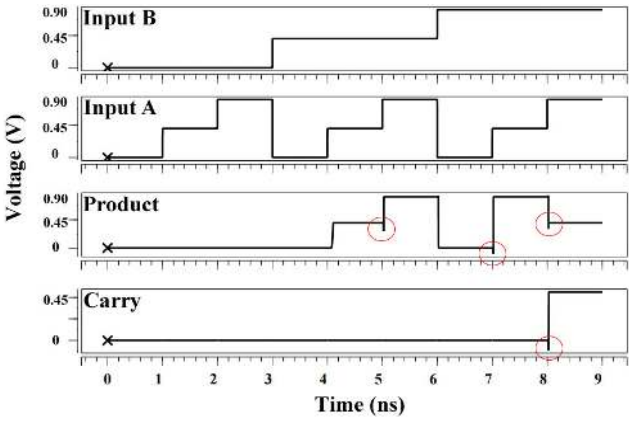


FIGURE 5. Proposed TMUL transient analysis.

Tables 7, 8, and 9 show the comparison of all investigated circuits for Unary Operators, THAs, and TMULs in terms of transistors count, average power, maximum delay, and PDP with power supply at 0.9 V, the temperature at 27°C, and the frequency at 1 GHz.

TABLE 7. Unary Operators Comparison.

	CNTFETs count	Power (nW)	Max. Delay (ps)	PDP (x10^{-20} J)
$\bar{A}^2$ in [23]	13	580	7.38	428
$\bar{A}^2$ in [22]	3	100	1.8	18
$\bar{A}^2$ in [37]	4	6	1.7	1
Proposed $\bar{A}^2$	4	4	2.32	0.93
Improvement w.r.t [37]	0%	50%	-36.4%	7.53%
A_1 in [15]	10	572	6.12	350
Proposed A_1	3	8	4.3	3.4
Improvement	70%	98.60%	29.74%	99%

TABLE 8. THAs Comparison.

THA / Year	CNTFETs Count	Power (μW)	Max. Delay (ps)	PDP (x10^{-18} J)
In [15] 2011	136	2.54	56.51	143.53
In [16] 2016	112	1.93	53.14	102.56
In [17] 2017	112	1.84	43.25	79.58
In [18] 2020	108 (GNRFET)	0.26	38.7	10.06
In [19] 2019	85	0.53	74.63	39.55
In [20] 2018	168	1.97	21.15	41.66
In [21] 2020	90	0.14	10.66	1.49
In [22] 2016	39	9.42	18.29	172.3
In [23] 2017	64	0.99	8.52	8.43
In [25] 2020	48	0.43	51.86	22.29
In [27] 2020	48	0.14	35.5	4.97
In [29] 2020	50	0.32	**4.3**	1.37
In [31] 2017	94	0.59	17.62	10.39
In [31] Design 2	66	0.25	16.52	4.13
In [32] 2018	64	0.37	23.45	8.67
In [33] 2021	60	0.18	7.27	1.31
In [34] 2021	34	0.128	9.5	1.21
Proposed THA	**35**	**0.12**	7.74	**0.99**
Improvement w.r.t [15]*	74.2%	95.3%	86.3%	99.3%
w.r.t [34]**	-2.9%	6.3%	18.5%	18.2%

* Compared to the highest PDP among other circuits
** Compared to the lowest PDP among other circuits

TABLE 9. TMULs Comparison.

TMUL / Year	CNTFETs Count	Power (μW)	Max. Delay (ps)	PDP (x10^{-18} J)
In [15] 2011	100	1.88	46.32	87.08
In [16] 2016	86	1.45	43.05	62.42
In [17] 2017	76	1.32	31.26	41.26
In [19] 2019	61	0.42	54.82	23.02
In [20] 2018	112	1.93	18.21	35.15
In [23] 2017	58	0.64	16.63	10.64
In [25] 2020	30	0.22	46.06	10.13
In [26] 2020	60	0.17	9.65	1.64
In [29] 2020	38	0.28	**4.81**	1.35
Proposed TMUL	**26**	**0.06**	**9.33**	**0.56**
Improvement w.r.t [15]*	74%	96.80%	79.86%	99.35%
w.r.t [29]**	31.6%	78.57%	-93.9%	58.52%

* Compared to the highest PDP among other circuits
** Compared to the lowest PDP among other circuits

A. RESULTS DISCUSSION

The power consumption in a transistor is composed of two types: Dynamic and Static.

Dynamic power is the power consumed while charging and discharging the capacitive nodes in the process of switching.

Static power essentially consists of the power used when the transistor is not in the process of switching. If diode-connected transistors exist, then the transistors will act as Resistors. Thus, Joule effect power is created and generated heat in the circuit.

Total Power consumption :

$$P = P_s + P_d \tag{8}$$

Static Power :

$$P_s = N * Vdd * Id + N_d * R * Id^2 \tag{8a}$$

Dynamic Power :

$$P_d = N * Vdd^2 * f * CL \tag{8b}$$

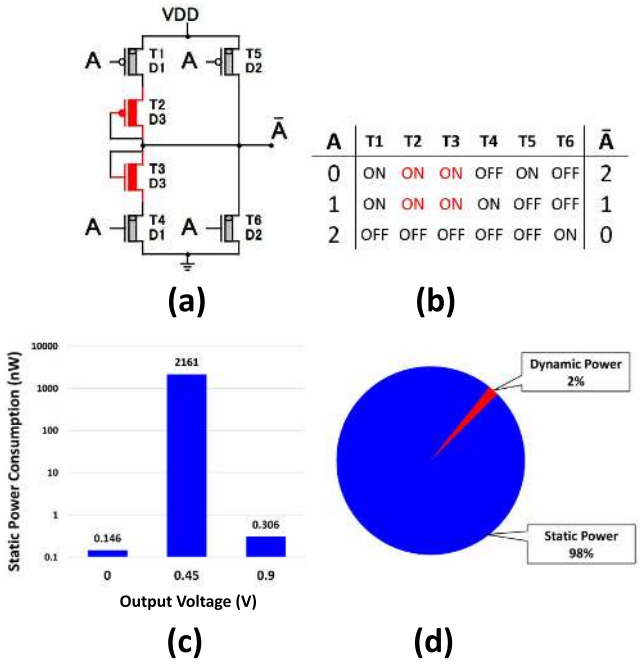
where,

N : Number of transistors in the circuit
Nd : Number of Diode-Connected transistors if exist
Vdd : Power Supply
Id : Current in transistors
f : Frequency of the Vinput
CL : Load Capacitor and Internal Capacitance
R : Resistor value of the Diode-Connected Transistor

To decrease the power consumption, we must remove the diode-connected transistors and reduce the number of transistors.

The results of the proposed designs are very good as expected, as shown in Tables 8 and 9, due to our major contributions (See Subsection I.C.). We will explain the results in detail, as follow.

1) The proposed designs do not use diode-connected transistors that act like resistors to generate logic 1 (Vdd/2). This technique will generate the direct current path from the power supply (Vdd) to the ground, which will increase the static power in a drastic way, as described in equation (8a). Therefore, one of the advantages of this paper is the use of Vdd/2 in the designs to eliminate these two diode-connected transistors and to decrease the static power to a very small value due to very small leakage current in CNFET transistor.
   The Standard Ternary Inverter (STI) is the typical example to generate logic 1 from one power source Vdd. We analyze the static power of STI [15] in Fig. 6: (a) The transistor-level of STI, (b) the truth table of STI, (c) shows that when logic 1 (0.45V) is generated by two diode-connected transistors, the static power is 2000 times higher than other outputs, and (d) shows that 98% from the average power consumption is for static power.
2) The proposed designs do not utilize basic logic gates, TDecoders, and encoders that lead to high transistors count and PDP.
3) The proposed designs use unary operators of the ternary system that can replace the basic logic gates, which significantly reduce the number of used transistors and energy consumption.



A	T1	T2	T3	T4	T5	T6	Ā
0	ON	ON	ON	OFF	ON	OFF	2
1	ON	ON	ON	ON	OFF	OFF	1
2	OFF	OFF	OFF	OFF	OFF	ON	0

FIGURE 6. Static power analysis of the STI of [15]. (a) The transistor-level, (b) the truth table of STI, (c) shows the static power consumption according to the output voltage level, and (d) shows the ratio of the static power and dynamic power in the average power consumption.

So as explained above, the proposed designs reduce the power consumption more than 90% compared to [15]–[21] that use diode-connected transistors and between 6% and 60% reduction compared to [29], [31], [33], [34] that do not use diode-connected transistors.

B. PVT VARIATIONS

To validate and test the proposed designs by how are working in all different conditions?

Therefore, this paper analyses and simulates the proposed and all the investigated THAs and TMULs for PVT (Process, Voltage, Temperature) variations.

Process variation is generally occurring change in the attributes of transistors (i.e., oxide thickness, length, ...) during the fabrication of the integrated circuits (ICs). The variation becomes a larger percentage at smaller process nodes and has a strong influence on the behavior of the circuits.

Therefore, all THAs and TMULs circuits are validated in the presence of major process variations: TOX, CNT's Count, Channel length, and CNT diameter using Monte Carlo analysis [38].

Monte Carlo analysis is based on the statistical Gaussian distributions with ±5%, ±10%, and ±15% variations at the ±3 sigma (σ) level with 1000 running simulations.

Also, the proposed circuits and all the investigated circuits simulated with voltage variations (from 0.8V to 1V) and temperature variations (from 10°C to 70°C).

Figures 7 and 8 show the comparison to the existing THA of [15], [21], [23], [34] and TMUL of [15], [19], [25], [29].

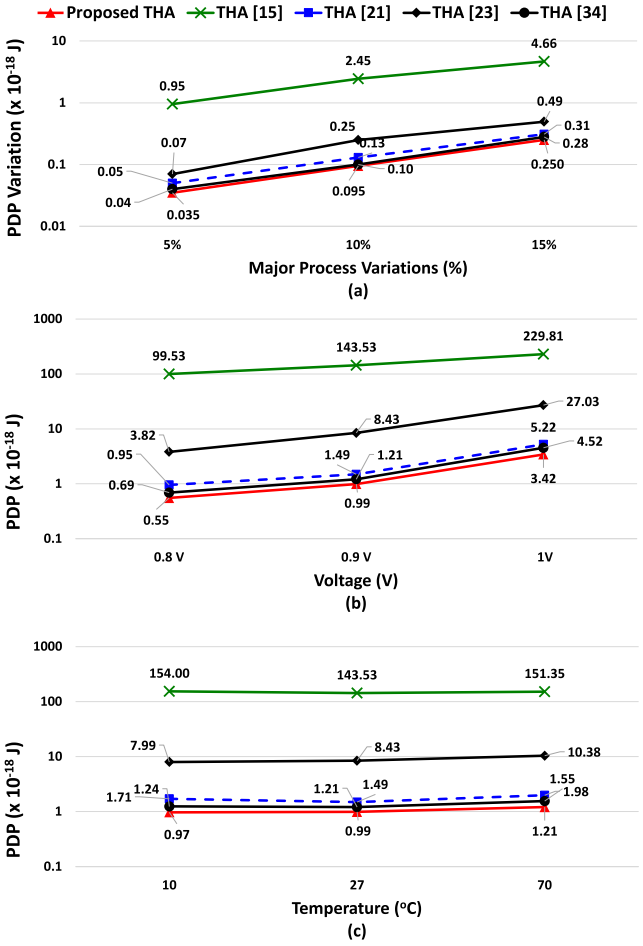


FIGURE 7. PVT Variations for THAs: (a) Major Process Variations, (b) Voltage Variations, (c) Temperature Variations.

We choose one reference to compare from each section in Table 1 "Summary of literature review", which is the best among its technique.

Figures 7(a) and 8(a) show that the proposed THA and TMUL have a lower sensitivity to process variations and more robustness compared to the other designs because their PDP variations are the smallest among all the investigated circuits.

Figures 7(b) and 8(b) show that the proposed THA and TMUL have a significant reduction in PDP between 18.2% & 99.44% for THA and between 48.7% & 99% for TMUL with voltage variations (from 0.8V to 1V), the temperature at 27°C, and frequency at 1 GHz.

Figures 7(c) and 8(c) show that the proposed THA and TMUL have a significant reduction in PDP between 18.2% & 99.37% for THA and between 57.8% & 99.3% for TMUL with temperature variations (from 10°C to 70°C), the voltage at 0.9V, and frequency at 1 GHz.

C. NOISE EFFECT

In addition to PVT validation, the proposed circuits are tested with the injection into the inputs by a noise signal, as shown

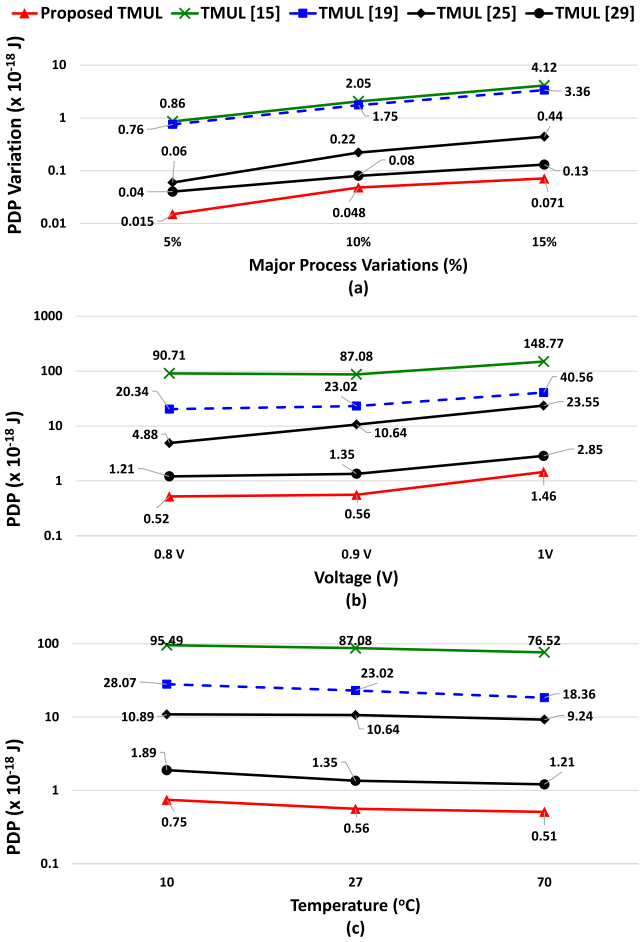


FIGURE 8. PVT Variations for TMULs: (a) Major Process Variations, (b) Voltage Variations, (c) Temperature Variations.

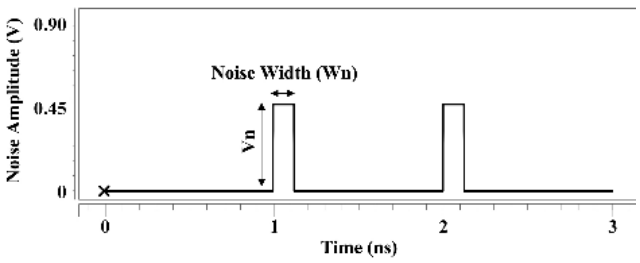


FIGURE 9. Noise Signal.

in Fig. 9. The noise signal has a pulse width (W_n) and a pulse amplitude (V_n).

To determine the influence of noisy inputs on all circuits, the Noise Immunity Curve (NIC) is used.

To draw NIC, choose a W_n and try several values for V_i to get the maximum value of V_i, which is V_n that the output remains correct.

Above that point (W_n, V_n), the circuit will provide an output error. Then we choose another value of W_n and try again to get new V_n, and so on till we get an almost horizontal line. We do it for all investigate circuits.

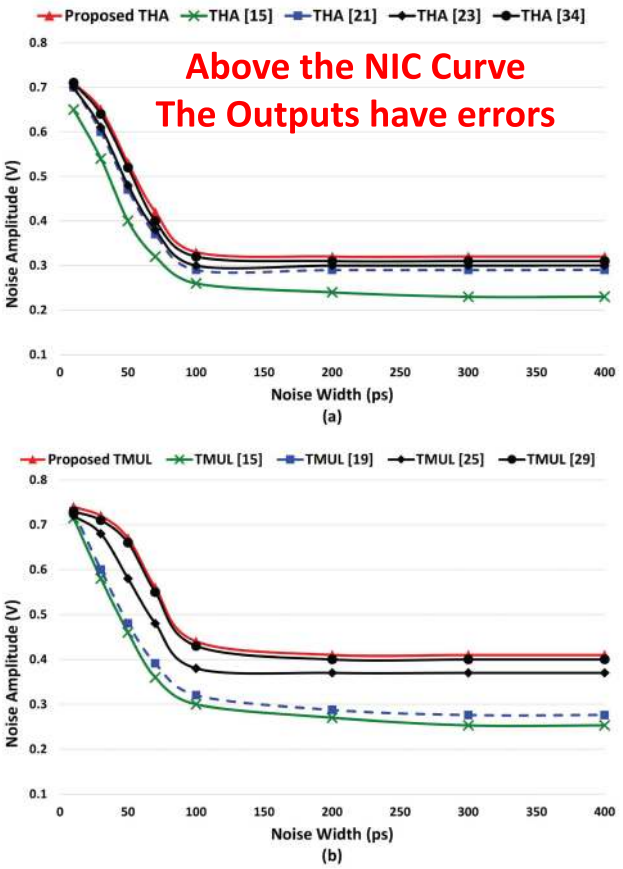


FIGURE 10. Noise Immunity Curve (NIC) for: (a) THAs, (b) TMULs.

Thus, any circuit with higher NIC shows a more noise-tolerant circuit [39].

Figure 10 shows that the proposed THA and TMUL have higher noise immunity among other designs because their NIC curves are above all curves.

D. SCALABILITY STUDY

To verify the scalability of the proposed THA and TMUL in big circuits. Two and three cascading THAs, and two cascading TMULs are simulated with power supply at 0.9 V, the temperature at 27°C, the frequency at 1 GHz, and fall and rise time of 20 ps, as shown in Tables 10 and 11.

TABLE 10. Scalability of the proposed THA.

	Power (μW)	Max. Delay (ps)	PDP (x10^{-18} J)
Without Cascading	0.12	7.74	0.99
Cascading Two THAs	0.18	13.1	2.36
Cascading Three THAs	0.22	18.3	4.03

TABLE 11. Scalability of the proposed TMUL.

	Power (μW)	Max. Delay (ps)	PDP (x10^{-18} J)
Without Cascading	0.06	9.33	0.56
Cascading Two TMULs	0.08	14.2	1.13

* The outputs of cascading three TMULs are zeros.

When the number of cascading THAs and TMULs are increasing, the power consumption, delay, and PDP are increasing less than or around double. Therefore, the proposed THAs and TMULs have scalability in big circuits.

V. CONCLUSION

This paper proposed novel designs of 32 nm CNTFET-Based Ternary Half Adder and Ternary Multiplier using proposed Unary Operators combined with transmission gates without using ternary decoders, basic logic gates, or ternary encoders.

The design process utilizes different techniques in terms of transistor arrangement, two power supplies (Vdd, Vdd/2), transistor count reduction to reach the final target.

The HSPICE simulation results of the proposed circuits to existing circuits demonstrate higher performance and lower energy consumption for different simulation environments, such as PVT (process, voltage, and temperature) variations, and the noise effect study. The results confirmed that the proposed circuits had higher robustness to process variations and higher noise tolerance than other models.

Finally, the proposed THA and TMUL can be implemented in low-power nano-scale embedded systems and IoT devices to save battery consumption.

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REFERENCES

[1] W. Zhao and G. Prenat, Eds., *Spintronics-Based Computing*. Cham, Switzerland: Springer, 2015. [Online]. Available: http://link.springer.com/10.1007/978-3-319-15180-9

[2] G. Hills *et al.*, "Understanding energy efficiency benefits of carbon nanotube field-effect transistors for digital VLSI," *IEEE Trans. Nanotechnol.*, vol. 17, no. 6, pp. 1259–1269, Nov. 2018. [Online]. Available: https://ieeexplore.ieee.org/document/8476614/

[3] S. L. Hurst, "Multiple-valued logic—Its status and its future," *IEEE Trans. Comput.*, vol. C-33, no. 12, pp. 1160–1179, Dec. 1984, doi: 10.1109/TC.1984.1676392.

[4] Y. Chen, Z. Wang, A. Patil, and A. Basu, "A 2.86-TOPS/W current mirror cross-bar-based machine-learning and physical unclonable function engine for Internet-of-Things applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 6, pp. 2240–2252, Jun. 2019. [Online]. Available: https://ieeexplore.ieee.org/document/8608007/

[5] X.-N. Ye, K.-H. Liu, and S.-T. Liong, "A ternary bitwise calculator based genetic algorithm for improving error correcting output codes," *Inf. Sci.*, vol. 537, pp. 485–510, Oct. 2020. [Online]. Available: https://linkinghub.elsevier.com/retrieve/pii/S0020025520305053

[6] R. A. Jaber, A. M. El-Hajj, A. M. Haidar, and A. Kassem, "A novel CNFET-based ternary to binary converter design in data transmission," in *Proc. 32nd Int. Conf. Microelectron. (ICM)*, Dec. 2020, pp. 1–4.

[7] N. Saleh, A. Kassem, and A. M. Haidar, "Energy-efficient architecture for wireless sensor networks in healthcare applications," *IEEE Access*, vol. 6, pp. 6478–6486, 2018. [Online]. Available: http://ieeexplore.ieee.org/document/8247183/

[8] A. Saha, N. D. Singh, and D. Pal, "Efficient ternary comparator on CMOS technology," *Microelectron. J.*, vol. 109, Mar. 2021, Art. no. 105005. [Online]. Available: https://linkinghub.elsevier.com/retrieve/pii/S0026269221000161

[9] F. Zahoor, F. A. Hussin, F. A. Khanday, M. R. Ahmad, I. M. Nawi, C. Y. Ooi, and F. Z. Rokhani, "Carbon nanotube field effect transistor (CNTFET) and resistive random access memory (RRAM) based ternary combinational logic circuits," *Electronics*, vol. 10, no. 1, p. 79, Jan. 2021. [Online]. Available: https://www.mdpi.com/2079-9292/10/1/79

[10] S. Bos, H. Gundersen, and F. Sanfilippo, "UMemristorToolbox: Open source framework to control memristors in unity for ternary applications," in *Proc. IEEE 50th Int. Symp. Multiple-Valued Log. (ISMVL)*, Nov. 2020, pp. 212–217.

[11] R. A. Jaber, A. M. El-Hajj, A. M. Haidar, A. Kassem, and L. A. Nimri, "A novel binary to ternary converter using double pass-transistor logic," in *Proc. 31st Int. Conf. Microelectron. (ICM)*, Cairo, Egypt, Dec. 2019, pp. 240–243. [Online]. Available: https://ieeexplore.ieee.org/document/9021886/

[12] M. K. Q. Jooq, M. H. Moaiyeri, and K. Tamersit, "Ultra-compact ternary logic gates based on negative capacitance carbon nanotube FETs," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, early access, Dec. 24, 2020, doi: 10.1109/TCSII.2020.3047265.

[13] N. Azimi, R. F. Mirzaee, K. Navi, and A. M. Rahmani, "Ternary DDCVSL: A combined dynamic logic style for standard ternary logic with single power source," *IET Comput. Digit. Techn.*, vol. 14, no. 4, pp. 166–175, Jul. 2020. [Online]. Available: https://onlinelibrary.wiley.com/doi/10.1049/iet-cdt.2019.0216

[14] E. Shahrom and S. A. Hosseini, "A new low power multiplexer based ternary multiplier using CNTFETs," *AEU, Int. J. Electron. Commun.*, vol. 93, pp. 191–207, Sep. 2018, doi: 10.1016/j.aeue.2018.06.011.

[15] S. Lin, Y.-B. Kim, and F. Lombardi, "CNTFET-based design of ternary logic gates and arithmetic circuits," *IEEE Trans. Nanotechnol.*, vol. 10, no. 2, pp. 217–225, Mar. 2011. [Online]. Available: http://ieeexplore.ieee.org/document/5340626/

[16] M. Muglikar, R. Sahoo, and S. K. Sahoo, "High performance ternary adder using CNTFET," in *Proc. 3rd Int. Conf. Devices, Circuits Syst. (ICDCS)*, Coimbatore, India, Mar. 2016, pp. 236–239. [Online]. Available: http://ieeexplore.ieee.org/document/7570599/

[17] H. Samadi, A. Shahhoseini, and F. Aghaei-Liavali, "A new method on designing and simulating CNTFET_based ternary gates and arithmetic circuits," *Microelectron. J.*, vol. 63, pp. 41–48, May 2017, doi: 10.1016/j.mejo.2017.02.018.

[18] Z. T. Sandhie, F. U. Ahmed, and M. H. Chowdhury, "Design of ternary logic and arithmetic circuits using GNRFET," *IEEE Open J. Nanotechnol.*, vol. 1, pp. 77–87, 2020.

[19] R. A. Jaber, A. Kassem, A. M. El-Hajj, L. A. El-Nimri, and A. M. Haidar, "High-performance and energy-efficient CNFET-based designs for ternary logic circuits," *IEEE Access*, vol. 7, pp. 93871–93886, 2019. [Online]. Available: https://ieeexplore.ieee.org/document/8759881/

[20] D. Das, A. Banerjee, and V. Prasad, "Design of ternary logic circuits using CNTFET," in *Proc. Int. Symp. Devices, Circuits Syst. (ISDCS)*, Howrah, India, Mar. 2018, pp. 1–6. [Online]. Available: https://ieeexplore.ieee.org/document/8379661

[21] R. A. Jaber, A. M. El-Hajj, A. Kassem, L. A. Nimri, and A. M. Haidar, "CNFET-based designs of ternary half-adder using a novel 'decoder-less' ternary multiplexer based on unary operators," *Microelectron. J.*, vol. 96, Feb. 2020, Art. no. 104698, doi: 10.1016/j.mejo.2019.104698.

[22] B. Srinivasu and K. Sridharan, "Low-complexity multiternary digit multiplier design in CNTFET technology," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 8, pp. 753–757, Aug. 2016. [Online]. Available: http://ieeexplore.ieee.org/document/7409999/

[23] B. Srinivasu and K. Sridharan, "A synthesis methodology for ternary logic circuits in emerging device technologies," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 8, pp. 2146–2159, Aug. 2017. [Online]. Available: http://ieeexplore.ieee.org/document/7895162/

[24] T. Sharma and L. Kumre, "CNTFET-based design of ternary arithmetic modules," *Circuits, Syst., Signal Process.*, vol. 38, no. 10, pp. 4640–4666, Oct. 2019, doi: 10.1007/s00034-019-01070-9.

[25] T. Sharma and L. Kumre, "Energy-efficient ternary arithmetic logic unit design in CNTFET technology," *Circuits, Syst., Signal Process.*, vol. 39, no. 7, pp. 3265–3288, Jul. 2020, doi: 10.1007/s00034-019-01318-4.

[26] R. A. Jaber, A. M. Haidar, and A. Kassem, "CNTFET-based design of ternary multiplier using only multiplexers," in *Proc. 32nd Int. Conf. Microelectron. (ICM)*, Dec. 2020, pp. 1–4.

[27] S. Kim, S.-Y. Lee, S. Park, K. R. Kim, and S. Kang, "A logic synthesis methodology for low-power ternary logic circuits," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 9, pp. 3138–3151, Sep. 2020. [Online]. Available: https://ieeexplore.ieee.org/document/9089220/

[28] S. Tabrizchi, N. Azimi, and K. Navi, "A novel ternary half adder and multiplier based on carbon nanotube field effect transistors," *J. Zhejiang Univ. Sci. C*, vol. 18, no. 3, pp. 423–433, Mar. 2017, doi: 10.1631/FITEE.1500366.
[29] A. D. Zarandi, M. R. Reshadinezhad, and A. Rubio, "A systematic method to design efficient ternary high performance CNTFET-based logic cells," *IEEE Access*, vol. 8, pp. 58585–58593, 2020. [Online]. Available: https://ieeexplore.ieee.org/document/9044858/
[30] F. Zahoor, T. Z. A. Zulkifli, F. A. Khanday, and S. A. Z. Murad, "Carbon nanotube and resistive random access memory based unbalanced ternary logic gates and basic arithmetic circuits," *IEEE Access*, vol. 8, pp. 104701–104717, 2020. [Online]. Available: https://ieeexplore.ieee.org/document/9099815/
[31] S. K. Sahoo, G. Akhilesh, R. Sahoo, and M. Muglikar, "High-performance ternary adder using CNTFET," *IEEE Trans. Nanotechnol.*, vol. 16, no. 3, pp. 368–374, May 2017. [Online]. Available: http://ieeexplore.ieee.org/document/7809029/
[32] C. K. Vudadha and M. B. Srinivas, "Design of high-speed and power-efficient ternary prefix adders using CNFETs," *IEEE Trans. Nanotechnol.*, vol. 17, no. 4, pp. 772–782, Jul. 2018. [Online]. Available: https://ieeexplore.ieee.org/document/8353717/
[33] A. S. Vidhyadharan and S. Vidhyadharan, "An ultra-low-power CNFET based dual V ternary dynamic half adder," *Microelectron. J.*, vol. 107, Jan. 2021, Art. no. 104961. [Online]. Available: https://linkinghub.elsevier.com/retrieve/pii/S0026269220305607
[34] R. A. Jaber, B. Owaidat, A. Kassem, and A. M. Haidar, "A novel low-energy CNTFET-based ternary half-adder design using unary operators," in *Proc. Int. Conf. Innov. Intell. Informat., Comput. Technol. (3ICT)*, Dec. 2020, pp. 1–6.
[35] J. Deng and H.-S.-P. Wong, "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—Part II: Full device model and circuit performance benchmarking," *IEEE Trans. Electron Devices*, vol. 54, no. 12, pp. 3195–3205, Dec. 2007. [Online]. Available: http://ieeexplore.ieee.org/document/4383022/
[36] M. D. Miller and M. A. Thornton, "MVL concepts and algebra," in *Multiple Valued Logic: Concepts and Representations*, vol. 2. San Rafael, CA, USA: Morgan & Claypool, 2008, ch. 2, p. 32, doi: 10.2200/S00065ED1V01Y200709DCS012.
[37] S. Tabrizchi, A. Panahi, F. Sharifi, K. Navi, and N. Bagherzadeh, "Method for designing ternary adder cells based on CNFETs," *IET Circuits, Devices Syst.*, vol. 11, no. 5, pp. 465–470, Sep. 2017. [Online]. Available: https://onlinelibrary.wiley.com/doi/10.1049/iet-cds.2016.0443
[38] A. Raychowdhury and K. Roy, "Carbon nanotube electronics: Design of high-performance and low-power digital circuits," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 11, pp. 2391–2401, Nov. 2007. [Online]. Available: http://ieeexplore.ieee.org/document/4383254/
[39] G. Balamurugan and N. R. Shanbhag, "The twin-transistor noise-tolerant dynamic circuit technique," *IEEE J. Solid-State Circuits*, vol. 36, no. 2, pp. 273–280, Feb. 2001. [Online]. Available: http://ieeexplore.ieee.org/document/902768/

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