

Novel Thermally Enhanced Power Package

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Abstract— Heat generated in microelectronic devices as a result of dissipated power is a major issue in power electronics applications resulting in elevated application PC board temperatures. In order to minimize the downward heat transfer to the application board an efficient method enabling the upward flow of heat from the silicon die to the top of the microelectronic package and subsequently transferred to the environment via forced convection needs to be employed [1]. The problem is that most of the current packaging technologies have a very poor junction-to-top thermal resistance so it is very difficult to have a substantial portion of the heat flowing to the top of the device [2]. In this paper we present a novel power package design that enables heat conduction to the top surface of the microelectronic package through the use of a high thermal conductivity path which reduces by more than a factor of ten the junction-to-top thermal resistance compared to standard solutions. The thermal resistance junction-to-top is found to be as low as 1 C/W, which is comparable with thermal resistance junction to board. This allows for a significant portion of the dissipated energy in the die to be conducted to the topside of the package where natural or forced convection can transfer the heat to the air. We discuss the design, manufacturability, performance and reliability of the package as well as thermal measurements which demonstrates the ability of the package to dissipate the heat. We also compare this solution with existing solutions in the marketplace.

I. INTRODUCTION

Continuous integration of microelectronic devices and shrinkage in electronic board dimensions are driving power densities to levels that endanger the performance and reliability of the electronic systems. This increase in power dissipation density is particularly worse in power application boards. Engineers and System designers have to design solutions that maintain temperatures of key components under certain limits to ensure proper electrical performance and reliability. For example many computing applications have a strict rule of 100C for the maximum temperature the board can reach in operation. One solution to this problem is to conduct the generated heat to the external environment via natural or forced convection, instead of conducting it to the board. Since the heat is generated internally in the

microelectronic devices it is critical to have a package solution that allows the heat to be easily transferred to the ambient. A package technology, referred to as DUAL COOL™, was developed that allows standard QFN type of devices to achieve very low junction-to-top thermal resistance (Θ_{j-t}). In the first section the technology is described along with manufacturability aspects. In the second section the results of the thermal measurements of the package are shown and comparing the results with standard package solutions available in the marketplace.

II. TECHNOLOGY DESCRIPTION

Figure 1 shows a construction diagram of a device using a DUAL COOL™ technology. The backside electrode of MOSFET die is attached to the leadframe of the package with solder and a copper clip is soldered to the topside electrode. In a standard QFN package the device is over molded with low thermal conductivity mold compound making the thermal resistance to the top of the device (Θ_{j-t}) high.

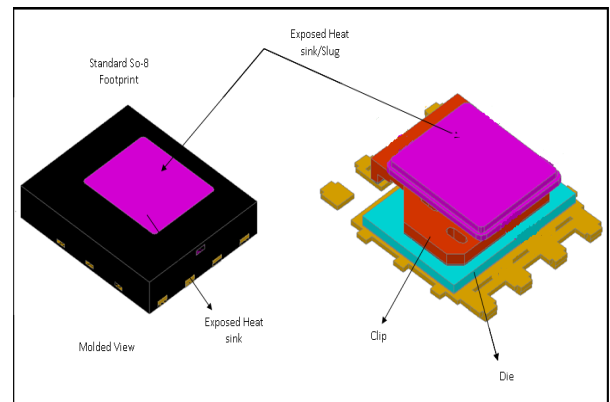


Figure 1: Construction diagram of a dual cool device

In this case the high thermal conductivity of the copper leadframe will force most of the heat to be conducted downwards to the application board. The DUAL COOL™

technology consists of an exposed heat sink or heat slug connected to the clip providing for a low thermal resistance path for the heat to be conducted to the topside of the device. Using this technology thermal resistances to the top of the device (Θ_{j-t}) are comparable to thermal resistance junction to case (Θ_{j-c}), so similar amounts of heat can be dissipated to the environment provided an appropriate heat sink is attached to the top of the device as we show in Figure 3. The DUAL COOL™ devices are manufactured with same set of tools used for the standard QFN device (SO-8 footprint compatible) so no major changes are needed in the QFN production line to manufacture devices with DUAL COOL™ technology. Design consideration were taken into account for small non-coplanarities between the heat slug and the mold cavity producing mold flashes/ mold bleeds in the event the heat slug is not in full contact with the mold cavity. This was solved by tightening the height tolerances of the internal components of the device and controlling the bond line thickness of the die attach. In addition, a mechanical buffing step was added at the end of the process flow to eliminate residual mold compound flashes over the exposed heat sink. The product is fully qualified and passed Moisture Sensitivity Level 1 classification.

III. THERMAL PERFORMANCE

Figure 2 shows the thermal resistance junction to top for three 5x 6 mm QFN devices with the same silicon die but different constructions: a) the wire bond package has seven 8 mil Al wires connecting the drain to the pins b) the clip package used a 10 mil thick clip covering 70% of the die area to connect the drain with the external pins and c) the same clip package but in this case we used a dual cool technology.

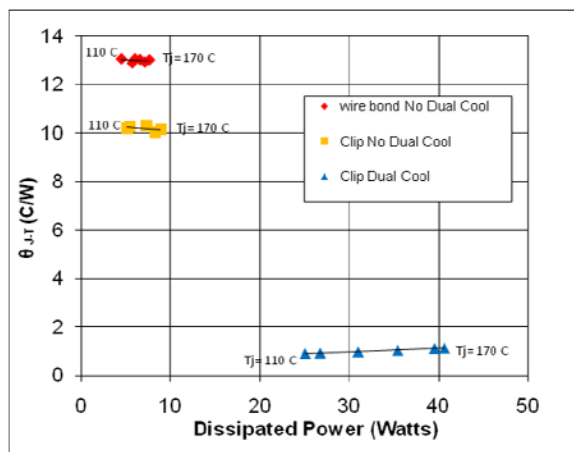


Figure 2: Thermal resistance junction-top vs power

The results (Fig 2.) show a dramatic improvement when the DUAL COOL™ technology is used by reducing this thermal resistance by a factor of ten. The wire bond solution has the highest Θ_{j-t} (13 C/W) reflecting the poor capability the wires and the mold compound to conduct the heat to the top side. The clip package has a lower Θ_{j-t} (10.2 C/W) because the thick Cu clip on top of the die helps to conduct the heat to the topside. As expected the device that uses the DUAL COOL™ technology has the lowest thermal resistance

junction-to-top of package ($\Theta_{j-t} = 1$ C/W) similar to the junction to case thermal resistance (Θ_{j-c}) (exposed pad of the leadframe on the backside of the package).

To evaluate the system level impact of the DUAL COOL™ technology, simulations were performed using a model that considers the device mounted on a typical board and with a heat sink mounted on top of the device. To make the calculations, datasheet values for all the thermal resistances associated with the devices (Θ_{j-t} and Θ_{j-c}) and standard values for thermal resistances board to air $\Theta_{B-A} = 7^\circ\text{C/W}$ and thermal resistance device top to air $\Theta_{T-A} = 2.5^\circ\text{C/W}$ were used.

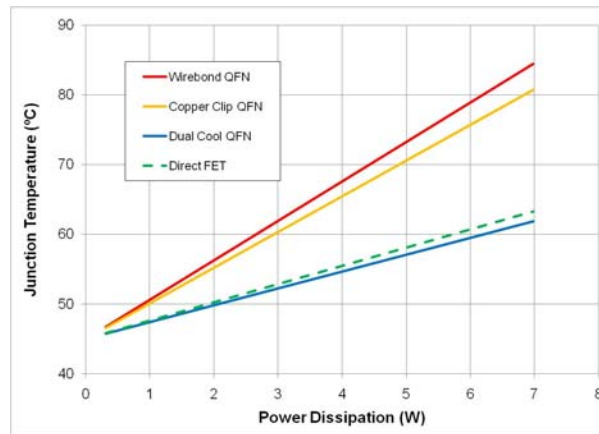


Fig 3: Thermal performance comparison for different packaging technologies.

Fig 3 shows the results of the simulation for different packaging technologies [3]. The plot shows the junction temperature as a function of the dissipated power. As you can see the improvement in thermal performance using the DUAL COOL™ technology is significant. For a typical power dissipation of 5 Watts the reduction in the junction temperature is 16 C or almost 25%. The DUAL COOL™ solution has excellent thermal characteristics because the power dissipated in the active device channel on the top side of the die is in close proximity to the Cu clip, so heat moving to the top side only needs to conduct through the Cu clip and heat slug.

To further demonstrate the effect of the DUAL COOL™ technology on the thermal performance of a device we performed an experiment with the objective of comparing a standard device with a device that uses the DUAL COOL™ technology. Two MOSFET transistors with the same die were packaged in a clip QFN 5x6 mm. Device “A” utilized the DUAL COOL™ technology while device “B” did not. This is the only difference between both devices. The devices were mounted to identical standard application boards and attached to heat sinks commonly used by in systems. The temperature of the junction was measured using an *Analysis-Tech* thermal measurement system that allows the junction temperature to be measured by using the forward diode voltage of the transistor as a thermometer (after a proper calibration). A thermal IR camera was also used to measure the external

temperature of the system. In the first part of the experiment we forced a enough continuous current through the transistors to dissipate a power of $P_{diss}=2.1W$ (this is a typical dissipation of these transistors in the real application) while a fan of 300 lfm is forcing convection parallel to the fins of the heat sink. Figure 4 shows the results. For the same conditions the device using the DUAL COOL™ technology has a junction temperature of $T_j=58^\circ C$ in comparison with $T_j=71^\circ C$ of the device that does not. This is a reduction of $13^\circ C$ or a reduction of 20% in junction temperature for the same conditions in a real application board. The IR image also shows the difference in temperature of the heat sink of both systems: device “A” (DUAL COOL™) shows a hotter heat sink than device B (standard solution) indicating that more heat is being conducted to the top in the system using the DUAL COOL™ concept.

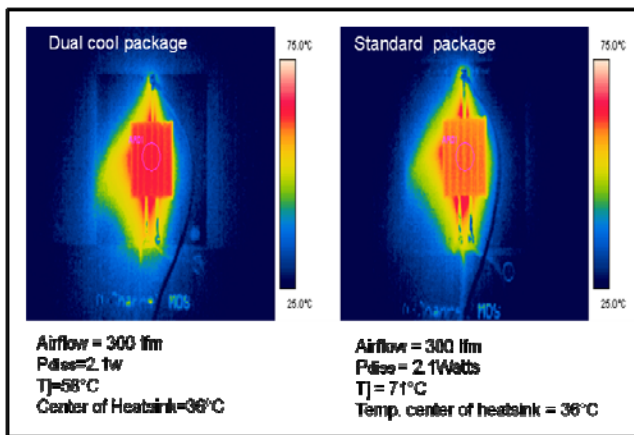


Fig 4: Results of the experiment to compare the dual cool solution with the standard technology at system level.

Figure 5 shows how the effectiveness of the DUAL COOL™ technology changes if the fan off is turned off. As you can see the improvement of $13^\circ C$ or 20% with the fan on is reduced to $8^\circ C$ or 7% with the forced convection off. Clearly the maximum advantage of the DUAL COOL™ technology is obtained in a forced convection situation.

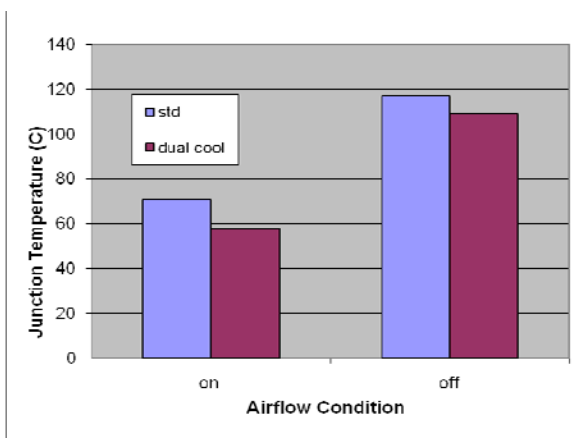


Fig 5: Advantages of using dual cool technology with or without forced convection.

Another way to take advantage of the DUAL COOL™ technology is to increase the current capability of the device keeping the same junction temperature. In Fig. 6 the results of such a condition are shown. The dissipated power P_{diss} is adjusted for both systems until the same junction temperature was measured in both devices “A” and “B”. It can be seen that with the fan on, the current in device “A” can be increased up to a 30% and still have the same junction temperature as device “B”.

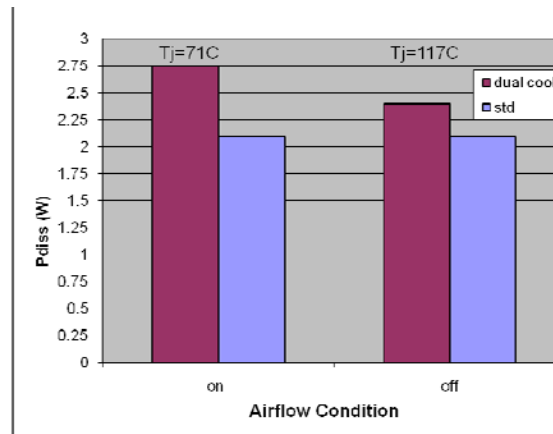


Fig 6: Current in the dual cool device can be increased keeping the same junction temperature

IV. CONCLUSIONS

An innovative and cost effective high power packaging technology that reduces the junction-to-top thermal resistance to a level comparable to the thermal resistance junction to case has been presented.

Thermal measurements confirm the dramatic improvement in performance in comparison with standard wire bond and clip package technologies were shown. Systems level simulations that show the improvement from a real application point of view were also demonstrated. At the system design level the DUAL COOL™ technology can enable the following benefits:

- 1) Higher current densities for a given junction temperature.
- 2) Lower junction temperatures and lower PC board temperatures resulting in increased long term reliability.

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