Novel Transformer-Flux-Balancing Control of Dual-Active-Bridge Bidirectional Converters

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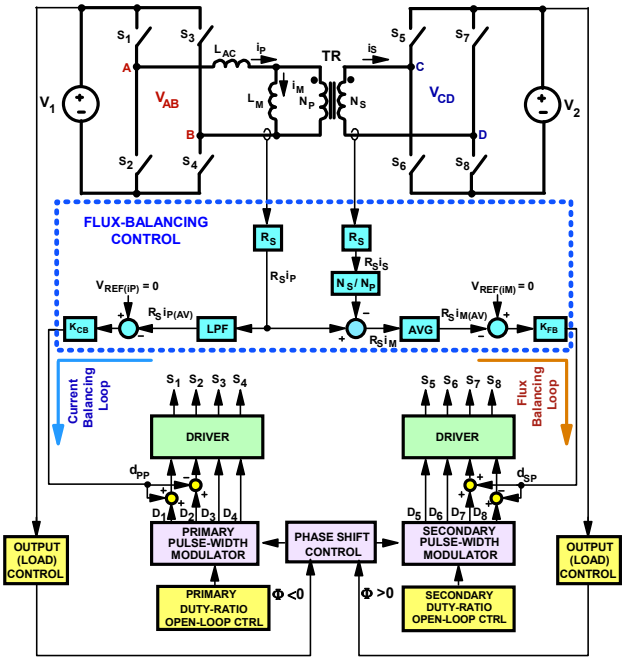
***Abstract* - In this paper, a novel flux-balancing method for the isolated dual-active-bridge (DAB) bidirectional converter based on direct control of the magnetizing current is proposed. In the proposed method, the dc component of the primary and secondary current is controlled by providing two control loops; one to keep the average magnetizing current approximately zero and the other to keep the average primary and secondary current approximately zero. The performance of the proposed flux-balancing control is experimentally evaluated on a 3.3-kW DAB prototype designed for automotive applications.**

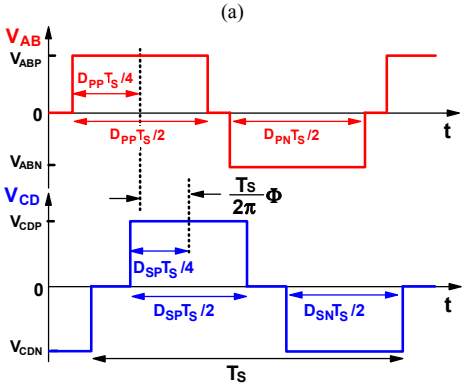
I. Introduction

Today, bidirectional converters are increasingly finding applications in power systems with energy-storage capability, most notably in "smart"-grid and automotive applications [1]. Generally, they are employed to condition charging and discharging of the energy-storage devices such as batteries and supercapacitors. Specifically, in automotive applications, isolated bidirectional dc-dc converters are used in electric vehicles (EVs) to provide bidirectional energy exchange between the high-voltage (HV) and low-voltage (LV) battery, whereas bidirectional ac-dc converters are required for future vehicle-to-grid (V2G) applications. Due to a relatively wide battery-voltage range that is dependent on battery's state of charge, achieving high efficiency across the entire battery voltage range is a major design challenge of bidirectional dc-dc converters.

One of the most widely used bidirectional isolated converter topology is the dual-active-bridge (DAB) converter [2], shown in Fig. 1(a). Generally, the power flow in the DAB converter is controlled by phase-shift Φ between bridge voltages V_{AB} and V_{CD}, as illustrated in Fig. 1(b). For positive phase shifts, power flows from source V_1 to source V_2, i.e., source V_1 delivers power while source V_2 receives power. Therefore, for positive phase shifts $\Phi>0$ source V_1 can be considered to be the input and source V_2 to be the output to the load. For negative phase shifts $\Phi<0$, the power flow is in the reverse direction so that V_2 can be considered to be the input and V_1 to be the output to the load. Since the output side typically requires regulation, bidirectional converters may require two output (load) control feedback loops, as illustrated in Fig. 1(a). These two loops work one at a time. For positive phase-shifts $\Phi>0$ the loop regulating the V_2 side is active, whereas for negative phase-shifts $\Phi<0$ the loop regulating the V_1 side is active. It should be noted that in the circuit in Fig. 1(a),



(a)



(b)

Fig. 1 DAB converter: (a) power stage and control block diagram, (b) waveforms of the primary-side and secondary-side bridge voltages V_{AB} and V_{CD}

depending on the nature of sources V_1 and V_2 the output (load) loops are set up to regulate the respective output voltages, and/or output currents, and/or output power.

Various aspects of DAB converter performance optimization are addressed in numerous technical papers [3]-[8]. The majority of these papers are focused on their efficiency improvements through power-stage refinements and advanced control techniques, such as duty-cycle modulation of the switches in the individual bridges as shown in Figs. 1(a) and (b). However, the transformer saturation issue, which is of paramount importance for reliable operation of isolated bidirectional converters, is almost completely ignored in the literature, although isolated bidirectional converters are more susceptible to transformer saturation than their unidirectional counterparts. Namely, because in bidirectional converters both the primary and secondary side of the transformer are connected to voltage sources, any differences of duty cycles caused by mismatching of drive signals timing and/or unequal voltage drops on semiconductor switches cause a difference in positive and negative volt-seconds, which leads to flux walking that eventually may result in transformer core saturation.

Generally, passive and active approaches used in unidirectional isolated full-bridge converters to eliminate transformer saturation due to flux walking can also be applied in bidirectional converters. Passive approaches include conservative transformer designs with a low peak flux density and large core gap that can absorb the anticipated worst-case flux imbalance without saturating the core and/or adding blocking capacitors in series with the primary and/or secondary winding of the transformer to eliminate their dc currents [9]-[12]. These passive approaches are not desirable because the transformer overdesign approach leads to an increased transformer core and/or requires an increased peak value of the magnetizing current which increases conduction and switching losses [9]-[11], whereas the blocking-capacitor approach requires additional components which increase the size and cost [12].

A number of active approaches that are based on sensing of transformer currents and using sensed signals to modify duration of driving signals of the switches to maintain flux balance in unidirectional isolated converters have been introduced [13]-[15], whereas a methods of preventing transformer saturation in DAB converters have been introduced in [16], [17]. In [16], a flux-density transducer, called "magnetic ear," is employed to measure flux density in the core of the transformer and eliminate its dc component by an active flux-balancing control loop. This paper also offers an excellent review of existing direct and indirect sensing and measurement methods of the magnetic flux in the core of the transformer, as well as the review of passive and active methods of preventing core saturation. In [17], a method of preventing transformer saturation in Dual-Active-Bridge-Buck-Boost (DAB^3) converter has been proposed. In this active flux-balancing method, the dc component of the primary and secondary current of the transformer are virtually eliminated by sensing the average primary and secondary current and injecting the signal proportional to their value into the sensed filter inductor current which by peak-current control adjusts and maintains the flux-balance of both the primary and secondary winding.

In this paper, a novel flux-balancing method for the DAB bidirectional converter based on direct control of the magnetizing current outlined in [18] is thoroughly described, analyzed, and its performance experimentally verified. In the proposed method, the dc component of the primary and secondary current is controlled by providing two control loops; one to keep the average magnetizing current approximately zero and the other to keep the average primary and secondary current approximately zero. The flux-balancing loop that keeps magnetizing current zero is implemented by calculating the average magnetizing current from the sensed primary and secondary current and by adjusting the duty cycle of the switches of one bridge so that the dc component of the magnetizing current is eliminated. The current-balancing loop that keeps the average primary and secondary current zero is implemented by averaging the sensed primary or the sensed secondary current and using it to adjust the duty cycle of the switches in the other bridge to eliminate their dc components. The performance of the proposed flux-balancing control is experimentally evaluated on a 3.3-kW DAB prototype designed for automotive applications.

II. PROPOSED FLUX-BALANCING METHOD

The blocks related to proposed transformer flux-balancing control are shown in Fig. 1(a) inside the dashed blue rectangle. In Fig. 1(a), the control of the DAB circuit is implemented with two current-control feedback loops in addition to the output-feedback control loops and the primary- and secondary-side duty-cycle open-loop control. One current loop is used to regulate average magnetizing current i_M^{av} to approximately zero to avoid saturation of the transformer magnetic core, whereas the other control loop is employed to regulate average primary current i_P^{av} to approximately zero to prevent unnecessary power loss in the primary and secondary side of the converter caused by the dc component of these currents, as well as to prevent the eventual saturation of the magnetic core of inductor L_{AC}.

Two current loops are needed because the magnetizing current is given by the difference between primary current i_P and scaled secondary current i_S, i.e., as $i_M = i_P - \frac{N_S}{N_P} i_S$, where N_P and N_S are the number of turns of the primary and secondary winding, respectively. Therefore, forcing the average magnetizing current to zero by the magnetizing current control loop does not guarantee that the average primary and secondary currents are also zero since the zero value of the average magnetizing current can be achieved with non-zero values of the average primary and secondary currents [18].

In Fig. 1(a), the current loop that regulates the average magnetizing current is implemented by sensing primary current i_P and secondary current i_S by current-sensing devices with gain R_S and subtracting the sensed value of the primary current $R_S \cdot i_P$ from the scaled value of the sensed secondary current $(N_S/N_P) \cdot R_S \cdot i_S$ to obtain the sensed value of magnetizing current $R_S \cdot i_M$. Sensed magnetizing current $R_S \cdot i_M$ is then averaged by the AVG block in Fig. 1(a). After the averaging, average sensed magnetizing current $R_S \cdot i_M^{av}$ is compared with reference $V_{REF(iM)}$ that is set to zero value. The difference between the average sensed magnetizing current and its reference is further processed by controller K_{FB} whose output modulates the duty cycles of the complementary-switched same-leg secondary-side switches S_7 and S_8 so that the value of sensed magnetizing current $R_S \cdot i_M^{av}$ is maintained at approximately zero.

The complementary modulation of the duty cycle of secondary-side switches S_7 and S_8, shown in Fig. 1(a), i.e., the change of the duty cycle of switch S_7 by amount d_{SP} and a simultaneous change of the duty cycle of the same-leg switch S_8 for an equal amount of the opposite sign, $-d_{SP}$, causes the modulation of duty cycle of positive bridge voltage V_{CDP}, as illustrated in Fig. 2. As can be seen in Fig. 2, during half-periods of negative bridge voltage

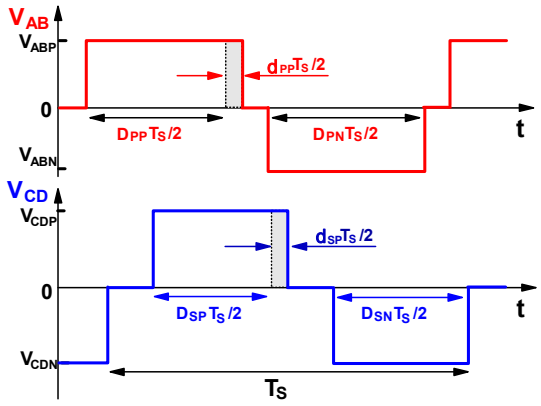


Fig. 2 Modulation of primary and secondary bridge voltages V_{AB} and V_{CD} to implement proposed flux-balancing control.

V_{CDN} no modulation takes place. With this one-sided modulation, the control can adjust the positive volt-second product across the secondary winding and, therefore, magnetizing inductance, to balance the flux between the positive and negative half-periods, i.e., to maintain the average magnetizing current approximately at zero.

The current loop that regulates the average primary current is implemented by averaging sensed primary current $R_S \cdot i_P$ by low-pass filter (LPF) block in Fig. 1(a). After the averaging, average sensed primary current $R_S \cdot i_P^{av}$ is compared with reference $V_{REF(iP)}$ that is set to zero value. The difference between the average sensed primary current and its reference is further processed by controller K_{CB} whose output modulates the duty cycles of the complementary-switched same-leg primary-side switches S_3 and S_4 so that the value of sensed primary current $R_S \cdot i_P^{av}$ is maintained at approximately zero. It should be noted that by maintaining both the average magnetizing and primary current close to zero by the two-current-loop control, the average secondary current, which is proportional to the difference between these two currents, is also kept close to zero.

The complementary modulation of the duty cycle of primary-side switches S_3 and S_4, i.e., the change of the duty cycle of switch S_3 by amount d_{PP} and a simultaneous change of the duty cycle of the same-leg switch S_4 for the equal amount of the opposite sign, $-d_{PP}$, causes the modulation of duty cycle of positive bridge voltage V_{AB}, as illustrated in Fig. 2. As can be seen from Fig. 2, during negative half-periods of bridge voltage V_{AB} no modulation takes place. With this one-sided modulation, the control can adjust the positive volt-second product across the inductor L_{AC} to balance the flux between the positive and negative half-periods, i.e., to maintain the average inductor current at approximately zero value.

To be effective in preventing transformer saturation, the flux-balancing loop that keeps the average magnetizing current to approximately zero must be very fast. It should be designed with the maximum possible loop bandwidth since the loop must respond to any transformer core flux imbalances as fast as possible. The bandwidth of the primary current balancing loop that eliminates the dc component of the primary current may be much lower than that of the flux-balancing loop since primary inductor L_{AC} is designed to carry substantial dc current without saturating its magnetic core. By having the bandwidths of two current-control loops well separated, the interaction between the two loops is virtually eliminated which enhances the robustness of the control.

Finally, it should be noted that the bandwidths of the output-feedback loops must also be well separated from the bandwidths of the two current loops to avoid undesirable loop interactions. For this reason, the bandwidths of the output loops should be placed well below the bandwidth of the fast flux-balancing control loop and well above the bandwidth of the slow current-balancing loop.

III. Modeling, Analysis, And Design Considerations

A. General Considerations

Implementation of the proposed flux-balancing control can be either analog or digital. A digital implementation of the proposed control in DAB converter is preferred since today's DSPs offer adequate performance and flexibility to implement a reliable control that requires simultaneous phase-shift and duty-cycle modulation.

The digital implementation of the flux-balancing control which is analyzed in this paper is shown in Fig. 3. In the implementation in Fig. 3, the sensed magnetizing current is first sampled and quantized by analog-to-digital converter ADC and then averaged to obtain the value of its dc component. The magnetizing current averaging can be implemented in many different ways, i.e., by employing various averaging algorithms. To be effective in preventing transformer saturation, the flux-balancing loop must be very fast and, therefore, the averaging time of the magnetizing current must be minimized. In digital implementations, the averaging time can be minimized by calculating the magnetizing current average value from the sum of two samples taken one-half of the switching period apart, i.e., 180° out of phase [19]. This approach is possible and provides acceptable accuracy because the magnetizing current waveform exhibits odd symmetry.

As shown in Fig. 3, the sensed average magnetizing current is compared with the zero reference and the difference is processed by compensator K_{FB} and PWM modulator which adjusts the duty cycle of secondary bridge voltage V_{CD} so that the average magnetizing current is maintained to approximately zero.

In this paper, simple proportional compensator with gain K_{FB} was selected to provide fast loop response and low computation time. Gain K_{FB} can be either constant or adaptive. Adaptive implementation is desirable in applications where the input and/or the output voltage have a wide range. A proportional compensator has lower regulation accuracy than a compensator with an integral action. However, when gain K_{FB} is properly designed, the proportional control accuracy is sufficient since a practical transformer can tolerate a small dc magnetizing current without saturation.

Since the current-balancing loop is slow, the averaging of the primary current in Fig. 3 is performed by an RC filter. Compensator K_{CB} of the current-balancing loop can be propor-

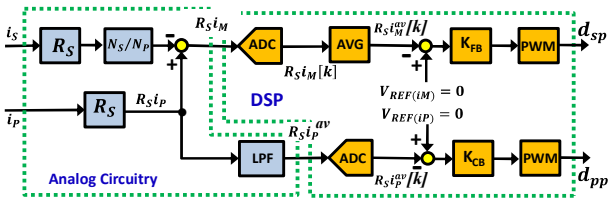


Fig.3 Proposed digital implementation of flux-balancing and current-balancing controls.

tional or proportional-integral one. In this paper, proportional compensator K_{CB} was selected to reduce DSP computational load.

B. DAB Converter Power Stage Simplified Model

To facilitate the analysis and design optimization of the proposed transformer flux-balancing control, the DAB power stage is represented by the primary-side-referred large-signal equivalent circuit shown in Fig. 4(a). In the circuit in Fig. 4(a), L_M is the primary-side magnetizing inductance, $N = N_{PRIM}/N_{SEC}$ is the transformer turns ratio, and R_{PRIM} and R_{SEC} are the total resistances on the primary and the secondary side, respectively. Specifically, resistor R_{PRIM} represents the on-resistances of conducting primary switches S1-S4 and the ac resistances of inductor L_{AC} and the transformer primary winding, whereas resistor R_{SEC} represents the on-resistances of conducting secondary switches S5-S8 and the ac resistance of the transformer secondary winding. As shown in Fig. 2, voltage sources V_{AB} and V_{CD} are dependent on duty cycles d_{PP} and d_{SP}, respectively.

Because the bandwidth of the flux-balancing loop is much higher than that of the current-balancing loop, further simplifications of the model in Fig. 4(a) are possible. Specifically, it can be assumed that primary-bridge voltage V_{AB} that is modulated to regulate the current-balancing loop is unchanged during the modulation of secondary-bridge voltage V_{CD} that is employed for flux-balancing control. As a result, when analyzing the fast flux-balancing loop, the equivalent circuit in Fig. 4(a) can be simplified to one shown in Fig. 4(b) since $N^2R_{SEC} \ll R_{PRIM} + sL_{AC}$., except at very low frequencies.

Similarly, when analyzing the slow current-balancing loop, it can be assumed that average magnetizing current i_M^{av} and average bridge-voltage V_{CD}^{av} are kept to zero by the fast flux-balancing loop so that the equivalent circuit at low frequencies is simplified to one in Fig. 4(c), where $R_{TOTAL} = R_{PRIM} + N^2R_{SEC}$.

C. Flux-Balancing Control

Because of well-separated bandwidths, design optimization of the flux- and current-balancing loop can be performed independently. The block diagram of the fast flux-balancing-loop according to the control implementation in Fig. 3 is shown in Fig. 5, where $G_{i_M d_{SP}}(s)$ is the duty-cycle-to-magnetizing-current transfer function. Since the loop consists of continuous-time and discrete-time blocks, it can be modeled either in s- or z-domain. Due to the digital implementation of the control, it is more accurate to model the flux-balancing loop in z-domain. This

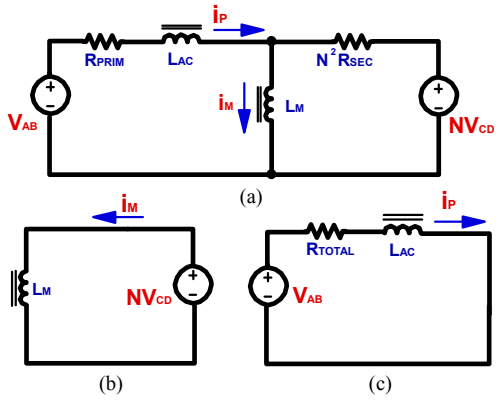


Fig. 4 DAB converter power stage model: (a) primary-side-referred large-signal equivalent circuit, (b) simplified equivalent circuit for flux-balancing control, and (c) simplified equivalent circuit for current-balancing control.

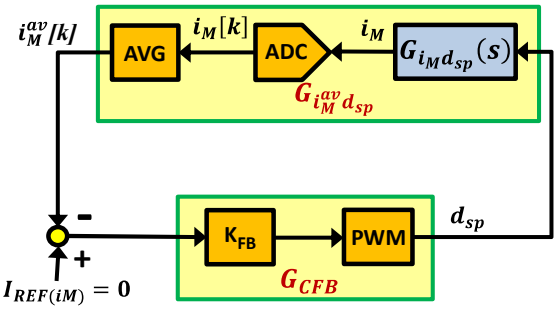


Fig. 5 Block diagram of flux-balancing loop according to control implementation in Fig. 3.

modeling is performed by finding z-transfer functions $G_{i_M^{av} d_{SP}}(z)$ and $G_{CFB}(z)$, shown in Fig. 5. $G_{i_M^{av} d_{SP}}(z)$ represents the discrete-time transfer function from duty cycle d_{SP} to average magnetizing current i_M^{av}, whereas $G_{CFB}(z)$ represents the transfer function of the discrete-time controller of the flux-balancing loop.

Since discrete-time modeling in this paper is based on establishing recursive relationship between the average magnetizing current values in consecutive sampling periods, modeling of the magnetizing current waveform is required. According to the simplified model in Fig. 4(b), for a bipolar square-wave voltage V_{CD}, the waveform of magnetizing current i_M is piecewise linear, as shown in Fig. 6. As can be seen in Fig. 6, sampling period T_{SMP} is equal to one-half of switching period T_S and the samples are taken in the middle of the off time, i.e., in the middle of the intervals where voltage V_{CD}=0.

Two implementations of the flux-balancing loop were considered. In both implementations, the duration of positive voltage V_{CDP} is adjusted by modulating its duty cycle, as shown in Fig. 6. The adjustment of positive-voltage V_{CDP} duty cycle $D_{SP} + d_{SP}[k+1]$ in [k+1]-th switching period is based on the estimate of average magnetizing current $i_M^{av}[k]$ obtained in k-th switching period, namely

$$d_{SP}[k+1] = -K_{FB} \cdot i_M^{av}[k]. \quad (1)$$

Note that (1) assumes unity PWM gain.

For implementation A, average current $i_M^{av}[k]$ is estimated based on two consecutive magnetizing current samples from the [k-1]-th and [k]-th switching period, i.e., as

$$i_M^{av}[k] = \frac{1}{2}\left(i_M^{v}[k-1] + i_M^{peak}[k]\right), \quad (2)$$

whereas for implementation B the average magnetizing current is calculated from two samples in the [k]-th period, i.e., as

$$i_M^{av}[k] = \frac{1}{2}\left(i_M^{v}[k] + i_M^{peak}[k]\right). \quad (3)$$

The only difference between the two implementations is that for implementation B the delay time between the instant the average magnetizing current is calculated and the instant the duty cycle is changed is by one sampling period $T_{SMP}=T_S/2$ shorter. Because of a shorter delay time, implementation B is expected to achieve a higher bandwidth (for the same phase margin). On the other hand, a slower and cheaper DSP can be employed in implementation A since it offers more time for necessary calculations. In this paper, due to a space constraint derivations are performed for implementation A and only final expressions are given for implementation B.

To derive transfer function $G_{i_M^{av} d_{SP}}(z) = i_M^{av}(z)/d_{SP}(z)$, relationships between discrete values $i_M^{av}[k+1]$, $i_M^{av}[k]$, $d_{SP}[k+1]$, and $d_{SP}[k]$ are established based on inspection of Fig. 6 as

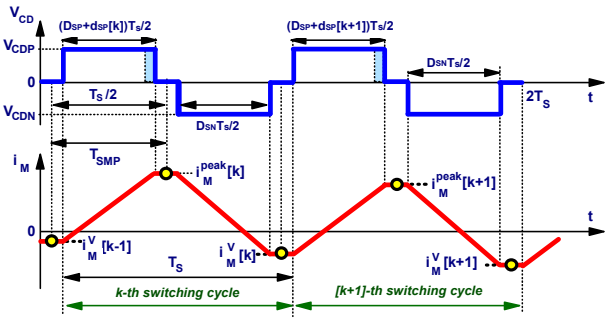


Fig. 6 Waveforms of bridge-voltage V_{CD} and magnetizing current i_M in two consecutive switching cycles.

$$i_M^{peak}[k] = i_M^v[k-1] + (D_{SP} + d_{SP}[k]) \cdot N \cdot V_{CDP}(T_S/2L_M) \quad (4)$$

$$i_M^v[k] = i_M^{peak}[k] - D_{SN} \cdot N \cdot V_{CDN} \cdot (T_S/2L_M), \quad (5)$$

$$i_M^{av}[k+1] = i_M^v[k] + 1/2 \cdot (D_{SP} + d_{SP}[k+1]) \cdot N \cdot V_{CDP} \cdot (T_S/2L_M). \quad (6)$$

From (2), (4)-(6), the difference equation relating the average magnetizing current and duty cycle can be obtained as

$$i_M^{av}[k+1] - i_M^{av}[k] = 2 \cdot V_{SEC}^{dc} \cdot B + 1/2 \cdot V_{CDP} \cdot B \cdot (d_{SP}[k+1] + d_{SP}[k]), \quad (7)$$

where $B = N \cdot T_S/2L_M$ and $V_{SEC}^{dc} = (D_{SP} \cdot V_{CDP} - D_{SN} \cdot V_{CDN})/2$ is the dc voltage applied across the secondary winding without the flux-balancing control.

Application of z-transform to difference equation (7) and its rearrangement results in

$$i_M^{av}(z) = 2 \cdot V_{SEC}^{dc} \cdot B \cdot \frac{z}{(z-1)^2} + 1/2 \cdot V_{CDP} \cdot B \cdot d_{SP}(z) \cdot \frac{z+1}{z-1} \quad (8)$$

From (8), transfer function $G_{i_M^{av} d_{SP}}(z) = i_M^{av}(z)/d_{SP}(z)$ is obtained by setting $V_{SEC}^{dc} = 0$ as

$$G_{i_M^{av} d_{SP}}(z) = 1/2 \cdot V_{CDP} \cdot B \cdot \frac{z+1}{z-1} \quad (9)$$

Control transfer function $G_{CFB}(z) = -d_{SP}(z)/i_M^{av}(z)$ is derived by applying z-transform to difference equation (1), which yields

$$d_{SP}(z) = -K_{FB} \cdot z^{-1} \cdot i_M^{av}(z), \quad (10)$$

so that

$$G_{CFB}(z) = K_{FB}/z, \quad (11)$$

In accordance with equations (8), (9), and (11), the resulting control block diagram is shown in Fig. 7. Flux-balancing loop gain $T_{FB}(z)$ is a product of transfer functions $G_{i_M^{av} d_{SP}}(z)$ and $G_{CFB}(z)$ and is given by

$$T_{FB}(z) = \frac{F}{2} \cdot \frac{z+1}{z \cdot (z-1)}, \quad (12)$$

where $F = K_{FB} \cdot V_{CDP} \cdot B$ is dimensionless control gain.

Transfer function $2B\frac{z}{(z-1)^2}$ in Fig. 7 models the effect of dc voltage V_{SEC}^{dc} on the flux-balancing loop operation, which causes non-zero steady-state value I_M^{dc} of average magnetizing current $i_M^{av}[k]$. From Fig. 8, the relationship between the average magnetizing current i_M^{av} and V_{SEC}^{dc} is derived as

$$i_M^{av}(z) = 2B\frac{z}{(z-1)^2} \cdot \frac{1}{1+T_{FB}(z)} V_{SEC}^{dc} = 2B\frac{z^2}{(z-1)\cdot[z^2+(F/2-1)z+F/2]} V_{SEC}^{dc} \quad (13)$$

According to z-transform finite-value property, steady-state value I_M^{dc} is calculated from (13) as

$$I_M^{dc} = \lim_{z \to 1}[(z-1) \cdot i_M^{av}(z)] = \frac{D_{SP} - D_{SN} \cdot V_{CDN}/V_{CDP}}{K_{FB}} \quad (14)$$

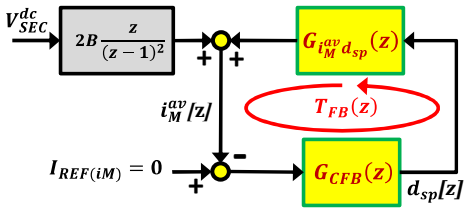


Fig. 7 Z-domain block diagram of the flux-balancing control loop.

Stability and dynamic performance of the flux-balancing control is determined by loop gain $T_{FB}(z)$. To analyze loop gain $T_{FB}(z)$ in frequency domain, it is mapped from z- to s-domain. Since both discrete-time signals $i_M^{av}(z)$ and $d_{SP}(z)$ are updated once per switching period T_S, mapping relationship $z = e^{j\omega T_S}$ is used. After the $z = e^{j\omega T_S}$ substitution, the loop gain in (12) can be expressed as

$$T_{FB}(e^{j\omega T_S}) = \frac{F}{2} \cdot \cot(\omega T_S/2) \cdot \frac{-j}{e^{j\omega T_S}}. \quad (15)$$

From (15), the magnitude and phase of the loop gain can be respectively derived as

$$|T_{FB}(\omega)| = \frac{F}{2} \cdot \cot(\omega T_S/2) \quad (16)$$

and

$$\arg\big(T_{FB}(\omega)\big) = -\frac{\pi}{2} - \omega T_S \quad (17)$$

From (16), the relationship between loop gain crossover frequency f_C, i.e., loop bandwidth, and control gain F is calculated

$$f_C/f_S = \frac{1}{\pi} \cdot \tan^{-1}(F/2), \quad (18)$$

where $f_S = 1/T_S$ is the switching frequency.

Equation (17) is used to derive stability phase margin PM

$$PM = \frac{\pi}{2} \cdot (1 - 4\, f_C/f_S) \quad (19)$$

To calculate the gain margin, phase frequency f_C^{zpm} that corresponds to the zero phase margin is calculated first from (19) as

$$f_C^{zpm}/f_S = 1/4. \quad (20)$$

Substituting (20) into (16), the relationship between stability gain margin GM and control gain F is obtained as

$$GM = -20 \cdot \log(F/2). \quad (21)$$

The last equation indicates that maximum control gain value which corresponds to stability boundary is $F_{MAX} = 2$.

Employing the same approach, derivations were also done for control implementation B. The results for both implementations A and B are summarized in Table I. As can be seen from Table I, for the given control gain, both implementations exhibit the same steady-state accuracy. However, for the same control gain implementation B exhibits higher loop bandwidth and higher phase margin than implementation A, as illustrated in Fig. 8 that shows normalized loop bandwidth f_C/f_S and phase margin PM as a function of control gain F for both implementations.

D. Current-Balancing Control

The block diagram of the slow current-balancing-loop according to the control implementation in Fig. 3 is shown in Fig. 9, where $G_{i_P d_{PP}}$ is the duty-cycle-to-primary-current transfer function. Since the current-balancing loop is very slow, i.e., its bandwidth is very much below the sampling frequency, it can be modeled in s-domain with adequate accuracy.

Since during current-balancing loop transients the flux-balancing loop maintains average secondary voltage V_{CD}^{av} and average magnetizing current i_M^{av} at zero level, small-signal changes of voltage V_{AB} are related to the corresponding changes

TABLE I. MODELING AND ANALYSIS RESULTS FOR TWO IMPLEMENTATIONS OF FLUX-BALANCING CONTROL.

	Implementation A	**Implementation B**
Control gain definition	$F = K_{FB} \cdot V_{CDP} \cdot N \cdot T_S / 2L_M$	
Loop Gain	$T_{FB}(z) = \frac{F}{2} \cdot \frac{z+1}{z \cdot (z-1)}$	$T_{FB}(z) = \frac{F}{z-1}$
Steady-state dc magnetizing current	$I_M^{dc} = \frac{D_{SP} - D_{SN} \frac{V_{CDN}}{V_{CDP}}}{K_{FB}}$	$I_M^{dc} = \frac{D_{SP} - D_{SN} \frac{V_{CDN}}{V_{CDP}}}{K_{FB}}$
Normalized loop bandwidth	$f_C/f_S = 1/\pi \cdot \tan^{-1}(F/2)$	$f_C/f_S = 1/\pi \cdot \sin^{-1}(F/2)$
Phase Margin	$PM = \pi/2 \cdot (1 - 4\, f_C/f_S)$	$PM = \pi/2 \cdot (1 - 2\, f_C/f_S)$
Gain Margin	$GM = -20 \cdot \log(F/2)$	$GM = -20 \cdot \log(F/2)$
Control gain corresponding to stability boundary	$F_{MAX} = 2$	$F_{MAX} = 2$

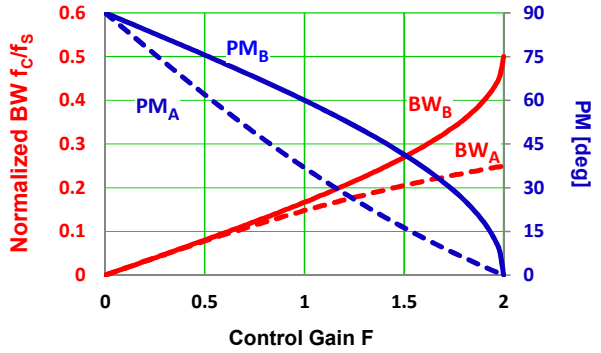


Fig. 8 Normalized bandwidth and phase margin versus control gain F for implementations A (dashed lines) and B (solid lines).

of primary current i_P according to the equivalent circuit in Fig. 4(c) as

$$\hat{v}_{AB}(s) = R_{TOTAL} \cdot [1 + s \cdot L_{AC}/R_{TOTAL}] \cdot \hat{\imath}_P(s), \quad (22)$$

where $\hat{v}_{AB}$ and $\hat{\imath}_P$ denote small-signal perturbations of primary-bridge voltage and primary current, respectively.

The relationship between perturbations of primary-bridge voltage V_{AB} and primary duty cycle d_{PP} can be found from perturbing of the average voltage V_{AB}

$$V_{AB}^{av} + \hat{v}_{AB} = \frac{(D_{PP}+\hat{d}_{PP}) \cdot V_{ABP} \cdot T_S/2 - D_{PN} \cdot V_{ABN} \cdot T_S/2}{T_S} = \frac{D_{PP} \cdot V_{ABP} - D_{PN} \cdot V_{ABN}}{2} + \frac{V_{ABP}}{2} \hat{d}_{PP}. \quad (23)$$

From (23) relationships for small-signal and steady-state signal components are derived respectively as

$$\hat{v}_{AB} = \frac{V_{ABP}}{2} \hat{d}_{PP} \quad (24)$$

and

$$V_{AB}^{av} = V_{PRIM}^{dc} + \frac{V_{ABP}}{2} d_{PP}, \quad (25)$$

where V_{PRIM}^{dc}=$[D_{PP} \cdot V_{ABP} - D_{PN} \cdot V_{ABN}]/2$ is the dc voltage across the primary winding.

Taking into account (22), (25), and control equation, the block diagram for steady-state operation of the current-balancing loop is shown in Fig. 10. Dc voltage V_{PRIM}^{dc} in Fig. 10 disturbs the current-balancing loop operation and causes non-zero steady-state value I_P^{dc} of the average primary current. From Fig. 10, the relationship between the steady-state average primary current and V_{PRIM}^{dc} is derived as

$$I_P^{dc} = \frac{V_{PRIM}^{dc}}{R_{TOTAL} \cdot \left[1 + \frac{V_{ABP} \cdot K_{CB}}{2 \cdot R_{TOTAL}}\right]} \quad (26)$$

From (22) and (24), the power stage small-signal transfer function of the power stage $G_{i_{PRIM}d_{PP}}(s)$ is obtained as

$$G_{i_P d_{PP}}(s) = \frac{\hat{\imath}_P(s)}{\hat{d}_{PP}(s)} = \frac{V_{ABP}}{2 \cdot R_{TOTAL} \cdot [1 + s \cdot L_{AC}/R_{TOTAL}]}. \quad (27)$$

The small-signal block diagram of the current-balancing control loop in s-domain is shown in Fig. 11. Delay block $e^{-s \cdot T_D}$ in Fig. 11 represents total time delay T_D in the loop which includes the digital controller calculation time and the digital PWM delay. Typical value of this delay is between one and two sampling periods depending on the speed of employed DSP and sampling frequency. Since bandwidth f_{CI} of the current-balancing loop is much lower than switching frequency f_S, i.e., since $f_{CI} \ll f_S$, the effect of delay time T_D on the loop performance (bandwidth and phase margin) can be neglected.

It should be noted that, different from the flux-balancing loop model, resistances R_{PRIM} and R_{SEC} cannot be neglected in modeling transfer function $G_{i_{PRIM}d_{PP}}(s)$. Since typically $L_{AC} \ll L_M$, pole frequency $f_P = 1/(2\pi\, L_{AC}/R_{TOTAL})$ is higher than current-balancing-loop crossover frequency f_{CI}. As a result, within the bandwidth of the loop, $G_{i_P d_{PP}}(s)$ is approximately a constant gain. If R_{TOTAL} is neglected, $G_{i_P d_{PP}}(s)$ behaves as an integrator within the loop bandwidth, which is not correct.

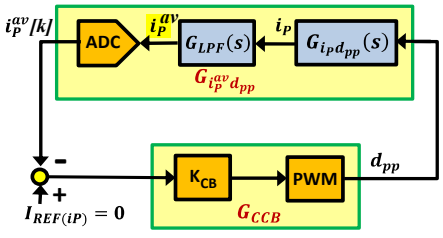


Fig. 9 Block diagram of current-balancing loop according to control implementation in Fig. 3.

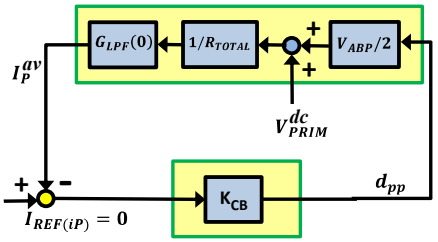


Fig. 10 Steady-state block diagram of the current-balancing control loop.

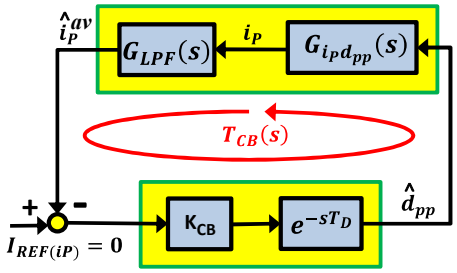


Fig. 11 S-domain small-signal block diagram of the current-balancing control loop.

From Fig. 11, neglecting the effect of the digital time delay, current-balancing loop gain T_{CB} is given by

$$T_{CB}(s) = G_{i_P d_{PP}}(s) \cdot G_{LPF}(s) \cdot K_{CB}, \quad (28)$$

where $G_{LPF}(s) = \frac{1}{1+s/(2\pi \cdot f_{LPF})}$ is the transfer function of the low-pass filter with corner frequency f_{LPF}.

Finally, expressions for gain crossover frequency f_{C1} and corresponding phase margin PM of loop gain T_{CB} in (28) are derived as

$$\left[1+\left(\frac{f_{C1}}{f_P}\right)^2\right] \cdot \left[1+\left(\frac{f_{C1}}{f_{LPF}}\right)^2\right] = \left[\frac{V_{ABP} \cdot K_{CB}}{2 \cdot R_{TOTAL}}\right]^2 \quad (29)$$

$$PM = \pi - \tan^{-1}\left(\frac{f_{C1}}{f_P}\right) - \tan^{-1}\left(\frac{f_{C1}}{f_{LPF}}\right) \quad (30)$$

Equations (26), (29), and (30) provide the basis for the design of the current-balancing loop. Namely, for the specified values of steady-state accuracy I_P^{dc} and phase margin PM and given power-stage parameters f_P, V_{ABP}, and R_{TOTAL}, loop bandwidth f_{C1} and corresponding controller gain K_{CB} can be determined from (26) and (29)-(30).

IV. Experimental Evaluation

The performance of the proposed transformer flux-balancing control was evaluated on an experimental 3.3-kW, 35-kHz DAB converter prototype designed to provide energy exchange between 395-V source V_1 and source V_2 which has 240~430V range. IKW40N65F5 IGBTs were employed for the primary and secondary switches. Inductor L_{AC} was built with PQ50/50 core and its inductance was 82 µH. The transformer was built with ETD59 core and had turns ratio N_P/N_S =34:30 and secondary-side magnetizing inductance L_M = 1.9 mH. The sum of measured total resistance of transformer windings and estimated resistive component of IGBT device voltage drop was $R_{TOTAL} = 0.21\ \Omega$. The banks of three paralleled 470µF /450-V aluminum capacitors were used on the input and the output side. Selected values of control gains K_{FB} and K_{CB} of the flux- and current-balancing loops were 0.21 A^{-1} and 0.12 A^{-1}, respectively. For this selection of control gains, the calculated flux-balancing loop bandwidth is f_C=4.13 kHz with PM=47° and GM=8.2 dB stability margins, whereas the calculated bandwidth of the current-balancing loop is f_{C1}=62 Hz with PM=81° and GM=35.6 dB stability margins. The controller was implemented by TI TMS320F28027 DSP. Experimental data was collected when the prototype was operating with 98-% nominal values of the primary and the secondary duty cycles.

To test the proposed control, transformer volt-second imbalance was introduced as -1% mismatch of duty cycles D_{PP} and D_{PN} on the primary side and +1% mismatch of duty cycles D_{SP} and D_{SN} on the secondary side. Figure 12(a) shows measured waveforms of bridge voltages V_{AB} and V_{CD} and transformer currents i_P and i_S

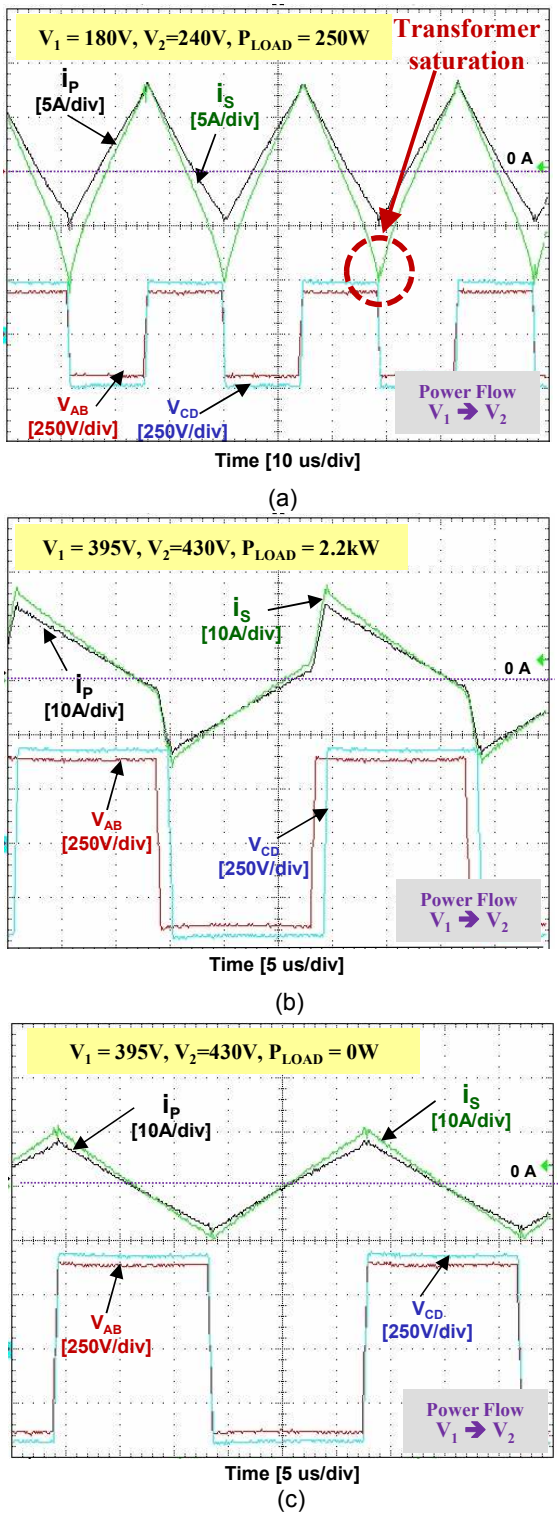


Fig. 12 Measured waveforms (a) without flux- and current-balancing controls; (b) and (c) with balancing controls.

without flux- and current-balancing controls. The measured -1.71A dc value of the magnetizing current exceeds the calculated -1.27A value corresponding to the transformer saturation onset. The negative peaks of the secondary current waveform clearly indicate saturation of the transformer core. The waveforms in

TABLE II. MEASURED DC VALUES OF TRANSFORMER CURRENTS AT VARIOUS OPERATING POINTS.

Energy Transfer	Voltage V_1 [V]	Voltage V_2 [V]	Load Power [kW]	Dc primary current [mA]	Dc secondary current [mA]	Dc magnetizing current [mA]	Saturating value of dc magnetizing current [mA]
$V_1 \rightarrow V_2$	395	240	0	170	180	11	1120
			2.2	190	220	4	
		430	0	310	410	-52	500
			2.2	340	520	-119	
$V_2 \rightarrow V_1$	395	240	0	280	350	-29	1120
			2.2	250	330	-41	
		430	0	260	370	-66	500
			2.2	200	300	-65	

Figs. 12(b)-(c) were taken with flux-balancing and current-balancing loops activated during energy transfer from source V_1 to V_2. The waveforms in Figs. 12(b) and (c) were taken at high load and no load condition, respectively. As can be seen from Figs. 12(b) and (c), with activated balancing loops, transformer saturation is eliminated.

The measured dc values of transformer currents along with the calculated values of the magnetizing current, corresponding to the transformer saturation onset, are summarized in Table II. Table II contains the data for both directions of power transfer. The data in the table indicate that the proposed balancing control effectively keeps the transformer far from the saturation region while maintaining low dc values of the primary and secondary currents.

V. SUMMARY

The paper proposed a novel flux-balancing method for the dual-active-bridge bidirectional converter based on direct control of the magnetizing current. In the proposed method, the dc components of the primary and secondary current are controlled by two feedback loops. The objective of the first loop is to maintain the average magnetizing current at approximately zero level, whereas the purpose of the other loop is to keep the average primary and secondary currents close to zero. To be effective in preventing transformer saturation, the flux-balancing loop that keeps the average magnetizing current to approximately zero must be very fast. To avoid interactions between the loops, the current-balancing-loop bandwidth should be designed much lower with respect to the flux-balancing loop bandwidth. The dynamic models for the flux- and current-balancing loops were developed and applied to loop design. The performance of the proposed current balancing controls was experimentally evaluated on the 3.3-kW, 35-kHz DAB converter prototype.

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