Novel Tunnel-Contact-Controlled IGZO Thin-Film Transistors with High Tolerance to Geometrical Variability

Radu A. Sporea, Kham M. Niang, Andrew J. Flewitt and S. Ravi P. Silva*

Dr. Radu A. Sporea, Prof. S. Ravi P. Silva

Advanced Technology Institute, Department of Electrical and Electronic Engineering, University of Surrey, Guildford GU2 7XH, United Kingdom.
E-mail: r.a.sporea@surrey.ac.uk

Dr. Kham M. Niang, Prof. Andrew J. Flewitt

Electrical Engineering Division, Department of Engineering, Cambridge University, 9 JJ Thomson Avenue, Cambridge CB3 0FA, United Kingdom.

Keywords: tunnel barriers, thin-film transistors, source-gated transistors, IGZO, amorphous oxide semiconductors.

For the first time, thin insulating layers are used to modulate a depletion region at the source of a thin-film transistor. Bottom contact, staggered electrode transistors fabricated using RF-sputtered IGZO as the channel layer, with a 3 nm ALD Al_2O_3 layer between the semiconductor and Ni source-drain contacts show behaviours typical of source-gated transistors (SGTs): low saturation voltage (V_{D_SAT} ~ 3V), change in V_{D_SAT} with gate voltage of only 0.12 V/V and flat saturated output characteristics (small dependence of drain current on drain voltage). The transistors show high tolerance to geometry variations: saturated current changes only 0.15× for channel lengths between 2 - 50 μm, and only 2× for source-gate overlaps between 9 - 45 μm. A higher than expected (5×) increase in drain current for a 30K change in temperature, similar to Schottky-contact SGTs, underlines a more complex device operation than previously theorised. Optimizations for increasing intrinsic gain and reducing temperature effects are discussed. These devices complete the portfolio of contact-controlled transistors, comprising devices with: Schottky contacts, bulk barrier or heterojunctions, and now, tunnelling insulating layers. The findings should also apply to nanowire transistors, leading to new low-power, robust design approaches as large-scale fabrication techniques with sub-nanometre control mature.

Rapid advances in high-rate large-area fabrication techniques [1–4] are enabling new ways of realising electronic devices. Along with a number of groups, we believe that revolutionary transistor design[5–9] presents opportunities that are inaccessible to evolutionary developments, in terms of energy efficiency, gain, and large-area manufacturability. To this end, we propose thin-film transistors (TFTs) inspired by the principle of deliberately using blocking contacts. Significant application benefits, e.g. tolerance to manufacturing variability and superior gain at low drain-source voltages, can be derived using engineered potential barriers at the source of thin-film staggered-electrode transistors. Such structures, known as Source-Gated Transistors (SGT) have been proposed in numerous material systems[10–15] and are an attractive alternative to conventional device structures due to their potential for ultra-low power and robust operation[16–19]. As the current in these SGT structures is controlled by the source barrier region, the device operating speed is usually close to an order of magnitude lower than conventional transistors of identical geometry. If ionic oxide semiconductors are used as active layers, high performance can still be achieved due to the material's intrinsic carrier mobility, which is more than an order higher than amorphous silicon.[20] Moreover, the SGT can be more aggressively scaled without deteriorating its electrical characteristics[16,19].

The role of the barrier at the source is twofold: it induces saturation of drain current at low drain voltage[11,21,22], and pins the potential at the edge of the source to a value dependent on gate voltage. Consequently, the injection of charge from the bulk of the source electrode is by processes which result in low activation energy[21,23] and high intrinsic gain[16,18,19,24]. The barrier at the source of a SGT device is typically realised by a Schottky contact, but it is also possible to realise a similar effect by other means [24,25][26].

Nanometre and sub-nanometre scale conducting or semiconducting layers, such as graphene[40], CNT[43], $TiSi_x$[29], have been used at the contacts of TFTs[27–31], for gaining a better ohmic behaviour[44] or tunnelling behaviour [40,41]. Likewise, nanometre scale insulating layers also have been widely used as the gate insulators for deep-sub-micron transistors and memory devices based on floating-gate principles[32,33]. Moreover, these insulting films have also been used as contact barriers against dopant diffusion to reduce short-channel effects of polysilicon TFTs [34], and to allow depinning of the Fermi level at the metal-semiconductor interface for higher drain current[35–41]. The choice of insulator is responsible for the efficiency of charge transport across the contact[42]. Multiple insulating layers can be used to create a dipole which further contributes to barrier lowering, and similar techniques are applicable for organic devices[43].

The application of a thin insulating film at the source contact in SGTs had been theorised over a decade ago. Such tunnel-contact devices are predicted to have smaller temperature coefficient than Schottky-contact devices[24]. (In this communication, metal-insulator-semiconductor contacts whose properties would change from rectifying to ohmic in the absence of the thin insulating interlayer will be referred to as tunnel contacts.) However, tunnel-contact SGTs have not been explored experimentally thus far. Combining indium gallium zinc oxide (IGZO), a leading amorphous oxide semiconductor, at the channel, with aluminium oxide (Al_2O_3) thin layers at the source and drain contacts, we report on the first tunnel-contact oxide SGTs that exhibit low-voltage saturation for energy efficiency, and tolerance to geometrical variations for robust operation in large-area circuits. To our knowledge, this is the first use of thin insulators at the contacts to deliberately induce an energy barrier leading to the effects described above. While the challenges of accurate large-area deposition of nanometre-scale films at a practical cost cannot be overlooked, large-area

manufacturing techniques for such films are becoming increasingly viable[1,44] allowing the integration of the proposed devices into conventional manufacturing flows.

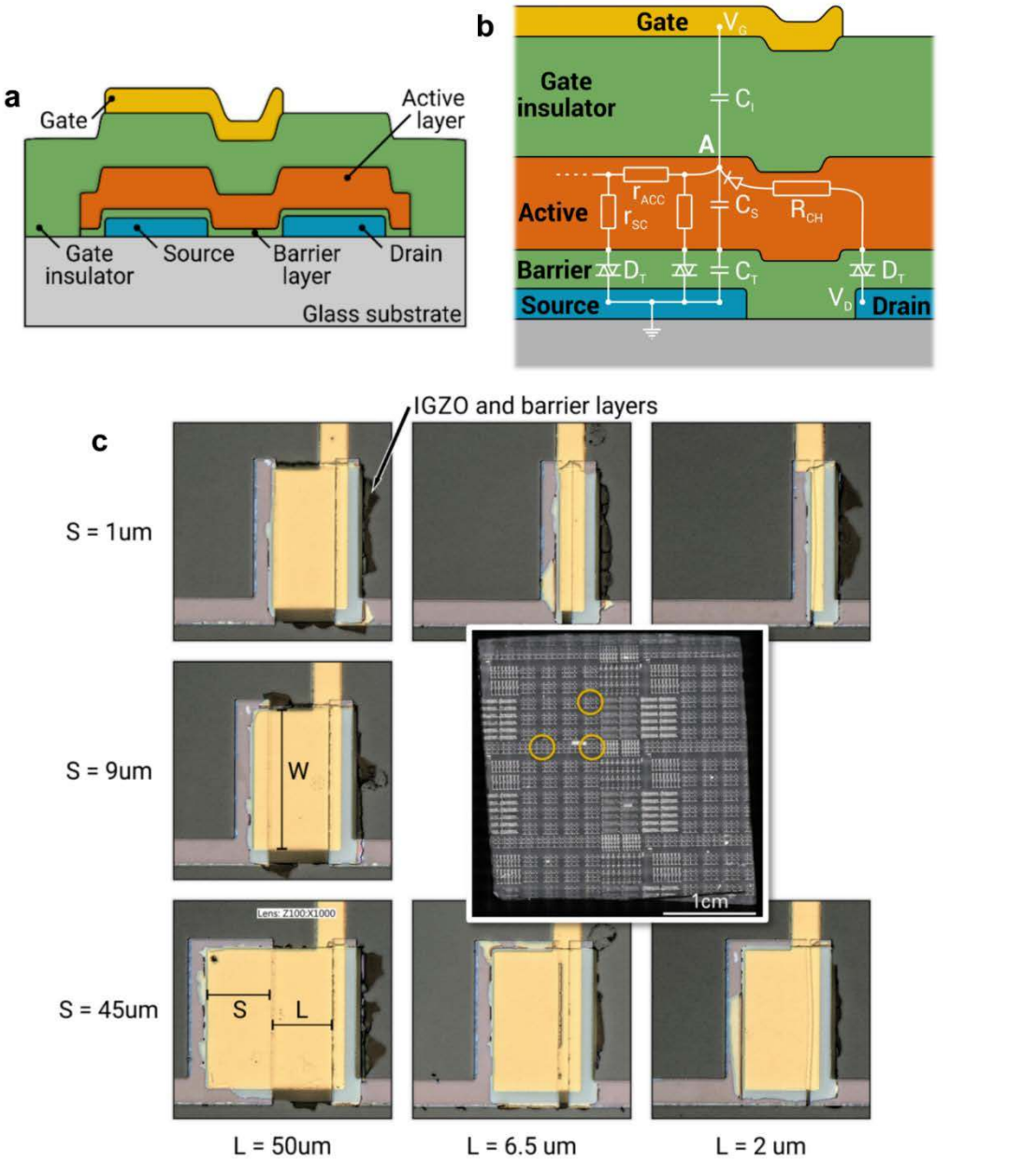

Figure 1. a) Schematic device cross-section of the Tunnel Contact Source-Gated Transistor, showing the staggered-electrode configuration with the gate overlapping the source, and the barrier layer interposed between the source/drain contacts and the semiconductor to engineer the potential barrier. b) Detailed conceptual cross-section illustrating the equivalent electrical model of the important regions of the device. c) Micrographs of typical fabricated devices with various source lengths (S) and source-drain gaps (L). Device width W = 110 µm. Devices with S = 9µm and L = 6.5 µm and 2 µm were damaged at the end of the measurement procedure and were not included in the figure.

Devices were fabricated in a top-gate, bottom-contact architecture using standard photolithography and were operated in a common-source configuration. **Figure 1**a shows the

schematic cross-section including the two main features of SGTs: (i) a thin barrier layer of Al_2O_3 deposited by atomic layer deposition which acts as a barrier between the IGZO channel and Ni source/drain electrodes, and (ii) the gate extending over the source electrode (source-gate overlap, S) in addition to covering the channel region as in the conventional TFTs. Figure 1b focuses on the region of interest at the source and illustrates the device's equivalent circuit which will be discussed later. Figure 1c shows the typical device layout with large variation of source-gate overlap, S (1, 9 and 45 μm), and source-drain gap, L (2, 6.5 and 50 μm). The substrate photograph is also shown in Figure 1 c. The width, W, of all devices was 110 μm. Several devices with S = 9 μm were tested to breakdown, and their micrographs can be found in **Figure S1** (Supporting Information).

Plots in **Figure 2** confirm that the fabricated devices here operate, in the first order, as SGTs. Figure 2a and b show that the drain current I_D only doubles when S is increased fivefold[45]. Next, as shown in Figure 2 b and c, I_D increases very little, only 0.15×, when L is increased 25×. These are consistent with the properties of SGTs that the device is controlled by the source region (S) and is less sensitive to L [20,48,49]. This is an advantage over conventional TFTs where the drain current is affected by the shorter channel and thus is susceptible to device-to-device fluctuations due to fabrication variability[46,47]. Moreover, Figure 2b and c show that the devices with longer channel has a higher saturated current than those with shorter channel, which is the opposite of what is observed in a traditional TFT. This is attributed to the 2-D potential distribution in the semiconductor owing to the staggered-electrode structure. This unusual effect has also been observed in other material systems[45,48]. The output characteristics in Figure 2 (a-c) show low saturation voltage, V_{D_SAT}, around 3 ± 1 V. It is noted that the V_{D_SAT} is similar for all S and L. The change in V_{D_SAT} with gate voltage extracted from these plots, 0.12 V/V, is also independent on S and L (see Figure 2d and e).

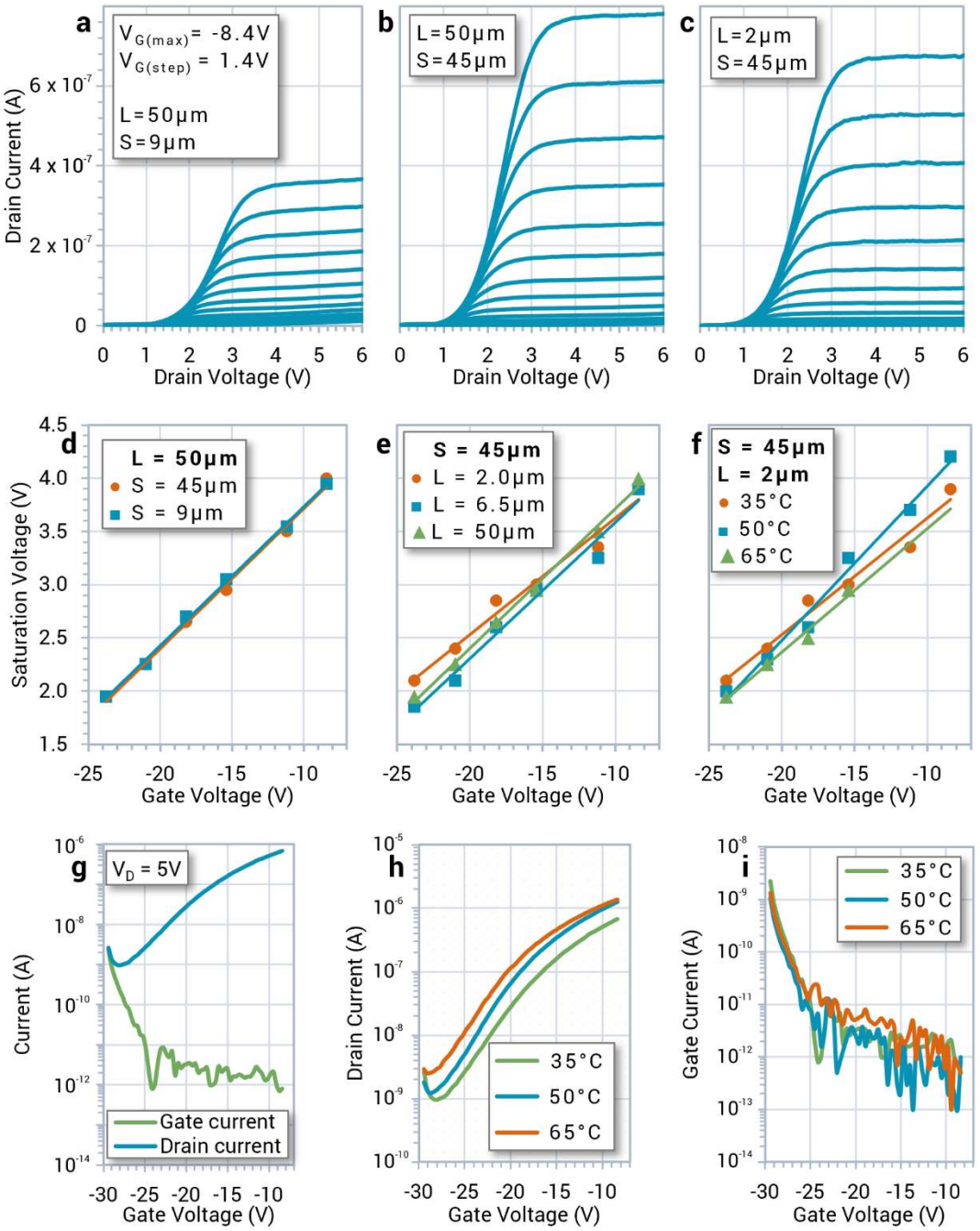

Figure 2. a-c) typical output characteristics for devices with barrier layer thickness t_t = 3 nm, demonstrating SGT behavior: low voltage saturation; flat saturated characteristics; minimal dependence of saturated current on L; dependence of drain current on source length S; current crowding at low V_D due to contact effects. d-f) The dependence of saturation voltage on gate voltage does not change significantly with geometry or temperature. g) Transfer curves show a negative threshold and gate leakage dominates transistor off current at high reverse gate voltage; h) Transfer characteristics show moderate temperature dependence. i) Gate leakage depends weakly on temperature.

Moreover, Figure 2 a – c shows very flat output curves indicating a low drain voltage

dependence in saturation. Conversely, devices fabricated without the thin insulating layer

show poor saturation as well as a much more negative threshold voltage (See Figure S2 in Supporting Information).

Next, Figure 2g reveals a large negative threshold voltage, and in the off state, gate leakage becomes the dominant proportion of drain current, as a large potential difference, as high as 30-36V is applied between the accumulation layer in the semiconductor and the gate electrode, across the <100nm gate insulator. The depletion-mode, normally-on operation of the device indicates a channel conductivity much higher than would be ideal. The deposited IGZO films have a carrier concentration ~ 10^{19} cm^{-3} with Hall mobility ~10 cm^2/V-s and they have been previously incorporated as the active layer in bottom gate TFTs [49]. However, as shown in this work, these films become too conductive when used in top gate transistors. Several causes for this behaviour are plausible, most likely linked to the condition under which the semiconductor-insulator interface, critical to device behavior, forms. The ALD growth step for the Al_2O_3 gate insulator requires subjecting the already-deposited IGZO layer to vacuum as well as chemical precursors which may change the properites of the surface. Most notably, this can result in the formation of indium nanoparticles[50] and/or the adsorption of OH^- at the surface of the semiconductor, with the net effect of increasing the conductivity of the IGZO layer at this interface. Inserting a barrier SiO_2 layer between IGZO and ALD Al_2O_3 [51] would certainly improve the device operation. This initial study was not intended to optimize transistor characteristics, and transfer curves are secondary to the device operation in SGTs. Moreover, recent studies have shown: that contact-controlled, source-gated transistors can be reliably made even with semimetals[19], with the requirement that the active layer geometry and contact barriers are optimized; and that contact engineering can be reliably used to switch off devices with highly conductive semiconductor layers[52]. In the present case this is evident when comparing transfer characteristics of devices with contact tunnelling layers (Figure 2g) with those of devices with conventional, ohmic metal-semiconductor contacts (Figure S2, Supporting Information): the presence of the contact barrier produces significantly

larger current modulation as the device is turned off. Large negative gate voltages are still required to turn off the devices, and this has an adverse effect on the off-current, as the gate leakage sharply increases below $V_G = -25V$. Transfer curves showing the impact of geometry, as well as an analysis of gate leakage current, are found in **Figure** S3 (Supporting Information). The gate leakage is largely unaffected by source area, yet the long channel device produces a noticeably larger leakage current. This may be linked to the fact that in source-gated transistors, most of the applied drain-source voltage is dropped on the source depletion region, enabling the channel to be biased at close to V_D over its whole length[53]. A longer channel results increasing the area over which a large potential difference is seen across the gate insulator, augmenting gate leakage at high absolute values of V_G.

The device operation and the influence of the various equivalent components in different biasing conditions is exemplified by the qualitative band diagram and the schematic circuit diagram presented in **Figure 3** and Figure 1b, respectively. Under no applied bias, as shown in the horizontal and vertical cross section of device in the top left and bottom left panels, the thin insulating layer between the metallic electrodes and the semiconductor effectively create blocking contacts. Applying a positive gate bias and a small positive V_D result in the band bending (top middle panel) and the flow of a small drain current, whose magnitude will be controlled by the applied drain bias and its distribution across the two contact barriers and semiconductor layer. As shown in Figure 1b, when a potential is applied across the source and drain tunnel barriers, D_T, an accumulation layer is formed at the semiconductor-gate insulator interfaces, with resistance, R_{CH}, in the gap between the source and the drain, with an incremental resistance (i.e. per unit length of the accumulation layer in the x direction), r_{ACC}. The drain current saturates at a drain voltage, V_{D_SAT}, which, for the tunnel-contact SGTs, can be defined as $(C_i / (C_i + C_T + C_s))\ (V_G - V_T) + k$ where C_i, C_S and C_T are the capacitances for

the gate insulator, the depleted semiconductor, and the tunnel layer respectively, $V_G - V_T$ is the effective applied gate voltage and k is a material-dependent constant.

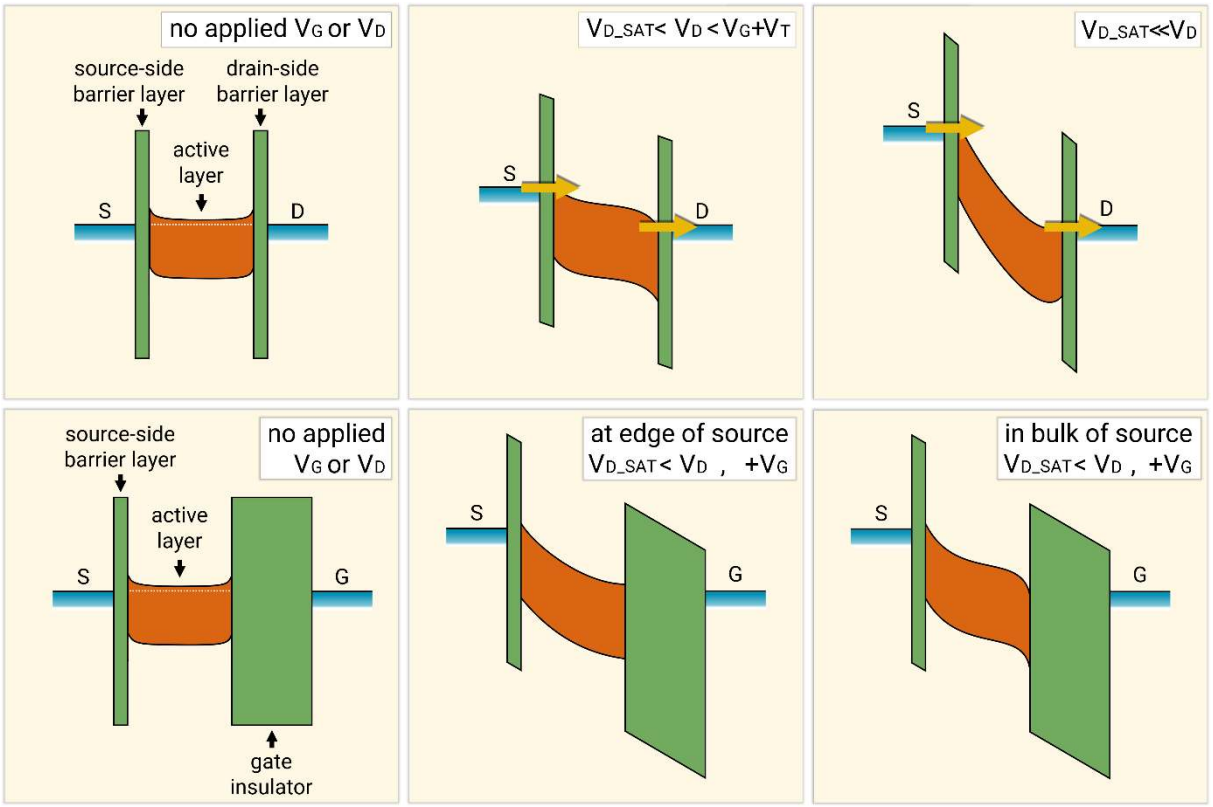

Figure 3. Conceptual band diagrams for the source-drain current path (top) and the vertical current-control structure between the source and the gate (bottom), in normal operation. Drain bias is required to overcome both the reverse-biased source barrier and the forward biased drain barrier, to obtain significant drain current. At the edge of the source, applied drain voltage reverse-biases the source barrier and a depletion layer forms at the semiconductor-insulator interface. In the bulk of the source, an accumulation layer is induced at the same interface by the gate potential acting across the gate insulator.

When the drain-source bias exceeds V_{D_SAT}, the semiconductor layer pinches off at the edge of the source closest to the drain (point *A* in Figure 1b)[10,11,21] due to an expanding depletion region in an effectively reverse-biased source-barrier layer semiconductor junction. This condition is illustrated by the band bending at the interface of active layer and gate insulator in the bottom middle panel of Figure 3. It has been previously observed that the semiconductor can be fully depleted close to the source[54,55], a phenomenon which allows for hot electron generation and transport at high effective mobility above the conduction band edge states to the drain[56]. Between point *A* and the edge of the source, the existence of a

potential division across the capacitances C_S and C_T, results in the majority of V_{D_SAT} being dropped across the depleted semiconductor as $C_S << C_T$, indicating a high-field operation. Since only a small proportion of V_{D_SAT} is dropped across the tunnel diode, we expect its I-V characteristics to control the current. Here, the current injected from the edge of the source into the depletion region dominates and this is conventionally defined in SGTs as mode I operation[21].

In the bulk area of the source which is overlapped by the gate (Figure 1a), however, the insulator interface is accumulated due to the applied gate potential. This condition is illustrated by the band bending at the interface of the active layer and the gate insulator in the bottom right panel in Figure 3. This accumulation layer is essential for charge transport from the bulk of the source towards the drain through a distributed resistor network which accounts for the accumulation layer resistivity, r_{ACC}, semiconductor layer resistivity, r_{SC}, and diodes, D_T (Figure 1 b).[11,19,21,33] Here, the current injected from the bulk of the source dominates and this is conventionally defined in SGTs as mode II operation[21] . Crucial for the operation of the device is a relatively low value of r_{SC}, which results in a significant proportion of the accumulation layer potential being applied to the thin barrier, making it able to sustain a large current density. However, Al_2O_3[57,58] and SiO_2[59,60] films of 2 – 3 nm thickness can tolerate significantly higher current density than that observed for the present devices, for applied potentials in the range of a few volts. Thus, we conclude that in the bulk of the source, the tunnel layer is effectively transparent, and the current injected from the bulk of the source is controlled by the resistive network described in Figure 1b, which is dominated by the vertical resistance of the semiconductor layer pinned at voltage V_{D_SAT} at point *A*.

Having described the device operation, the performance of the fabricated devices are further examined for their SGT properties. For $V_D < V_{D\_SAT}$, the semiconductor is not pinched off at

point *A*, and the current injected from the source obeys the I-V characteristic of the source barrier, hence the s-shape of the output curves at low V_D (Figure 2 a-c). To illustrate this behaviour further, we plot families of output curves from three devices with different source lengths (1, 9 and 45 μm) in **Figure 4**a, on a semilogarithmic scale to account for the difference in drain current magnitude.

An exponential dependence is observed at low V_D, indicating turn-on of the contact barrier as the potential is increased. While somewhat detrimental to the speed of logic circuits, the sub-linear output curves at low V_D is of no consequence in analog designs which typically operate in saturation. Of note in Figure 4a is also the independence of V_{D_SAT} on S for a given V_G. This behaviour is explained by the pinch-off mechanism which involves exclusively the edge of the source. Moreover, the S = 1 μm device injects only in Mode I and the potential across the tunnel barrier is small, hence a low current is produced. In longer S devices, Mode II injection with much higher current dominates, and a low contribution from the far side of the very long source due to the resulting resistive voltage drop results in minimal dependence of I_D on S [21,45,53] (see also Figure 1b).

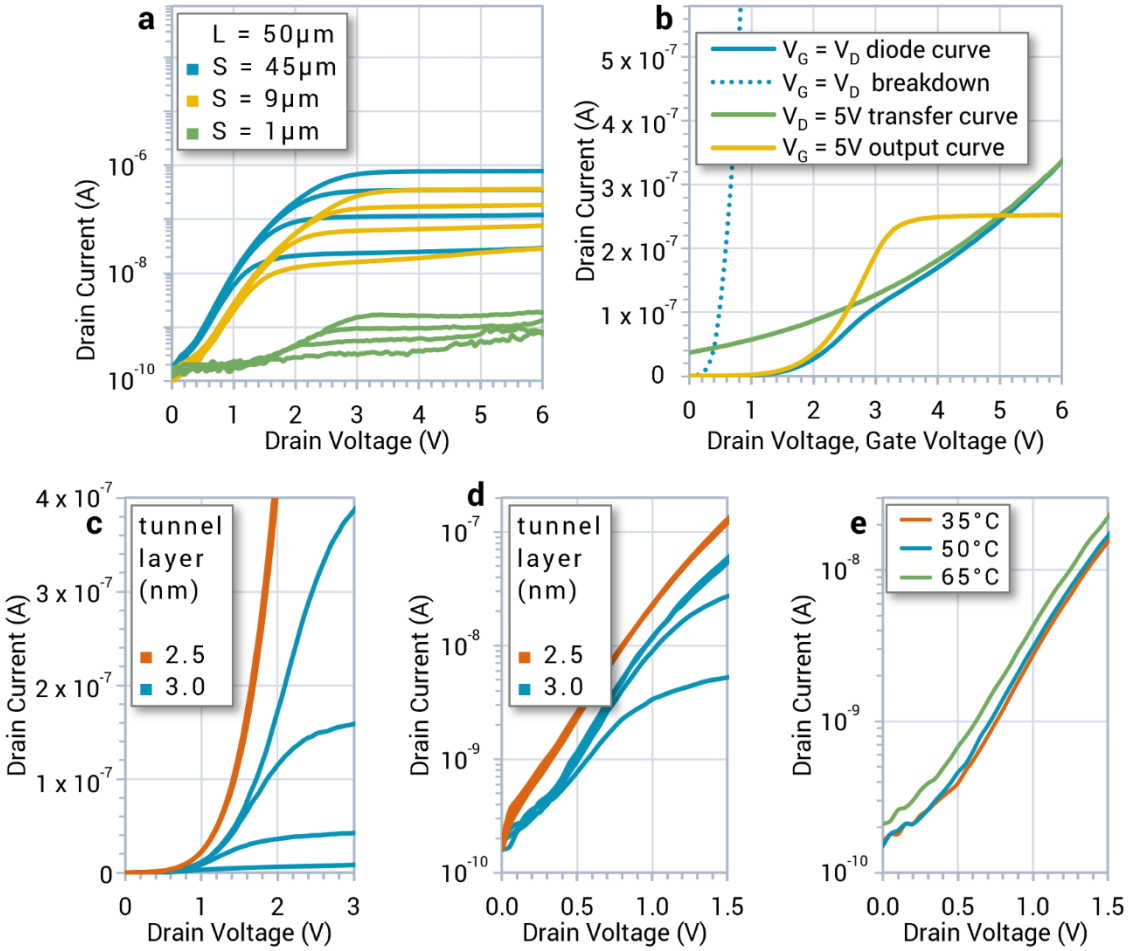

Figure 4. a) Output characteristics show dramatic changes in drain current with source length (S), as injection area varies, however the saturation voltage is similar for a given gate voltage (V_G = –8.4, –12.6, –16.8, –21 V) irrespective of current level. b) Output (I_D vs V_D), transfer (I_D vs V_G), and diode (I_D vs $V_G = V_D$) characteristics for a single device (L = 6.5 µm, S = 9 µm) at 35°C, revealing the dominant current regulating process; also shown (dotted line) is the diode characteristic after the destructive breakdown of the tunnel dielectric at the contacts through application of V_D > 8V. c-d) Output curves show a diode-like exponential behaviour at low voltage, and the current increases when a thinner tunnel dielectric is used. e) Low-V_D drain current depends weakly on temperature.

As previously shown in Figure 2, the output curves show the typical 'current crowding' non-linear low-voltage behaviour of forward biased non-ohmic contacts, which have been reported in numerous devices, e.g.[61]. Interestingly, the diode-like characteristic observed at low V_D shows a very small dependence on V_G. Figure 4b shows the sub-linear I-V characteristics at low V_D. Here we plot on the same graph the output (I_D vs V_D, V_G fixed), transfer (I_D vs V_G, V_D fixed), and diode (I_D vs $V_G = V_D$) characteristics, where the fixed potential is 5V, relative to the source. We can see that the diode characteristic follows the transfer curve at high

voltage, and the output curve at low voltage, indicating that the low-voltage drain current is exclusively controlled by the applied drain bias and is independent of gate bias. This effect is seen in all the families of curves in Figures 2 a-c, in which, before saturation, the plot follows the same envelope, linked to the capability of the source barrier to deliver current at a given bias.

To conclude the discussion relating to Figure 4b, we examine the diode curve obtained for the same device after being subjected to V_D > 8V (dotted line). This high voltage leads to permanent failure of the barrier layer, at values consistent with measurements on MIM structures[62] (see **Figure S4** in Supporting Information). The result is a behaviour closer to that of ohmic contacts, and is attributed to dielectric breakdown at the edge of the source, removing the possibility of pinch-off at point *A* (Figure 1b). It is reasonable to assume that, given the relative sizes of source and drain contacts, a similar barrier layer failure occurs at the drain contact.

A characteristic of Schottky-barrier SGTs is their ability to produce large intrinsic gain, $A_V = g_m / g_o$ due to the very low g_o which can be obtained with suitable device optimization, where $g_m = dI_D / dV_G$ is transconductance, and $g_o = dI_D / dV_D$ is output conductance. Intrinsic gain as high as ~ 85 for a-Si Schottky-barrier SGTs [63] and over 1,000 for polysilicon Schottky-barrier SGTs [16] has been reported. Here, the intrinsic gain is a modest ≈ 20. This can be improved by reducing both the gate insulator and semiconductor thicknesses, thereby increasing g_m. g_o is small but non-negligible in the operating range of V_G (Figure 2 a-c), although at very high gate bias, these transistors show negative g_o due to the two-dimensional potential distribution in the semiconductor[48]. It follows that, for a limited span of V_G, a very low g_o could be achieved. g_o may be further improved by field relief strategies, such as a source-metal overhang [12,13].

For the present devices, we can calculate $\gamma \equiv C_i / (C_i + C_T + C_s) = 0.23$ (V/V), which is much smaller than the value of unity specific to conventional FETs, but significantly larger than the measured $dV_{D\_SAT} / dV_G = 0.12$ (Figure 2 d-f)[16,63]. In Schottky barrier SGTs, the measured value is often larger than the calculated value, especially when the pinch-off at point *A* is weak due to either a low Schottky barrier height, or an inability to easily deplete the semiconductor-insulator interface due to fabrication practicalities. In the case of tunnel-contact SGTs shown here, the cause for the unusually low measured value is likely to be linked to the turn-on characteristic of the source diode and the resulting shape of the output characteristic. In practice, the curves saturate not when the calculated V_{D_SAT} is reached, but rather at the bias condition at which the resistive network in the source area of the semiconductor begins limiting the current, as opposed to the source diode (Figure 1b). Designing the devices with no tunnel layer at the drain contact and with thinner source tunnel layer should diminish the s-shape of the output curves and result in better agreement between measured (dV_{D_SAT} / dV_G) and theoretical (γ) values.

Devices with thinner, 2.5 nm barrier layers were also fabricated, and the output characteristics are compared in Figure 4 c and d. For both barrier layer thicknesses, we see the same behaviour of the exponential current at low V_D, and its independence of gate bias. The use of a thicker barrier layer reduces the drain current only by half, indicating that direct tunnelling may not be the principal charge injection mechanism. This is consistent with the model proposed in Figure 1b.

Figure 4e illustrates a comparatively high dependence on temperature of the current injected across the 3 nm barrier for the same low drain voltages (i.e. the current doubles for a 30 K temperature increase), which is again inconsistent with direct tunnelling at the contact. These results suggest the presence of an effective potential barrier at the contact that is reduced by

the applied bias (Figure 3). Likewise, the transfer curves in Figure 2h show an approximately five-fold increase of drain current upon a 30 K increase in temperature. The gate leakage current less than doubles with a 30 K increase in temperature (Figure 2i). This further supports our stated hypothesis that barrier-layer tunnelling is not the principal current control mechanism in these devices, as it would result in a very low temperature dependence. A space charge induced tunneling model coupled with ohmic transport in the semiconductor would be a plausible explanation of the observed characteristics.

To put the characteristics of the proposed devices in context, we refer to **Table 1**, which synthesises the structural differences and their impact on electrical behaviour for contact-controlled devices with: Schottky barriers[10] (traditional SGT), bulk or heterostructure barriers[25,26], and the proposed tunnel barriers. Choosing the most suitable design will depend in equal measure on the application and on the practicalities of fabrication (e.g. ability to produce reliable nanoscale contact barrier layers on a large area for the tunnel devices, or solvent orthogonality for solution-processed heterojunction-barrier devices). We highlight two important differences to conventional (ohmic-contact) TFTs: first, the temperature coefficient of drain current can vary dramatically based on the choice of source barrier and dominant injection mode; second, source area is an important design parameter in all three types of devices.

In conclusion, contact-controlled IGZO SGTs were fabricated and characterized. For the first time, pinch-off at the source was induced by interposing a nm-scale Al_2O_3 layer between the Ni source and drain contacts and the semiconductor. These devices behave qualitatively as source-gated transistors, with low saturation voltage, flat output characteristics, and tolerance against geometrical variations affecting the current flow. The behaviour of the fabricated devices deviates from the theory of Shannon and Balon[24], due to the significantly more

complex, two-dimensional injection and transport processes governing these devices, in contrast to a one-dimensional tunnel diode: the current is not limited by the tunnelling capability of the thin insulating layer at the contact, but by the electrostatics of the semiconductor layer in the source region, potentially with some assistance from the work function difference between the metal contact and the semiconductor.

Table 1. Structural and electrical characteristics of source-gated transistors with different barrier types. t_i – insulator thickness, t_s – semiconductor thickness, t_t – tunnel insulator layer thickness, ε_i – insulator permittivity, ε_s – semiconductor permittivity, S – length of source contact overlapped by the gate, ϕ_{B0} – effective zero-bias Schottky barrier height at the source contact, t_d – doped barrier layer thickness, x_d – extension of doped layer over the edge of the source contact into the source-drain gap , N_D – doping concentration in the doped barrier layer.

Parameter	Tunnel-barrier SGT (TSGT)	Schottky-barrier SGT (SBSGT)	Bulk-barrier and heterostructure SGT (BUSGT)
Barrier realized by	Thin insulating layer at source contact	Choice of source contact metal	Doping or heterostructure formation
Effective barrier height range	High	Low	High
Control over effective height of barrier	Difficult	Moderate	Moderate
Off-current	Low	Low	Low
On-current	Moderate	Low	High
Transconductance	Moderate	Low	High
Output conductance	Low (with field relief)	Very low (with field relief)	Potentially low (with field relief)
Temperature coefficient of drain current	Low	Moderate	Potentially low
Threshold tuning	Bulk semiconductor doping, gate work function	Bulk semiconductor doping, gate work function	Doped layer parameters, gate work function
Principal design parameters	t_i, t_s, t_t, ε_i, ε_s, S	t_i, t_s, ε_i, ε_s, S, ϕ_{B0}	t_i, t_s, ε_i, ε_s, t_d, x_d, S, N_D

As discussed above, optimisations of the channel layer and source contact area to maintain a constant potential at point A in Figure 1b, would be expected to increase the gain.[11–13] Maximizing this figure of merit improves energy efficiency and logic gate noise margin[13,18,19] and may reduce analog circuit complexity.

The suitability of such devices for high performance, high throughput thin-film electronics is supported by recent advances thin layer deposition techniques with precise control over large areas, such as atomic layer deposition. The chosen material system has several advantages: carrier mobility is superior to a-Si with potentially higher switching speed; achieving a high quality Al_2O_3 tunnel oxide / IGZO semiconductor interface is practical with current technologies; and the contact-controlled transistor on-current is robust against potential bias instability. Moreover, the potential replacement of the semiconducting layer with an atomically thin material from the transition metal dichalcogenide family (WS_2, MoS_2, etc.) would be of great interest for next generation, highly efficient electronic devices. Finally, a similar device design may be used in nanowire transistors, where deliberate growth of insulating shells should lead to source-gated behaviour, with large gain and tolerance to geometrical variations. We envisage this new architecture as a very promising opportunity for analog signal processing and biasing circuitry for low-power sensors made by low-cost and large area fabrication.

Experimental Section

Fabrication: Top-gate, bottom-contact transistors were fabricated on Corning Eagle 2000 glass (see Figure 1) by contact photolithography. The source and drain bottom contacts were defined by lift-off using AZ5214E photoresist and 55 nm Ni deposited by electron beam evaporation (custom system, Univex) at a rate of ~ 2 Å/s. A significant amount of distortion (bowing) is noticed in the channel of devices with $L = 2$ μm. This is a result of the poor adhesion of the photoresist to the substrate in that area, with negligible effect on the operation of the present devices.

Next, using the mask for the active layer, the barrier layer and the semiconductor island were defined by photolithography, in a single lift-off step: following this definition, the barrier Al_2O_3 layer was deposited by atomic layer deposition (ALD) using a Savannah 100 ALD

(Cambridge NanoTech, Inc.) at 150 °C using trimethylaluminum and deionized water for 25 and 30 cycles producing barrier layer thicknesses of 2.5 nm and 3 nm respectively. Ideally, the optimal device would have an ohmic drain contact, but this was impractical to realise and test with the current device layout and process. The active layers (35 nm IGZO) were deposited using RF magnetron sputtering from an In_2O_3:Ga_2O_3:ZnO (1:1:1) target in an argon atmosphere at a pressure of 7×10^{-3} mbar. Due to the comparatively high temperature experienced during the ALD process, the photoresist lift-off resulted in tearing of the edges of the defined patterns (Fig. 1c), well outside the active device area, but with potential bearing on device-to-device drain current uniformity.

Al_2O_3 was deposited by ALD using the same deposition condition as the barrier layers (1000 ALD cycles), achieving a thickness of 98 nm, refractive index 1.62 at λ = 633 nm) to serve as the gate insulator, and via holes were defined, then etched for ~ 5 minutes in 80% H_3PO_4 at ~ 70°C in the contact pad area.

Finally, top gate contacts and access pads for source and drain, consisting of 10 nm Ti and 80 nm Au were deposited by the same e-beam lithography technique, and defined by photolithography.

Characterization: Device characterization was performed manually, in air, on a Wentworth semiconductor prober and using the Keysight B2902A precision SMU, connected to a PC via USB. Electrical connections were made through BNC cables. The drain was connected to Channel 1, the gate to Channel 2, and the source to Channel 1 Ground. All measurement were performed with the source grounded, and all analysis and discussion implies common-source operation of the transistor. A heated chuck was used to set the substrate temperature.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

RAS acknowledges the Royal Academy of Engineering of Great Britain for the support through the Research Fellowship, Grant No. 10216/110 and EPSRC grant EP/R028559/1. KMN and AJF acknowledge the support of the Engineering and Physical Sciences Research Council (EPSRC) through project EP/M013650/1.

RAS thanks Mr Kostis Michelakis for the support during photolithographic mask design, Miss Barbara Salonikidou, Dr Brice Le Borgne and Miss Eva Bestelink for their assistance with streamlining the fabrication process, and Prof John Shannon for technical discussions.

Received: ((will be filled in by the editorial staff))

Revised: ((will be filled in by the editorial staff))

Published online: ((will be filled in by the editorial staff))

References

[1] H. C. Guo, E. Ye, Z. Li, M.-Y. Han, X. J. Loh, *Mater. Sci. Eng. C* **2017**, *70*, 1182.

[2] H.-W. Hsu, C.-L. Liu, *RSC Adv.* **2014**, *4*, 30145.

[3] J. Leppäniemi, O.-H. Huttunen, H. Majumdar, A. Alastalo, *Adv. Mater.* **2015**, *27*, 7168.

[4] C. Yilmaz, A. Sirman, A. Halder, A. Busnaina, *ACS Nano* **2017**, *11*, 7679.

[5] B. Liu, M. A. McCarthy, Y. Yoon, D. Y. Kim, Z. Wu, F. So, P. H. Holloway, J. R. Reynolds, J. Guo, A. G. Rinzler, *Adv. Mater.* **2008**, *20*, 3605.

[6] M. P. Klinger, A. Fischer, F. Kaschura, J. Widmer, B. Kheradmand-Boroujeni, F. Ellinger, K. Leo, *Sci. Rep.* **2017**, *7*, 44713.

[7] S. Lee, A. Nathan, *Science (80-.).* **2016**, *354*, 302.

[8] H. Yang, J. Heo, S. Park, H. J. Song, D. H. Seo, K.-E. Byun, P. Kim, I. Yoo, H.-J. Chung, K. Kim, *Science (80-.).* **2012**, *336*, 1140 LP.

[9] A. J. Ben-Sasson, N. Tessler, *Nano Lett.* **2012**, *12*, 4729.

[10] J. M. Shannon, E. G. Gerstner, *Solid. State. Electron.* **2004**, *48*, 1155.

[11] A. Valletta, L. Mariucci, M. Rapisarda, G. Fortunato, *J. Appl. Phys.* **2013**, *114*, 64501.

[12] R. A. Sporea, M. J. Trainor, N. D. Young, J. M. Shannon, S. R. P. Silva, *Electron Devices, IEEE Trans.* **2012**, *59*, 2180.

[13] N. Papadopoulos, F. De Roose, Y. Lai, J. van der Steen, M. Ameys, W. Dehaene, J. Genoe, K. Myny, in *2017 IEEE Cust. Integr. Circuits Conf.*, **2017**, pp. 1–4.

[14] A. M. Ma, M. Gupta, F. R. Chowdhury, M. Shen, K. Bothe, K. Shankar, Y. Tsui, D. W. Barlage, *Solid. State. Electron.* **2012**, *76*, 104.

[15] A. S. Dahiya, C. Opoku, R. A. Sporea, B. Sarvankumar, G. Poulin-Vittrant, F. Cayrel, N. Camara, D. Alquier, *Sci. Rep.* **2016**, *6*, 19232.

[16] R. A. Sporea, M. J. Trainor, N. D. Young, J. M. Shannon, S. R. P. Silva, *Electron Devices, IEEE Trans.* **2010**, *57*, 2434.

[17] R. A. Sporea, L. J. Wheeler, V. Stolojan, S. R. P. Silva, *Sci. Rep.* **2018**, *8*, 17558.

[18] R. A. Sporea, M. J. Trainor, N. D. Young, J. M. Shannon, S. R. P. Silva, *Sci. Rep.* **2014**, *4*, DOI 10.1038/srep04295http://www.nature.com/srep/2014/140306/srep04295/abs/srep04295.html#supplementary-information.

[19] J. Zhang, J. Wilson, G. Auton, Y. Wang, M. Xu, Q. Xin, A. Song, *Proc. Natl. Acad. Sci.* **2019**, 1.

[20] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, H. Hosono, *Nature* **2004**, *432*, 488.

[21] J. M. Shannon, R. A. Sporea, S. Georgakopoulos, M. Shkunov, S. R. P. Silva, *Electron Devices, IEEE Trans.* **2013**, *60*, 2444.

[22] S. D. Brotherton, *Introduction to Thin Film Transistors: Physics and Technology of TFTs*, Springer, **2013**.

[23] R. A. Sporea, M. Overy, J. M. Shannon, S. R. P. Silva, *J. Appl. Phys.* **2015**, *117*, 184502.

[24] J. M. Shannon, F. Balon, *Solid. State. Electron.* **2008**, *52*, 449.

[25] R. A. Sporea, W. Wright, J. M. Shannon, S. R. P. Silva, *ECS Trans.* **2015**, *67*, 91.

[26] R. A. Sporea, K. D. G. I. Jayawardena, M. Constantinou, M. Ritchie, A. Brewin, W. Wright, S. R. P. Silva, *ECS Trans.* **2016**, *75*, 61.

[27] L. Wang, Y. Sun, X. Zhang, L. Zhang, S. Zhang, M. Chan, *Appl. Phys. Lett.* **2017**, *110*, 152105.

[28] H.-Y. Huang, S.-J. Wang, C.-H. Wu, C.-K. Chiang, J.-Y. Su, *Appl. Phys. Lett.* **2013**, *102*, 92108.

[29] Y.-N. Z. and X. G. and C.-H. W. and J.-L. X. and S.-D. Wang, *Appl. Phys. Express* **2016**, *9*, 111601.

[30] K. Zhu, L. Wen, M. Zhang, *IEEE J. Electron Devices Soc.* **2017**, *5*, 411.

[31] D. Luo, H. Xu, M. Zhao, M. Li, M. Xu, J. Zou, H. Tao, L. Wang, J. Peng, *ACS Appl. Mater. Interfaces* **2015**, *7*, 3633.

[32] P. Punchaipetch, K. Ichikawa, Y. Uraoka, T. Fuyuki, A. Tomyo, E. Takahashi, T. Hayashi, *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct. Process. Meas. Phenom.* **2006**, *24*, 1271.

[33] C. Y. Ng, T. P. Chen, A. Du, *Phys. status solidi* **2006**, *203*, 1291.

[34] M. K. Moravvej-Farshi, M. A. Green, *IEEE Electron Device Lett.* **1987**, *8*, 165.

[35] A. M. Roy, J. Lin, K. C. Saraswat, *IEEE Electron Device Lett.* **2012**, *33*, 761.

[36] N. Tomonori, K. Koji, T. Akira, *Appl. Phys. Express* **2008**, *1*, 51406.

[37] R. R. Lieten, S. Degroote, M. Kuijk, G. Borghs, *Appl. Phys. Lett.* **2008**, *92*, 22106.

[38] P. J. King, E. Arac, S. Ganti, K. S. K. Kwa, N. Ponon, A. G. O'Neill, *Appl. Phys. Lett.* **2014**, *105*, 52101.

[39] D. Connelly, C. Faulkner, P. A. Clifton, D. E. Grupp, *Appl. Phys. Lett.* **2006**, *88*, 12105.

[40] A. Agrawal, J. Lin, M. Barth, R. White, B. Zheng, S. Chopra, S. Gupta, K. Wang, J. Gelatos, S. E. Mohney, S. Datta, *Appl. Phys. Lett.* **2014**, *104*, 112101.

[41] J. Hu, K. C. Saraswat, H. S. P. Wong, *J. Appl. Phys.* **2010**, *107*, 63712.

[42] J. Y. J. Lin, A. M. Roy, A. Nainani, Y. Sun, K. C. Saraswat, *Appl. Phys. Lett.* **2011**, *98*, 92113.

[43] B. E. Coss, W.-Y. Loh, H. Carlo Floresca, M. J. Kim, P. Majhi, R. M. Wallace, J. Kim, R. Jammy, *Appl. Phys. Lett.* **2011**, *99*, 102108.

[44] M. Bareiß, D. Kälblein, C. Jirauschek, A. Exner, I. Pavlichenko, B. Lotsch, U. Zschieschang, H. Klauk, G. Scarpa, B. Fabel, W. Porod, P. Lugli, *Appl. Phys. Lett.* **2012**, *101*, 83113.

[45] R. A. Sporea, G. Xiaojun, J. M. Shannon, S. R. P. Silva, in *Semicond. Conf. 2009. CAS 2009. Int.*, **2009**, pp. 413–416.

[46] S. C. Kim, Y. S. Kim, E. K.-H. Yu, J. Kanicki, *Solid. State. Electron.* **2015**, *111*, 67.

[47] G. Baek, K. Abe, H. Kumomi, J. Kanicki, in *2012 19th Int. Work. Act. Flatpanel Displays Devices*, **2012**, pp. 13–16.

[48] S. H. Rha, U. K. Kim, J. Jung, H. K. Kim, Y. S. Jung, E. S. Hwang, Y. J. Chung, M. Lee, J. Choi, C. S. Hwang, *IEEE Trans. Electron Devices* **2013**, *60*, 1128.

[49] A. Kiani, D. G. Hasko, W. I. Milne, A. J. Flewitt, *Appl. Phys. Lett.* **2013**, *102*, 152102.

[50] S. Hu, H. Ning, K. Lu, Z. Fang, Y. Li, R. Yao, M. Xu, L. Wang, J. Peng, X. Lu, *Nanomater.* **2018**, *8*, DOI 10.3390/nano8040197.

[51] R. Chen, W. Zhou, M. Zhang, M. Wong, H. S. Kwok, *Thin Solid Films* **2013**, *548*, 572.

[52] E. Bestelink, T. Landers, R. A. Sporea, *Appl. Phys. Lett.* **2019**, *114*, 182103.

[53] R. A. Sporea, S. R. P. Silva, in *2017 Int. Semicond. Conf.*, **2017**, pp. 155–158.

[54] G. A. J. Amaratunga, S. R. P. Silva, *Appl. Phys. Lett.* **1996**, *68*, 2529.

[55] R. D. Forrest, A. P. Burden, S. R. P. Silva, L. K. Cheah, X. Shi, *Appl. Phys. Lett.* **1998**, *73*, 3784.

[56] S. Bhattacharyya, S. J. Henley, E. Mendoza, L. Gomez-Rojas, J. Allam, S. R. P. Silva, *Nat. Mater.* **2005**, *5*, 19.

[57] D. Diesing, A. W. Hassel, M. M. Lohrengel, *Thin Solid Films* **1999**, *342*, 282.

[58] T. E. Hartman, J. S. Chivian, *Phys. Rev.* **1964**, *134*, A1094.

[59] A. Schenk, G. Heiser, *J. Appl. Phys.* **1997**, *81*, 7900.

[60] L. F. Register, E. Rosenbaum, K. Yang, *Appl. Phys. Lett.* **1999**, *74*, 457.

[61] R. Hattori, J. Shirafuji, *Japanese J. Appl. Phys. Part 1-Regular Pap. Short Notes Rev. Pap.* **1994**, *33*, 612.

[62] J. Kolodzey, E. A. Chowdhury, T. N. Adam, G. Qui, I. Rau, J. O. Olowolafe, J. S. Suehle, Y. Chen, *IEEE Trans. Electron Devices* **2000**, *47*, 121.

[63] J. M. Shannon, E. G. Gerstner, *Electron Device Lett. IEEE* **2003**, *24*, 405.

Supporting Information

Novel Tunnel-Contact-Controlled IGZO Thin-Film Transistors with High Tolerance to Geometrical Variability

Radu A. Sporea, Kham Niang, Andrew J. Flewitt and S. Ravi P. Silva*

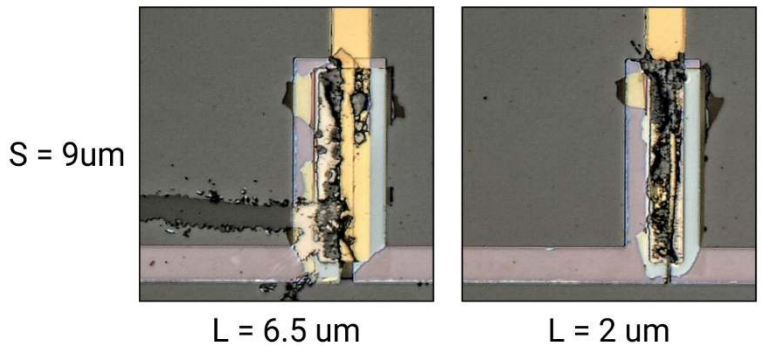

Figure S1. Two of the devices presented in the analysis failed catastrophically after electrical stress testing. We include the images of the actual devices, consistent with Figure 1c.

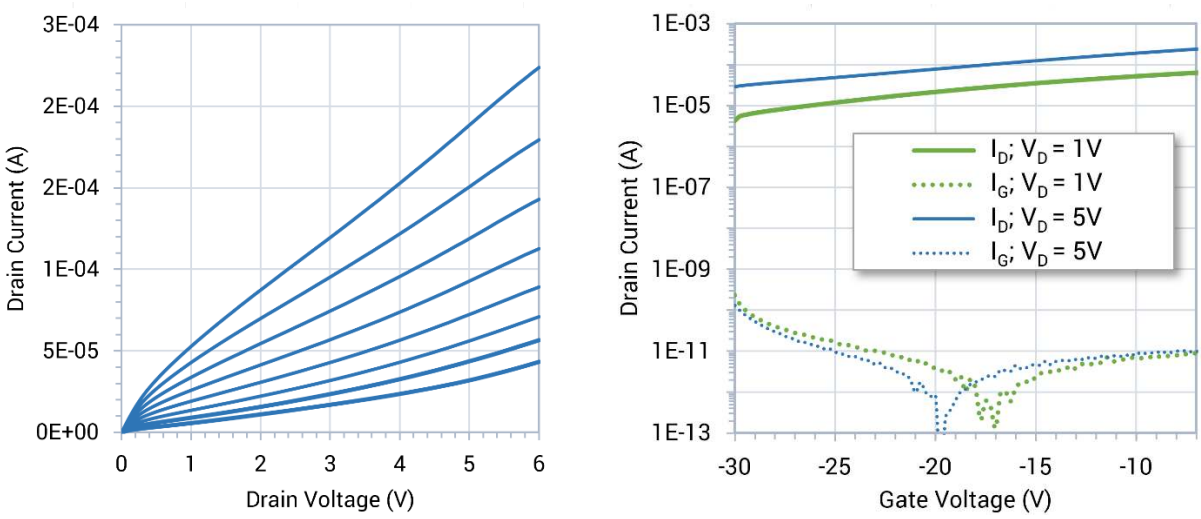

Figure S2. Output for $V_{G(min)}$ = -30V and $V_{G(step)}$ = 3V (left) and transfer (right) characteristics for devices with a similar construction to those characterised in Figure 2, but without Al_2O_3 tunnel layer. Here, S = 45 µm and L = 6.5 µm.

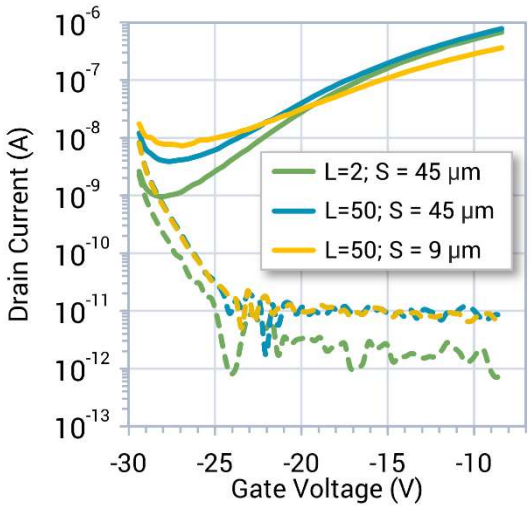

Figure S3. Transfer characteristics including drain leakage plots for three device geometries and V_{DS} = 5V. Source-drain separation, L, has no significant impact on on-current, and a shorter source, S, produces less current, both aspects consistent with SGT theory. At high negative gate voltage, off-current is dominated by gate leakage irrespective of geometry. Gate leakage is significantly reduced for the device with a short L, as a result of the decreased gate area (see left and right panels on the bottom row of Fig 1c.). The contribution from the area of the gate overlapping the source-drain gap is greater than that from the overlap with the source. The significantly lower leakage current seen for L = 2µm is due to the potential distribution in the accumulation layer at the semiconductor-gate insulator interface, in the source area and in the transistor "channel". The "channel" is practically at potential V_{DS} (in this case 5V), whereas the potential in the source region is at V_{D_SAT} (3V or less).

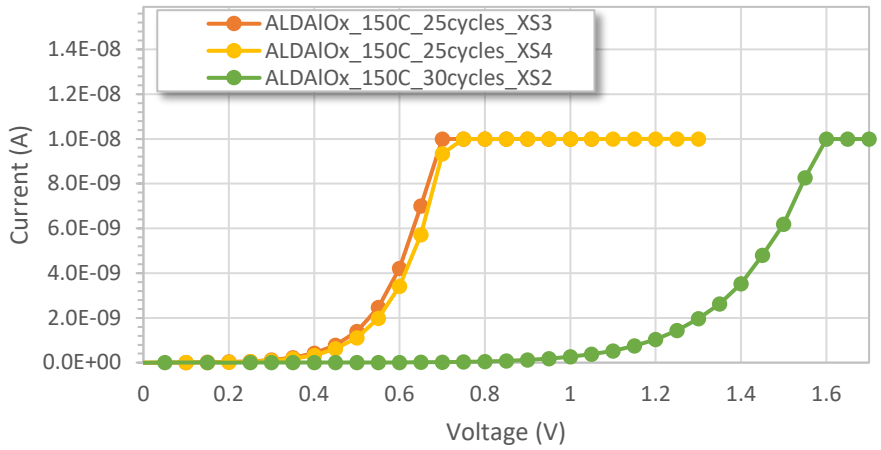

Figure S4. Dielectric breakdown measurements on the MIM capacitors (Au-Ti/barrier Al_2O_3/p^+ Si, capacitor area 1.3 × 10^{-7} m^2) showing breakdown at ~0.7V for 2.5 nm (25 ALD cycles), and ~ 1.6V for 3 nm (30 ALD cycles), consistent with literature[61].