Novel Zero-Voltage and Zero-Current-Switching Full Bridge PWM Converter Using Transformer Auxiliary Winding

Jung-Goo Cho, *Member, IEEE*, Ju-Won Baek, *Member, IEEE*, Chang-Yong Jeong, *Member, IEEE*, Dong-Wook Yoo, *Member, IEEE*, and Kee-Yeon Joe

***Abstract*—A novel zero voltage and zero current switching (ZVZCS) full bridge (FB) pulse width modulation (PWM) converter is proposed to improve the demerits of the previously presented ZVZCS-FB-PWM converters [5]–[8], such as, use of lossy components or additional active switches. A simple auxiliary circuit which includes neither lossy components nor active switches provides ZVZCS conditions to primary switches, ZVS for leading-leg switches and ZCS for lagging-leg switches. Many advantages including simple circuit topology, high efficiency, and low cost make the new converter attractive for high power (>2 kW) applications. The operation, analysis, features and design considerations are illustrated and verified on a 2.5 kW, 100 kHz insulated gate bipolar transistor (IGBT) based experimental circuit.**

***Index Terms*—insulated gate bipolar transistor, switching converter, zero current switching, zero voltage.**

I. Introduction

INSULATED gate bipolar transistors (IGBT's) are widely used in the switching power conversion applications because of their distinctive advantages such as easiness in drive and high frequency switching capability. The performance of IGBT's has been continuously improved and the latest IGBT's can be operated at 10–20 kHz without including any snubber circuit. Moreover, IGBT's are replacing metal oxide semiconductor field effect transistors (MOSFET's) for the several kilo-watts up to ten kilo-watts power range applications since IGBT's can handle higher power with higher power density and lower cost comparing to MOSFET's. The maximum operating frequency of IGBT's, however, is limited to 20–30 kHz [1] because of their tail current characteristic. To operate IGBT's at higher switching frequencies, it is required to reduce the turn-off switching loss. zero-voltage switching (ZVS) with a substantial external snubber capacitor or zero-current switching (ZCS) can be a solution. The ZCS, however, is more effective than ZVS since the minority carrier is swept out before turning off [7].

Full bridge-pulse width modulation-zero voltage switching (ZVS-FB-PWM) converters have received considerable attention in recent years [2]–[6]. This converter is controlled by phase shifted PWM technique which enables the use of all parasitic elements in the bridge to provide ZVS conditions for the switches. Distinctive advantages including ZVS with no additional components and low device voltage/current stresses make it very attractive for high-frequency, high-power applications where MOSFET's are predominantly used as the power switches. The IGBT's, however, are not suited for the ZVS-FB-PWM converter because the ZVS range is quite limited unless the leakage inductance is very large. In addition, several demerits such as duty cycle loss and parasitic ringing in the secondary limit the maximum power rating of the converter.

To apply IGBT's for high frequency (around 100 kHz), high power full bridge dc/dc converters, a ZVZCS technique, ZVS for leading-leg switches and ZCS for lagging-leg switches, has been introduced and a couple of ZVZCS-FB-PWM converters have been presented [8]–[11] (seeFig. 1). The ZVS of leading-leg switches is achieved by the same manner as that of the ZVS full bridge PWM converters [2]–[6] while the ZCS of lagging-leg switches is achieved by resetting the primary current during the freewheeling period. The primary current, however, is reset by different manners

1) by using the reverse avalanche break down voltage of the leading leg IGBT's[8], where the stored energy in the leakage inductance is completely dissipated in the leading-leg IGBT's;
2) by using the dc blocking capacitor voltage and a saturable reactor [9];
3) by adding an active clamp in the secondary side [10] which needs one additional active switch.

Using lossy components to reset the primary current [8], [9] reduces the overall efficiency and hinders the increase of power handling capability over than 5 kW. Using an active clamp increases the cost and the control complexity [10]. Another approach to reset the primary current is by adding a snubber circuit in the secondary side [11]. There is no lossy components in the snubber circuit however the rectifier voltage is increased to twice of the nominal voltage which, increases the voltage rating of the secondary rectifier diodes by twice.

This paper proposes an improved zero-voltage and zero-current-switching (ZVZCS) full bridge PWM converter to improve the disadvantages of the previously presented ZVZCS-FB-PWM converters [8]–[11]. The ZVS mechanism of leading leg switches is also the same as that of the converters in [2]–[6] and [8]–[11]. The ZCS of lagging leg switches, however, are achieved by adding a transformer auxiliary winding

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and a simple auxiliary circuit in the secondary side. No lossy components are involved and no additional active switch is added. Besides, no large circulating energy is generated. All active and passive devices are operated under minimum voltage and current stresses. So, most of the problems of the previous ZVZCS converters are solved.

The operation, analysis, features and design considerations of the proposed converter are illustrated. A 2.5 kW, 100 kHz prototype has been built using IGBT's and tested to verify the principle of operation.

II. Operation Principle

The basic operation of the proposed ZVZCS-FB-PWM converter is the same as that of the ZVS-FB-PWM converter, phase shift PWM control. The new converter has nine operating modes within each operating half-cycle. The equivalent circuits and simplified equivalent circuit are shown in Figs. 2 and 3, respectively, and the corresponding operation waveforms are shown in Fig. 4. In Fig. 3, the simplified equivalent circuit of Mode 1 is derived by reflecting the primary side to the auxiliary while those of Mode 4 and Mode 5 are derived by reflecting the secondary side to the primary.

To illustrate steady state operation, it is assumed that all components and devices are ideal and the output filter inductor current is constant during one operating half-cycle.

Mode 1: S1, S2, D1, and D2 are conducting and the input power is delivered to the output. The holding capacitor voltage V_{Ch} is charged up through the d1 and d2 by the resonance with leakage inductance as shown in Fig. 4. The simplified equivalent circuit reflected to the auxiliary circuit is shown in Fig. 3 and the holding capacitor voltage and the charging current can be obtained as follows:

$$I_c(t) = -\frac{mV_s}{Z_a}\sin(\omega_a t) \tag{1}$$

$$V_{Ch}(t) = mV_s(1-\cos(\omega_a t)) \tag{2}$$

where

$$m = \frac{N3}{N1}, \quad Z_a = \sqrt{\frac{m^2 L_{lk}}{C_h}}, \quad \omega_a = \frac{1}{\sqrt{m^2 L_{lk} C_h}}.$$

If the turns ratio of the auxiliary winding (m) is smaller than a half of that of the secondary winding ($n = N2/N1$)), the V_{Ch} reaches twice of mV's after one resonant period and D_h is never turned on. (The parasitic ringing between the leakage inductance and the junction capacitance of the secondary rectifier diodes is ignored to simplify the explanation of operation.)

Mode 2: After the half resonant period of L_{lk} and C_h, the capacitor C_h is trying to discharge through d1 and d2 and then, the d1 and d2 are turned off. The holding capacitor holds its voltage. The input power is still delivered to the output.

Mode 3: S1 is turned off and then the current through the primary winding charges capacitor $C1$ and discharges capacitor $C3$. The primary voltage is linearly decreased as follows:

$$V_{ab}(t) = V_s - \frac{nI_o}{C_1 + C_3}t \tag{3}$$

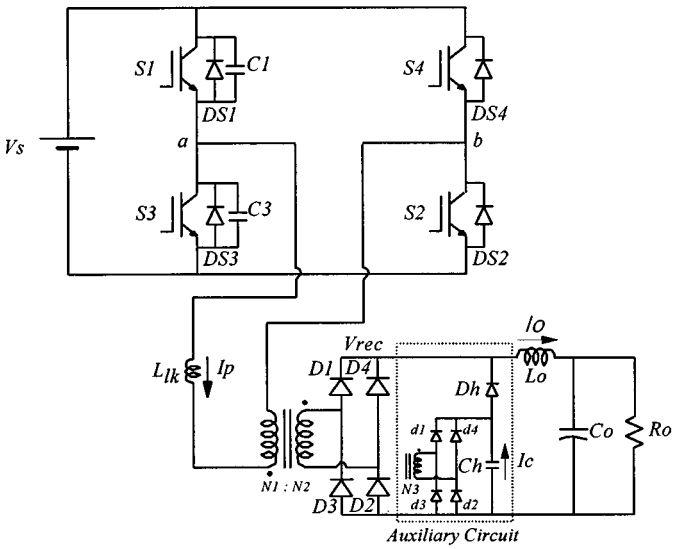

Fig. 1. Circuit topology of the proposed ZVZCS full bridge PWM converter.

and the secondary rectifier voltage is also decreased with the same rate.

Mode 4: When the rectifier voltage reaches the holding capacitor voltage V_{Ch}, the diode D_h is turned on and the rectifier voltage varies together with holding capacitor voltage. This means that the rectifier voltage decreases more slowly than the primary voltage. The primary voltage decreases almost same rate as before since the stored energy in the leakage inductance still charges $C1$ and discharges $C3$. (C_h is assumed much larger than $C1$ or $C2$.) The difference between the primary voltage and the reflected secondary voltage is applied to the leakage inductance and the primary current starts decreasing. The simplified equivalent circuit reflected to the primary is shown in Fig. 3 and the primary current and voltage and the secondary voltage can be obtained as follows:

$$I_p(t) = nI_o\left(1 - \frac{C_{eq}}{\omega_b^2}\right)\cos(\omega_b t) + \frac{C_{eq}}{\omega_b^2}nI_o \tag{4}$$

$$V_{ab}(t) = \frac{nI_o}{\omega_b}\left(\frac{1}{\omega_b^2} - \frac{1}{C_{eq}}\right)\sin(\omega_b t) - \frac{nI_o}{\omega_b^2}t + \frac{2mV_s}{n} \tag{5}$$

$$V_{rec}(t) = -\frac{I_o C_{eq}}{C_c \omega_b^3}\sin(\omega_b t) + \frac{I_o C_{eq}}{C_c \omega_b^2}t + 2mV_s \tag{6}$$

where

$$\omega_b = \sqrt{\frac{n^2 C_c + C_{eq}}{n^2 L_{lk} C_c C_{eq}}}, \qquad C_{eq} = C1 + C3.$$

At the end of this mode, the $C3$ is completely discharged and the primary current and the secondary voltage are defined as $I_p(TM4) \equiv I_a$, $V_{rec}(TM4) \equiv V_a$.

Mode 5: The $C3$ is completely discharged and then DS3 is conducting. The S3 can be turned on with ZVS. The whole reflected secondary voltage is applied to the leakage inductance and the primary current decreases more quickly. The C_h supplies more current to the load. The simplified equivalent circuit

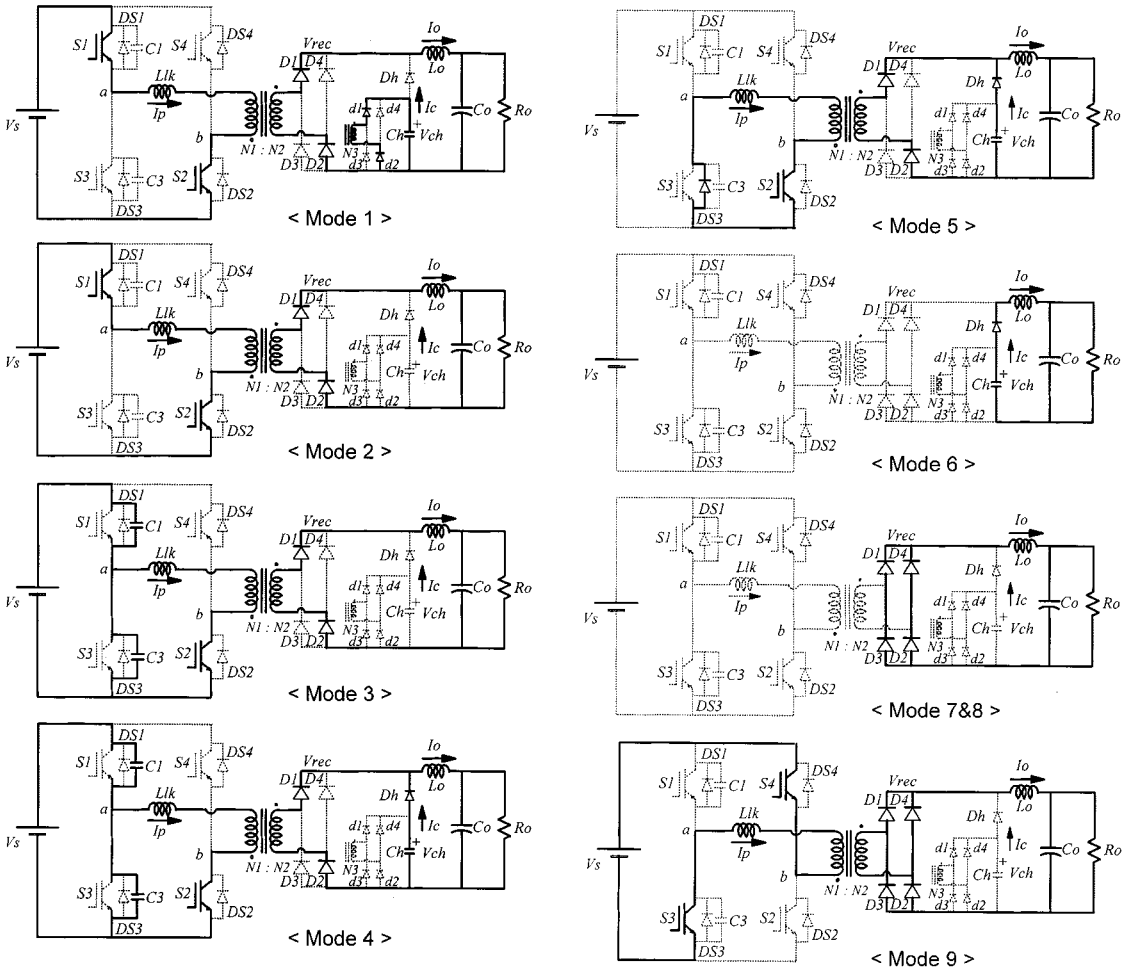

Fig. 2. Equivalent circuits for each operating mode.

reflected to the primary is shown in Fig. 3 and the primary current and the secondary voltage are obtained as follows:

$$I_p(t) = (I_a = nI_o)\cos(\omega_c t) - \frac{V_a}{nZ_c}\sin(\omega_c t) + nI_o \quad (7)$$

$$V_{rec}(t) = n(I_a = nI_o)Z_c \sin(\omega_c t) + V_a \cos(\omega_c t) \quad (8)$$

where

$$Z_c = \sqrt{\frac{L_{lk}}{n^2 C_c}}, \quad \omega_c = \frac{1}{\sqrt{n^2 L_{lk} C_c}}.$$

The primary current reaches zero at the end of this mode and the rectifier voltage is defined as $V_{rec}(TM5) = (V_\beta)$.

Mode 6: The primary current is completely reset and no current flows through the primary. Then the rectifier diodes D1 and D2 are turned off and the C_h supplies whole load current and thus the rectifier voltage is decreased quickly. From the equivalent circuit in Fig. 3, the rectifier voltage in this mode is linearly decreased as follows:

$$V_{rec}(t) = -\frac{I_o}{C_c}t + V_\beta. \quad (9)$$

Mode 7: The C_h discharges completely and then, the rectifier diodes D1–D4 start to conduct and the load current freewheels through the rectifier as most of the full bridge converters.

Mode 8: At the end of the freewheeling period, S2 is turned off with complete ZCS since there is no current in the device. The time period of this mode is the dead time between S2 and S4.

Mode 9: After dead time between S2 and S4, S4 is turned on. This turn-on process is also ZCS since the primary current can not be changed abruptly due to the leakage inductance. The primary current is linearly increased as follows:

$$I_p(t) = \frac{V_s}{L_{lk}}t. \quad (10)$$

The rectifier voltage is still zero. This is the end of an operating half-cycle.

III. Features of the Proposed Converter

A. Effective Soft Switching (ZVZCS)

In the proposed converter, the ZVS of leading leg switches is achieved by the same manner as that of the converters in [2]–[6] and [8]–[11] while the ZCS of lagging leg switches is achieved by adding a transformer auxiliary winding and a simple auxiliary circuit in the secondary side. Neither lossy components [8] and [9] nor additional active switch [10] are required to get ZCS. Besides, neither large circulating energy [11] nor high diode

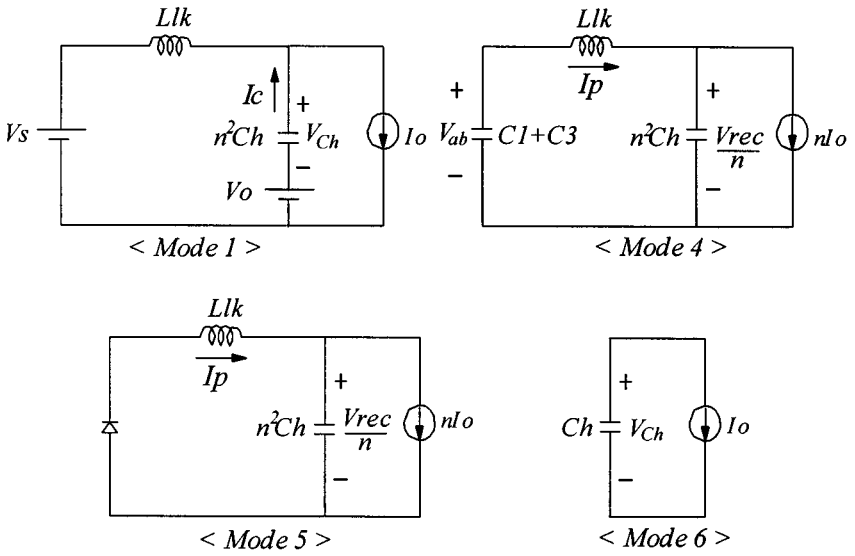

Fig. 3. Simplified equivalent circuits.

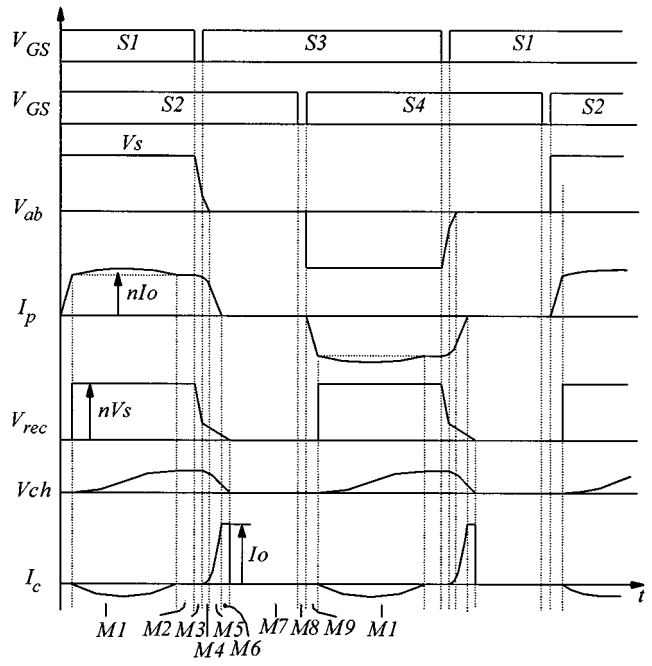

Fig. 4. Operation waveforms.

voltage stress [11] generated. All main switches and diodes are operated under minimum voltage and current stresses. In addition, wide ZVZCS range, small duty cycle loss, no severe parasitic ringing are exhibited. So, the ZVZCS is achieved very efficiently and cost effectively. Many of the problems of the previously presented ZVZCS converters [8]–[11] are solved. This means the proposed converter is very attractive for high power applications.

B. Simple Auxiliary Circuit

The proposed auxiliary circuit consists of a transformer auxiliary winding, two or four small rectifier diodes, a holding capacitor and a discharging diode. The auxiliary winding is only a few turns comparing to the main windings and thus, it does not increase the transformer size. The rectifier diodes and discharging diode are also small (about 20–30% of main diodes). The cost increase by the auxiliary circuit is almost negligible.

IV. Design Considerations

A. Design of Auxiliary Circuit

Due to the resonance between the leakage inductance and the holding capacitor, the holding capacitor voltage is increased to twice of the nominal voltage of the auxiliary winding as shown in (3). If the turns ratio of the auxiliary winding is larger than a half of the turns ratio of the secondary, the discharging diode D_h is turned on during the capacitor charging mode. This causes a ringing in the secondary rectifier. Therefore, the turns ratio of the auxiliary winding should be less than a half of that of the secondary.

If the holding capacitor voltage is high, the primary current reset time is decreased and in turn, the duty cycle loss is decreased. The circulating energy (loss), however, is increased. If the holding capacitor voltage is low, the primary current reset time is increased but the circulating energy is decreased. Therefore, the turns ratio of the auxiliary winding should be designed by trading off between the primary current reset time and the circulating energy.

The holding capacitor should be large enough to hold the secondary rectifier voltage for the time taken to reset the primary current but not to large to ensure that the holding capacitor is completely discharged during the freewheeling period. So, the holding capacitor should be optimized since large capacitance also increases the circulating energy.

B. ZVS Range of Leading-Leg

The ZVS range of leading-leg is wide but limited at light load. The snubber capacitors added to the leading-leg switches are discharged/charged by the load current first (mode 3) and then discharged/charged by the stored energy in the leakage inductance (mode 4). At light load, this stored energy in the leakage

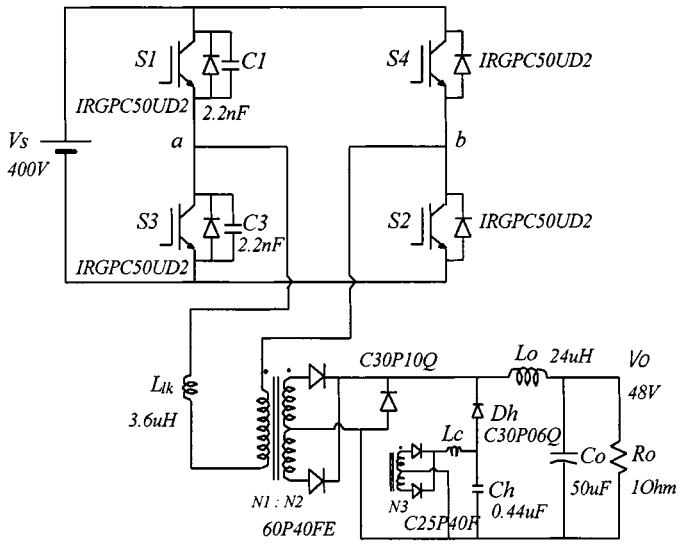

Fig. 5. Experimental circuit diagram of the proposed converter.

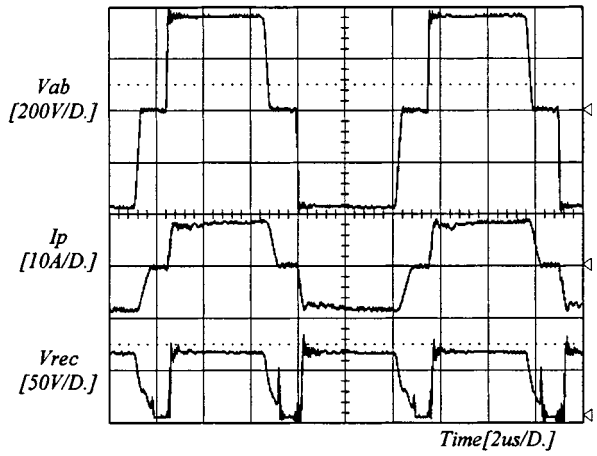

Fig. 6. Experimental waveforms of the primary voltage (V_{ab}) and primary current (I_p), and secondary rectifier voltage (V_{rec}).

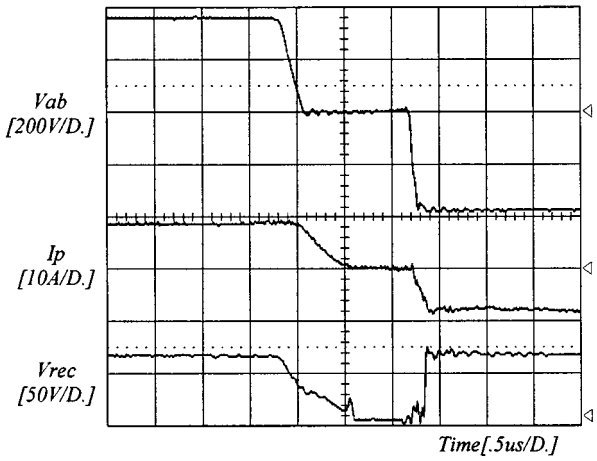

Fig. 7. Extended waveforms of Fig.6.

inductance determines the ZVS range of leading-leg. The primary voltage at the end of mode 3 is equal to the reflected peak holding capacitor voltage to the primary and then, ZVS range of leading-leg can be obtained from the energy relationship as follows:

$$I_o \geq \frac{2mV_s}{n^2}\sqrt{\frac{C1+C3}{L_{lk}}}. \tag{11}$$

It can be seen that he ZVS range of leading-leg is inversely proportional to the turns ratio of the auxiliary winding (m) and square of the snubber capacitors ($C1 + C3$), and proportional to the square of the leakage inductance.

C. ZCS Range of Lagging-Leg

The ZCS of lagging-leg is achieved by resetting the primary current and the primary current is reset by the holding capacitor voltage. At light load, the holding capacitor voltage may not be discharged completely. In this case, the holding capacitor is charged up less and the peak voltage is reduced as the load current is decreased. Then, the primary current reset time may be increased and ZCS of lagging-leg may not be achieved. The primary current, however, is also decreased as the load current is decreased and the ZCS of lagging-leg can be achieved by lower holding capacitor voltage. Therefore, the ZCS range of lagging-leg is wide enough.

V. Experimental Results

A 2.5 kW, 100 kHz prototype of the proposed ZVZCS-FB-PWM converter has been built and tested to verify the principle of operation. Fig. 5 shows the experimental circuit diagram with the part numbers of components used. The transformer is built using two PQ5050 cores in parallel with the turns ratio of $N1:N2 = 21:4$. The leakage inductance measured at the switching frequency is 3.6 μH. IRGPC50UD2 IGBT's are used for the primary switches. PC50F4 diode is used for the secondary rectifier and C30P10Q Schottky diode is used for freewheeling diode which allows the freewheeling current to flow not through the transformer secondary but through the Schottky diode. The circulating energy can be reduced since there is no diode reverse recovery during the transition from the free wheeling mode to the powering. The auxiliary winding is only 1.5 turns with center tapped structure and the holding capacitor is 0.44 μF.

Fig. 6 shows the waveforms of the primary voltage and current, and the secondary rectifier voltage and Fig. 7 shows their extended waveforms. It can be seen that the secondary rectifier voltage still left after the primary voltage falls down to zero and the primary current is completely reset by this secondary rectifier voltage during the freewheeling period. This provides ZCS condition to the lagging-leg IGBT's. All waveforms are quite clean thanks to complete soft switching and well matched with the theoretical ones.

Fig. 8 shows the ZVS waveforms of leading-leg switches. From the ZVS turn-on waveforms, the antiparallel diode current is not staying but decreasing to zero since the primary current is reset during freewheeling period. The ZVS turn-on is achieved by turning on S3 while the anti-parallel diode is conducting. The ZVS turn-off waveforms show the typical IGBT tail current

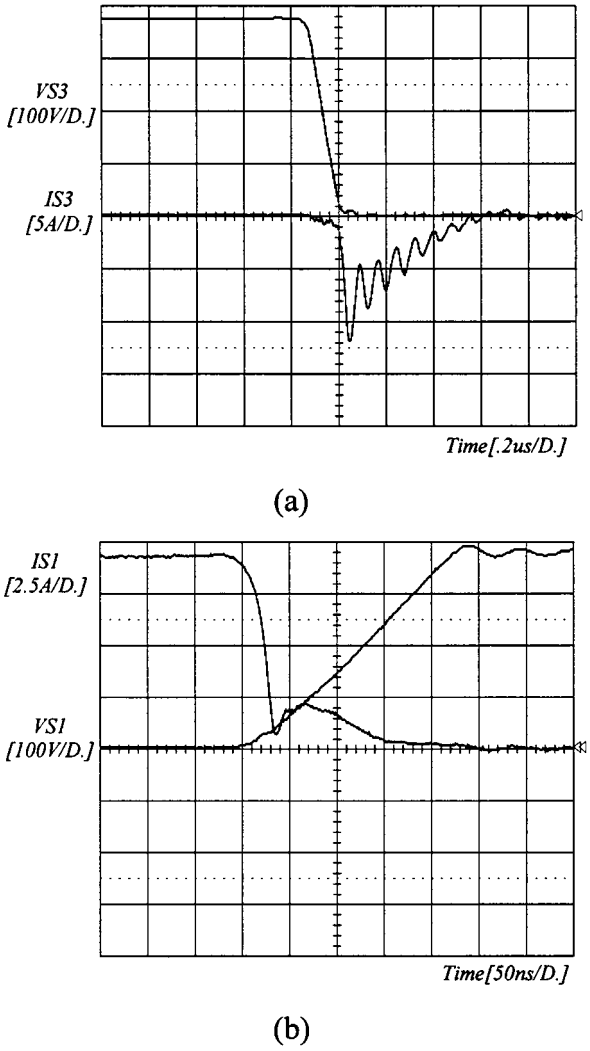

Fig. 8. ZVS waveforms of leading-leg switches: (a) turn-on and (b) turn-off.

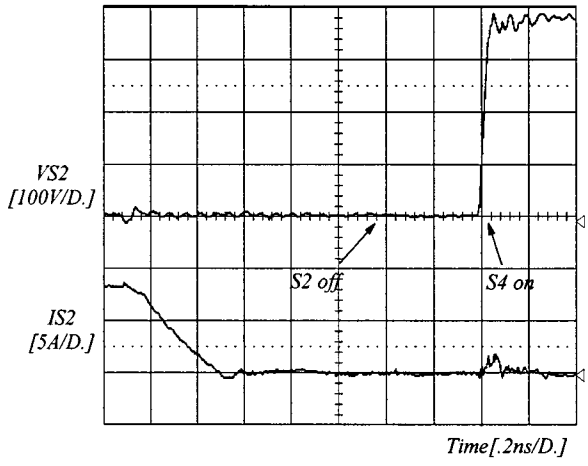

Fig. 9. ZCS waveforms of lagging-leg switches.

but the switching loss is considerably reduced by delaying the applied switch voltage.

Fig. 9 shows ZCS waveforms of lagging-leg switches. The switch S2 is turned off with complete ZCS since the current through it is zero before turning off. There is no IGBT tail current due to ZCS. A small current pulse when the S4 is turned on is the charging current of switch output capacitances. Fig. 10 shows the waveforms of rectifier voltage and holding capacitor voltage and current and Fig. 11 shows the extended waveforms of the Fig. 10. All waveforms are also the same as the expected except the holding capacitor voltage. The holding capacitor voltage goes to the negative, which is because of the stray inductance of rectifier and auxiliary circuit.

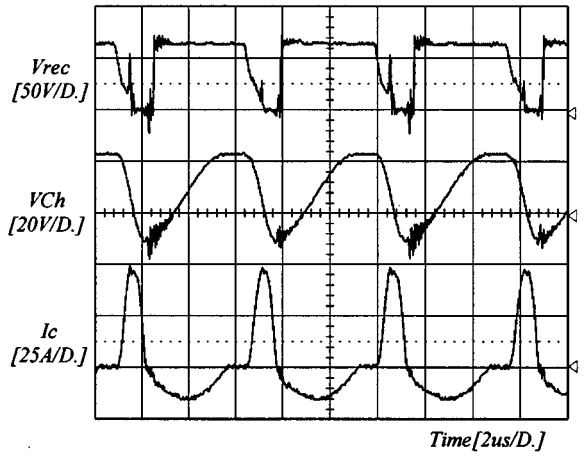

Fig. 10. Waveforms of secondary rectifier voltage (V_{rec}) and holding capacitor voltage (V_{Ch}), and current (I_c).

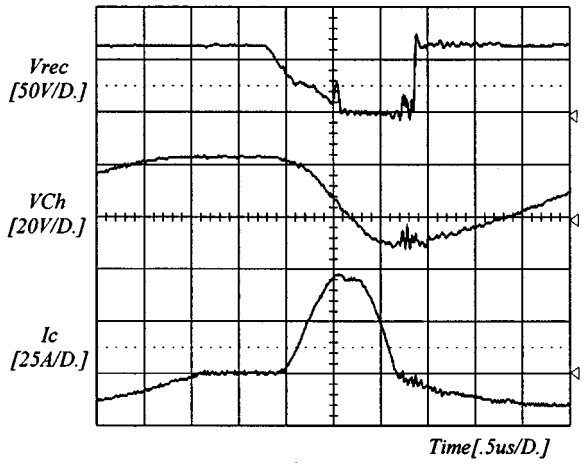

Fig. 11. Waveforms of secondary rectifier voltage (V_{rec}) and holding capacitor voltage (V_{Ch}) and current (I_c).

Fig. 12 shows the measured efficiency of the proposed converter with the efficiency of the previous ZVZCS converter [8] for comparison. Maximum efficiency of the proposed converter at full load is 94.5%. It can be seen that the proposed converter has higher efficiency at full load while it has lower efficiency at light load comparing to the efficiency of the previous ZVZCS converter [8]. That is because the circulating energy of the proposed converter becomes higher at light load.

Novel ZVZCS concept allows to use a low cost IGBT's (10–20 kHz recommended switching frequency) at a very high

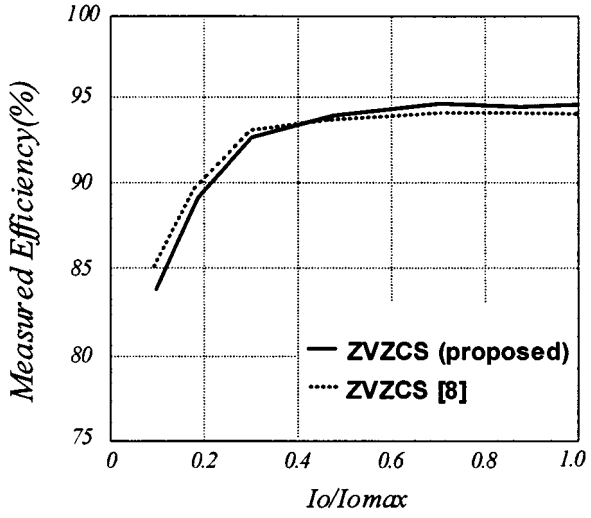

Fig. 12. Measured efficiencies of the proposed converter and the previous ZVZCS converter in [8].

frequency (100 kHz) without any detrimental effect on the efficiency.

VI. Conclusion

An improved ZVZCS-FB-PWM converter using the transformer auxiliary winding is presented. The operation, analysis, features and design considerations are illustrated. Experimental results from the 2.5 kW, 100 kHz IGBT based prototype is shown to verify the operation principle.

It is shown that ZVZCS is achieved by using the transformer auxiliary winding and the simple auxiliary circuit and most of problems of the previously presented ZVZCS converters are solved as follows: no lossy components are involved; no additional active switch, no additional device voltage and current stresses are exhibited. The distinct advantages of the new circuit including ZVZCS with wide load range (IGBT's can be used), small duty cycle loss, minimum device voltage and current stresses, and low cost make the proposed converter very promising for medium power (>2 kW) applications with high power density.

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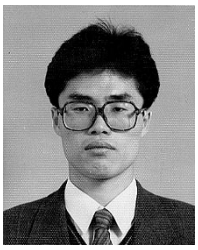

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