Novel Zero-Voltage and Zero-Current-Switching Full-Bridge PWM Converter Using a Simple Auxiliary Circuit

Jung-Goo Cho, *Member, IEEE*, Ju-Won Baek, Chang-Yong Jeong, and Geun-Hie Rim, *Member, IEEE*

***Abstract*— A novel zero-voltage and zero-current-switching (ZVZCS) full-bridge pulsewidth modulation converter is presented to simplify the circuits of the previously presented ZVSCS converters. A simple auxiliary circuit, which consists of one small capacitor and two small diodes, is added in the secondary to provides ZVZCS conditions to primary switches, as well as to clamp secondary rectifier voltage. The additional clamp circuit for the secondary rectifier is not necessary. The auxiliary circuit includes neither lossy components nor additional active switches, which makes the proposed converter efficient and cost effective. The principle of operation, features, and design considerations are illustrated and verified on a 2.5-kW 100–kHz insulated-gate-bipolar-transistor-based experimental circuit.**

***Index Terms*— DC/DC converter, insulated gate bipolar transistor, soft switching.**

I. Introduction

With the increasing demand for higher power density power conversion with lower cost, insulated gate bipolar transistors (IGBT's) are considered as power devices instead of MOSFET's in the high-frequency high-power applications, since IGBT's have higher power density and lower cost compared to MOSFET's. The operating frequency of IGBT's, however, is much lower than MOSFET's, (usually limited to 20–30 kHz) [1] because of higher switching loss which comes from the tail current during the turn-off period. Therefore, to operate IGBT's at higher switching frequencies, it is required to reduce the turn-off switching loss. Zero-voltage switching (ZVS) with a substantial external snubber capacitor or Zero-current switching (ZCS) can be a solution, but the ZCS is more effective than ZVS, since the tail current can be eliminated by removing the minority before turning off [4].

To apply IGBT's for high-frequency (around 100 kHz) high-power full-bridge dc/dc converters, a ZVZCS technique has been introduced and a couple of ZVZCS full bridge (FB) pulsewidth modulation (PWM) converters have been presented [5]–[9]. The ZVZCS means mixed operation of ZVS for leading-leg switches and ZCS for lagging-leg switches. The ZVS of leading-leg switches is achieved by the same manner as that of the ZVS FB PWM converters [2], [3], while the ZCS of lagging-leg switches is achieved by resetting the primary current during the freewheeling period. So far, a couple of ZVZCS-FB-PWM converters have been presented [5]–[9]. Their primary currents during freewheeling period, however, are reset by different manners. In the converter [5], the primary current is reset by using the reverse avalanche breakdown voltage of the leading-leg IGBT's, where the stored energy in the leakage inductance is completely dissipated in the leading-leg IGBT's. This approach is not efficient, unless the leakage inductance is very small. In the converter [6], the primary current is reset by using the dc blocking capacitor voltage and adding a saturable reactor. The saturable reactor loss limits the maximum power level by 5 kW. In the converter [7], the primary current is reset by adding an active clamp in the secondary side, which provides ZVZCS condition to the primary switches, as well as the active clamp of the secondary rectifier. The additional switch, however, makes switching loss due to hard switching and increases cost and control complexity. In the converter [8], the primary current is reset by adding a snubber circuit in the secondary side. There are no lossy components in the snubber circuit, however, the large circulating energy by the resonance between the leakage inductance and snubber capacitors reduces the overall efficiency and increases the voltage rating of the secondary rectifier diodes by two times. In the converter [9], the primary current is reset by using the transformer auxiliary winding. Neither lossy components involved nor an additional active switch are added. Besides, no large circulating energy is generated. All active and passive devices are operated under minimum voltage and current stresses. This approach can handle more than 10 kW, but the auxiliary circuit is a little bit complex.

This paper proposes a novel ZVZCS-FB-PWM converter with a simple auxiliary circuit to improve the previously presented ZVZCS-FB-PWM converters (see Fig. 1). The ZVS mechanism of leading-leg switches is also the same as that of the converters in [2], [3], and [5]–[9]. A simple auxiliary circuit provides not only ZVZCS condition to the primary switches, but clamping of the secondary rectifier. Therefore, most of the problems of the previous ZVZCS converters are solved and, furthermore, an additional passive or active clamp circuit is not necessary.

The operation, analysis, features, and design considerations of the proposed converter are illustrated. A 2.5-kW 100-kHz

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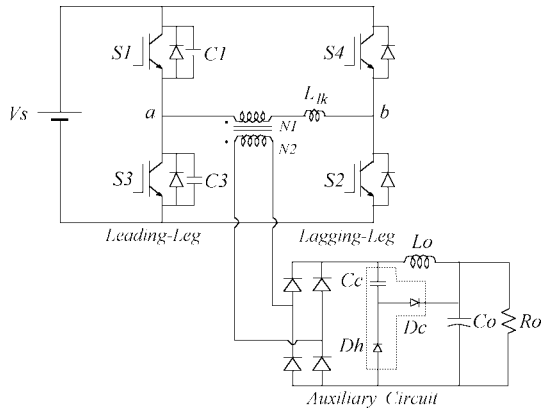

Fig. 1. Circuit topology of the proposed ZVZCS-FB-PWM converter.

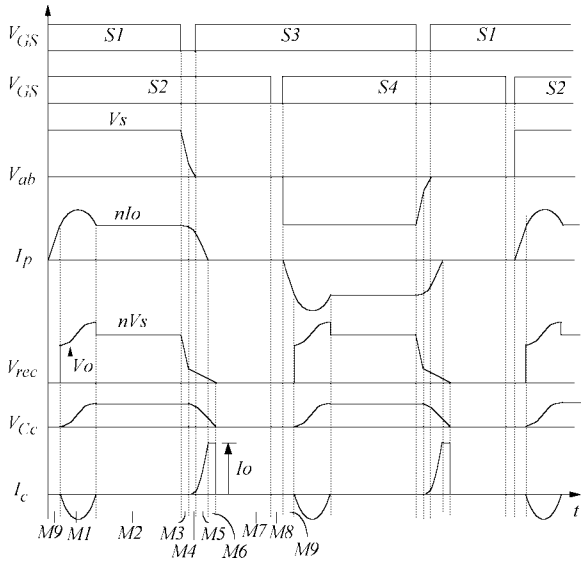

Fig. 2. Operation waveforms of the proposed converter.

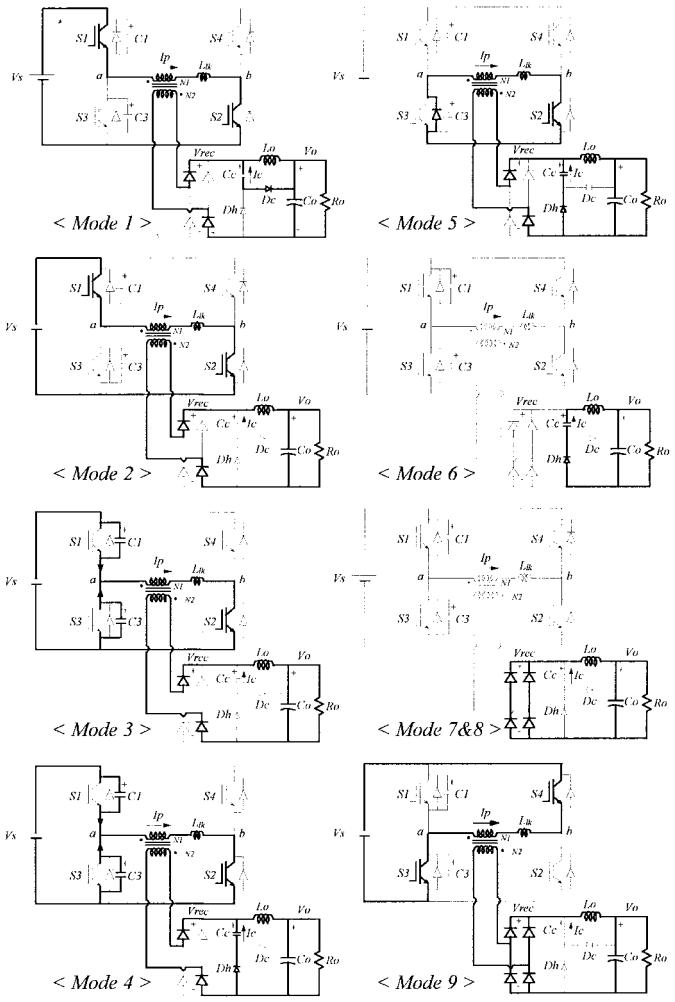

Fig. 3. Equivalent circuits for each operating mode.

prototype has been built using IGBT's and tested to verify the principle of operation.

II. Operation Principle

The basic operation of the proposed ZVZCS-FB-PWM converter is the same as that of the ZVS-FB-PWM converter, the phase shift PWM control. The new converter has nine operating modes within each operating half cycle. The operation waveforms and equivalent circuits are shown in Figs. 2 and 3, respectively. To illustrate steady-state operation, it is assumed that all components and devices are ideal and the output filter inductor is a constant current source.

Mode 1: $S1$ and $S2$ are conducting and the input power is delivered to the output. The clamping capacitor voltage V_{Cc} is charged up through D_c and C_o by the resonance with leakage inductance, as shown in Fig. 3. The V_{Cc} reaches twice $(nV_s - V_o)$ after a half resonance period (L_{lk} and C_c) at the end of this mode, where n is the transformer turns ratio. The rectifier voltage starts from V_o and reaches $V_{Cc}+V_o$, as shown in Fig. 2. The detailed equivalent circuit is shown in Fig. 4. (The junction capacitance of the secondary rectifier diodes is ignored to simplify the explanation of operation.) The primary current and the clamping capacitor voltage and current can be obtained as follows:

$$I_p(t) = nI_o(1-\cos(\omega_a t)) - \frac{V_s - V_o/n}{Z_a}\sin(\omega_a t) + nI_o \tag{1}$$

$$I_c(t) = nI_o - I_p(t) \tag{2}$$

$$V_{Cc}(t) = nV_s(1-\cos(\omega_a t)) - n^2 Z_a I_o \sin(\omega_a t) \tag{3}$$

where

$$Z_a = \sqrt{\frac{L_{lk}}{n^2 C)c}}, \qquad \omega_a = \frac{1}{\sqrt{n^2 L_{lk} C_c}}.$$

Mode 2: D_c is turned off and the rectifier voltage is returned to the nominal value nV_s. D_h is never turned on during this mode, unless the duty cycle is smaller than 0.5. The input power is still delivered to the output during this mode.

Mode 3: $S1$ is turned off and then the current through the primary charges C_1 and discharges C_3. The primary voltage is linearly decreased and the secondary rectifier voltage is also decreased with the same rate. The primary voltage decreased

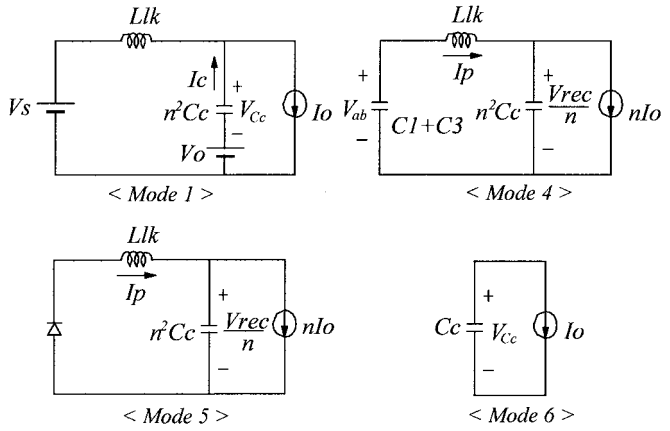

Fig. 4. Simplified equivalent circuits.

linearly as follows:

$$V_{ab}(t) = V_s - \frac{nI_o}{C1+C3}t. \tag{4}$$

Mode 4: When the rectifier voltage reaches the clamping capacitor voltage V_{Cc}, the diode D_h is turned on and the C_c holds the rectifier voltage, which means the rectifier voltage decreases much slower than the primary voltage. The primary voltage keeps decreasing with almost the same rate as before, since the stored energy in the leakage inductance still charges C_1 and discharges C_3. (C_c is assumed much larger than C_1 or C_3.) The difference between the primary voltage and the reflected secondary voltage is applied to the leakage inductance and the primary current starts decreasing. The simplified equivalent circuit reflected to the primary is shown in Fig. 4. The voltage and current of the circuit are as follows:

$$V_{ab}(t) = \frac{nI_o}{\omega_b}\left(\frac{1}{\omega_b^2} - \frac{1}{C_{eq}}\right)\sin(\omega_b t) - \frac{nI_o}{\omega_b^2}t + 2V_{Lo} \tag{5}$$

$$I_p(t) = nI_o\left(1 - \frac{C_{eq}}{\omega_b^2}\right)\cos(\omega_b t) + \frac{C_{eq}}{\omega_b^2}nI_o \tag{6}$$

$$V_{Cc}(t) = -\frac{I_o C_{eq}}{C_c\omega_b^2}\sin(\omega_b t) + \frac{I_o C_{eq}}{C_c\omega_b^2}t + 2V_{Lo} \tag{7}$$

where

$$\omega_b = \sqrt{\frac{n^2C_c + C_{eq}}{n^2L_{lk}C_cC_{eq}}}, \quad C_{eq} = C_1 + C_3.$$

The primary current and the secondary voltage at the end of this mode are defined as I_α and V_α.

Mode 5: C_3 is completely discharged and then $DS3$ is conducting. The reflected secondary voltage is applied to the leakage inductance and the primary current decreases quickly. C_c supplies more current to the load. The primary current and the clamp capacitor voltage are obtained as follows:

$$I_p(t) = (I_\alpha - nI_o)\cos(\omega_a t) - \frac{V_\alpha}{nZ_\alpha}\sin(\omega_a t) + nI_o \tag{8}$$

$$V_{Cc}(t) = n(I_\alpha - nI_o)Z_a\sin(\omega_a t) + \frac{V_\alpha}{n}\cos(\omega_a t). \tag{9}$$

The primary current reaches zero at the end of this mode. The rectifier voltage at the end of this mode is defined as V_β.

Mode 6: The primary current is completely reset and no current flows through the primary. Then, C_c supplies the whole load current and, thus, the secondary rectifier voltage is decreased quickly. From the equivalent circuit in Fig. 4, the clamping capacitor voltage is obtained as follows:

$$V_{Cc}(t) = -\frac{I_o}{C_c}t + V_\beta. \tag{10}$$

Mode 7: When C_c discharges completely, the rectifier diodes start to conduct and the load current freewheels through the rectifier.

Mode 8: At the end of the freewheeling period, S_2 is turned off with complete ZCS, since there is no current in the device. This mode is a dead time between S_2 and S_4.

Mode 9: S_4 is turned on. This turn-on process is also ZCS, since the primary current cannot be changed abruptly due to the leakage inductance. The primary current is linearly increased as follows:

$$I_p(t) = \frac{V_s}{L_{lk}}t. \tag{11}$$

The rectifier voltage is still zero. This is the end of an operating half cycle.

III. Features and Characteristics

A. Simple Auxiliary Circuit

The rectifier circuits and their typical voltage waveforms of the previously presented ZVZCS converters [8], [9] and the proposed converter are compared in Fig. 5. All rectifier circuits include neither lossy components nor additional active switches. The ZVZCS converter [9] includes the auxiliary circuit, which consists of a transformer auxiliary winding, a small bridge rectifier, a small clamping capacitor, and a small discharging diode and a passive clamp circuit, as shown in Fig. 5(a). The auxiliary circuit looks a little bit complex, even though two diodes can be eliminated by using the center-tapped rectifier. The rectifier voltage is clamped by clamp capacitor voltage and this clamping voltage depends on the discharging resistor Rc. The rectifier voltage is usually designed with 120% of the nominal voltage nVs. The clamp circuit, however, increases loss. The ZVZCS converter [8] includes the auxiliary circuit, which consists of three small diodes and two small capacitors, as shown in Fig. 5(b). No clamp circuit is required. The auxiliary circuit looks a little bit simpler than that of Fig. 5(a). The peak rectifier voltage, however, is increased up to almost twice the nominal voltage nVs, since $C1$ and $C2$ in series and the leakage inductance are fully resonant during the transition from the freewheeling mode to the powering. This means that the voltage stress of the rectifier diodes is almost twice that of the converter in Fig. 5(a), and there exists a lot of circulating energy, which also increases conduction loss. The proposed converter includes the auxiliary circuit which consists of a small capacitor and two small diodes. The auxiliary circuit is simplest. The peak rectifier voltage is not

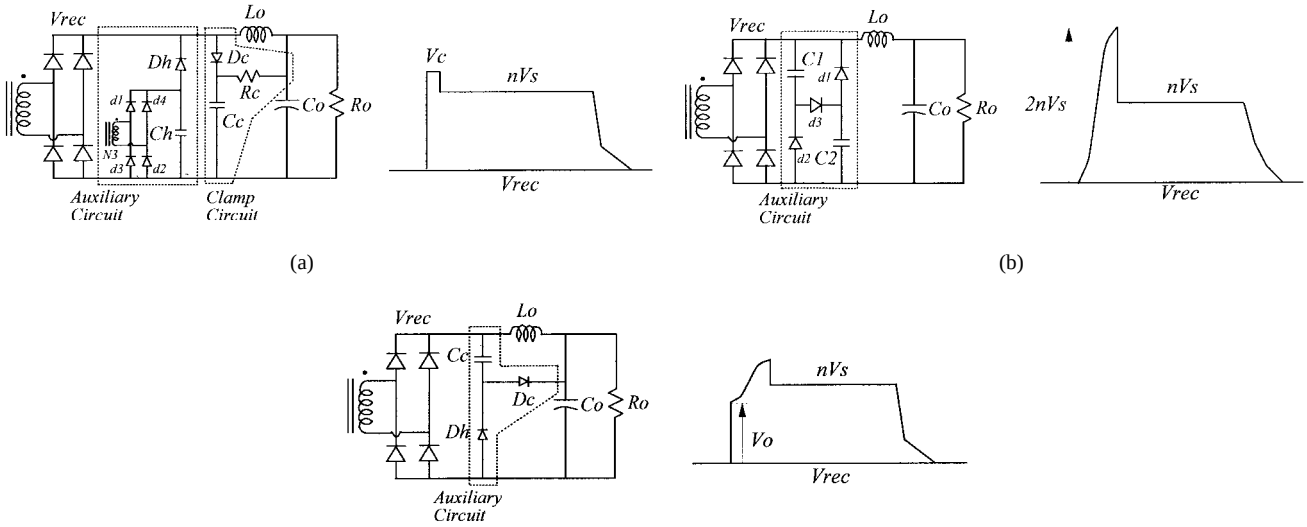

Fig. 5. Comparison of secondary rectifier circuits of the ZVZCS converters. (a) ZVZCS converter [9]. (b) ZVZCS converter [8]. (c) Proposed converter.

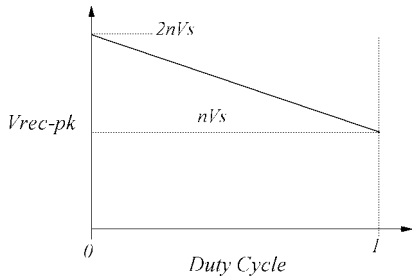

Fig. 6. Peak rectifier voltage according to the duty cycle.

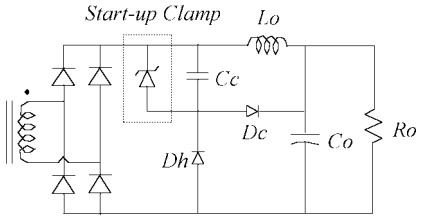

Fig. 7. Rectifier clamp circuit for startup.

constant, and it depends on the duty cycle as follows:

$$V_{\text{rec-pk}} = nVs(2 - D). \tag{12}$$

The peak rectifier voltage is inversely proportional to the duty cycle, as shown in Fig. 6, and the duty cycle should be high to achieve low rectifier voltage stress. The power supply designers usually push up the duty cycle as high as possible to acieve high efficiency. So, the low rectifier diodes voltage stress can be maintained practically and, in turn, the circulating energy is also minimized. For example, if the duty cycle is 0.8, the peak rectifier voltage is limited to 120% of the nominal voltage nVs, which is almost the same as that of the usual passive clamp circuit. During the startup period, however, the duty cycle starts up slowly from zero for soft start, which may give high voltage stress to the rectifier. To solve this problem, a small Zener diode is added in parallel with the clamping capacitor, as shown in Fig. 7. The Zener diode clamps the rectifier voltage during the startup and blocks in the steady state. The power rating of the Zener diode can be small, since the startup period is relatively small.

Fig. 14 shows measured efficiency of the proposed converter. Maximum efficiency at full load is close to 95%. The novel ZVZCS concept allows the use of low-cost IGBT's (10–30 kHz recommended switching frequency) at a very high frequency (100 kHz) without any detrimental effect on the efficiency.

B. Efficient Soft Switching

Neither lossy components, such as a saturable reactor, nor an additional active switch are involved to achieve ZVZCS. Besides, no large circulating energy is generated and no additional clamp circuit is necessary, since the secondary rectifier voltage is clamped to the clamping capacitor voltage plus the output voltage. All active and passive devices are operated under low voltage and current stresses. In addition, wide ZVZCS range, small duty cycle loss, and no severe parasitic ringing are exhibited. So, the ZVZCS of the proposed converter is achieved very efficiently and cost effectively and most of the problems of the previously presented ZVZCS converters [5]–[9] are solved. This means the proposed converter is very attractive for high-power applications.

IV. Experimental Results

A 2.5-kW 100-kHz prototype of the proposed ZVZCS-FB-PWM converter has been built and tested to verify the principle of operation. Fig. 8 shows the experimental circuit with the part numbers of the components used. The transformer is built using two PQ5050 cores in parallel with the turns ratio of $N1 : N2 = 21 : 4$. The leakage inductance measured at the switching frequency is 3.6 μH. IRGPC50UD2 IGBT's are used for the primary switches. A PC50F4 diode is used for the secondary rectifier and a C30P10Q Schottky diode is used for the freewheeling diode, which allows the freewheeling current to flow not through the transformer secondary, but through the

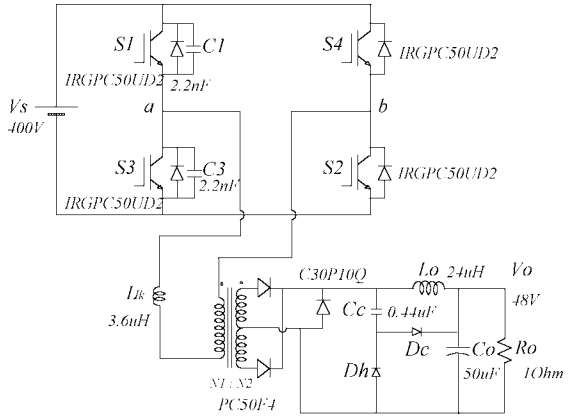

Fig. 8. Experimental circuit diagram of the proposed converter.

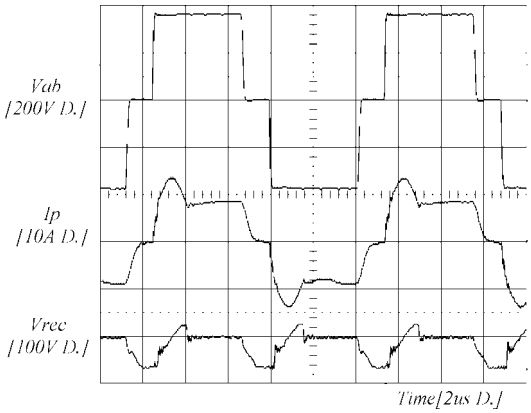

Fig. 9. Experimental waveforms of the primary voltage and current and secondary rectifier voltage.

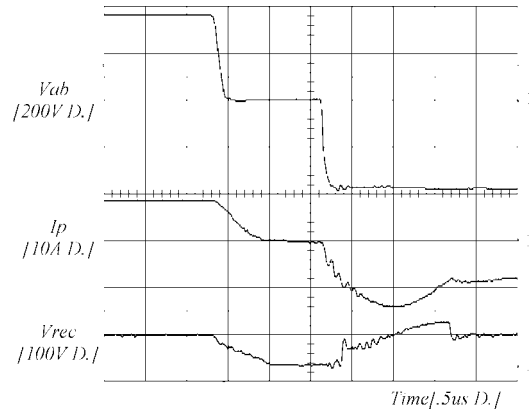

Fig. 10. Extended waveforms of Fig. 7.

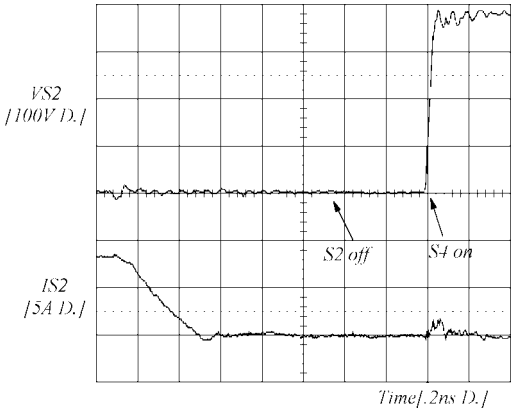

Fig. 11. ZCS waveforms of lagging-leg switches.

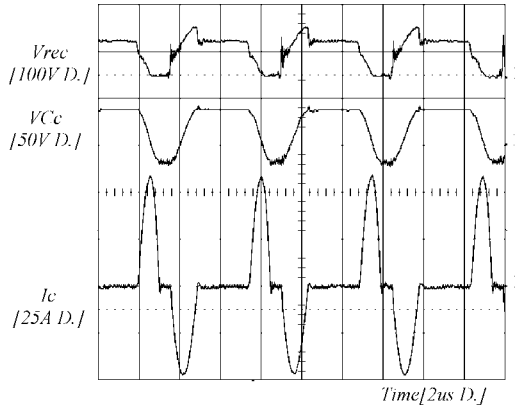

Fig. 12. Waveforms of secondary rectifier voltage and clamping capacitor voltage and current.

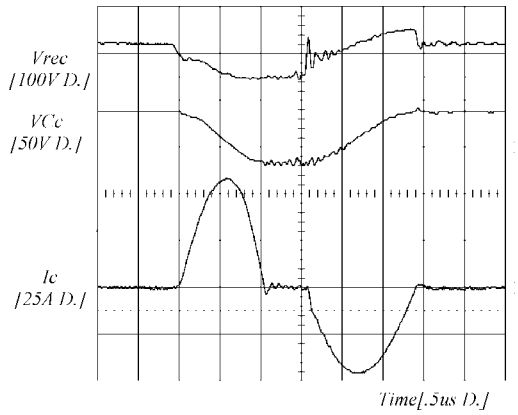

Fig. 13. Waveforms of secondary rectifier voltage and clamping capacitor voltage and current.

Schottky diode. The circulating energy and reverse recovery loss can be reduced, since there is no diode reverse recovery in the Schottky diode during the transition from the freewheeling mode to the powering. The clamping capacitor is 0.44 μF.

Fig. 9 shows the waveforms of the primary voltage and current and the secondary rectifier voltage, and Fig. 10 shows their expended waveforms. It can be seen that the primary current is completely eliminated during the freewheeling period, since the secondary rectifier voltage applies negative voltage to the leakage inductance. Fig. 11 shows the switching waveforms of lagging-leg switches. The current through switch $S2$ is zero before turning off and, thus, $S2$ is turned off with complete ZCS, and no tail current is exhibited. A small current pulse when $S4$ is turned on is the charging current of the output capacitance of $S2$**.** Figs. 12 and 13 show the waveforms of rectifier voltage and clamping capacitor voltage and current and their extended waveforms. The clamping capacitor voltage goes to the negative because of the stray inductance of the rectifier and auxiliary circuit layout, and the clamping capacitor current waveform is smoothed because of

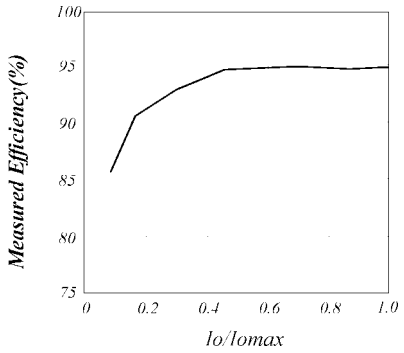

Fig. 14. Measured efficiency of the proposed converter.

the stray inductance and capacitance of the auxiliary circuit layout. All waveforms are matched with the expected.

V. Conclusion

The novel ZVZCS-FB-PWM converter has been presented, and the operation, features, and characteristics have been illustrated. Experimental results from the 2.5-kW 100-kHz IGBT-based prototype were shown to verify the operation principle.

It was shown that the clamping of rectifier diodes, as well as the ZVZCS of the primary switches, are achieved by adding a simple auxiliary circuit in the secondary. The auxiliary circuit consists of a small capacitor and two small diodes, the ratings of which are about 30% of the main diodes. Neither lossy components nor additional active switches are involved to get ZVZCS, and the secondary rectifier clamp circuit is eliminated. In addition, Distinctive advantages of the new circuit including ZVZCS with wide load range (IGBT's can be used), small duty cycle loss, low device voltage and current stresses, and low cost make the proposed converter very promising for high-power (>5 kW) applications with high power density.

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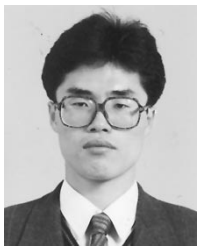

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