Numerical analysis of electronic circuits with FDTD-LE technique

M. Matteucci, P. Mezzanotte, L. Roselli, P. Ciampolini
Istituto di Elettronica, Università di Perugia, Via G. Duranti 1/A, I-06131 Perugia, Italy

Abstract

In this paper, an accurate technique for the simulation of high-frequency electronic circuits is described. The circuit simulator is based on a three dimensional implementation of the Lumped Element FDTD (LE-FDTD). A fairly wide library of basic linear and non linear device models suitable for HF simulations has been arranged, which includes: linear resistors, inductors and capacitors, matched voltage generators, pn and Shottky diodes, bipolar transistors, and MeSFETs. Dynamic, as well as static device behavior is taken into account. Some simulation examples are given, and compared with alternative simulation techniques.

1 Introduction

In this paper, a circuit simulation strategy is discussed, based on the Finite-Difference Time-Domain method and extended to accomplish the insertion of lumped elements [1].
The FDTD method [2] allows for the direct solution of Maxwell's equations over distributed domains (i.e., the interconnecting network), whereas equivalent-circuit descriptions are adopted for lumped models. This allows for the analysis of electromagnetic propagation effects occurring within electronic circuits: with respect to conventional circuit CAD tools (e.g., SPICE [3]), line discontinuities, crosstalk phenomena, parasitic impedances can be much more realistically taken into account.
Fundamentals of FDTD-LE technique can be found in [1, 3]; nevertheless, much work is still to be done in order to make such a technique suitable for practical and reliable circuit simulation [3 - 5]. Dealing with this purpose, this contribution describes recent achievements in the development of our FDTD-

LE simulator. More specifically, a large-signal GaAs MeSFET model has been, for the first time, incorporated into the FDTD integration scheme.
A remarkable computational robustness and efficiency has been attained by introducing an adaptive algorithm for the dynamic selection of the simulation time step [5]. Significant CPU-time savings can be obtained by this method, which makes it possible the simulation of fairly complex high-frequency circuits within reasonable computational efforts.
Two simulation examples will be discussed to demonstrate how FDTD-LE can be already considered a practical tool for the analysis of signal integrity and propagation in electronic circuits.

2 The Lumped Element FDTD Algorithm

To account for lumped elements, we start from Maxwell curl $\overline{H}$ equation:

$$curl(\overline{H}) = \varepsilon \frac{d\overline{E}}{dt} + \overline{J}_c \tag{1}$$

The conduction current density $\overline{J}_c$ in the above equation can be split into two separate contributions:

$$\overline{J}_c = \overline{J}_{cd} + \overline{J}_{cl}. \tag{2}$$

Here, $\overline{J}_{cd}$ represents the contribution of the current density flowing along the distributed medium, whereas $\overline{J}_{cl}$ stands for the contribution of the lumped elements. Linear, as well as nonlinear, lumped elements may show up in the latter term. Resistors, capacitors, inductors, voltage sources are modeled according to the literature [3]. The current flowing across a *pn*-junction is expressed as in [5] and includes the effects of non linear capacitances associated to the junction itself.
The resulting discretized expression of the diode current density becomes strongly nonlinear; numerical treatments of such non linearities has been discussed in [5].
Bipolar transistors are taken into account by arranging a network of non ideal junction diodes and current-controlled current-sources, according to the well known Ebers-Moll scheme. In this case, however, two coupled non linear equations are to be solved for each bipolar transistor of the circuit.
Similar building blocks can be assembled to obtain the large-signal equivalent circuit of the MeSFET shown in Fig. 1.

Transactions on Engineering Sciences vol 11, © 1996 WIT Press, www.witpress.com, ISSN 1743-3533

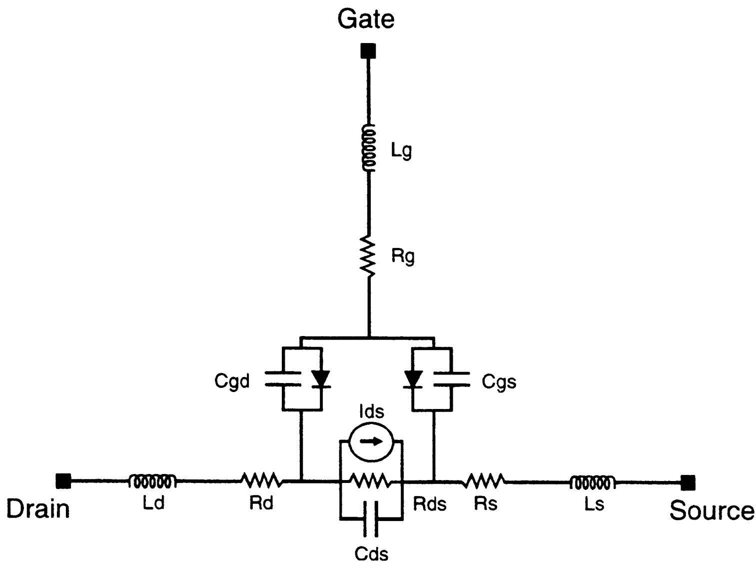

Figure 1: Large signal model of the GaAs MeSFET

In such a scheme, drain and source junctions are modeled by means of non-ideal pn junctions. Series resisistors ($R_{g,s,d}$) and inductors ($L_{g,s,d}$) are taken into account at each device terminal. The drain current is expressed, according to Curtice [7]:

$$I_{ds}\left(V_{ds},V_{gs}(t-\tau)\right)=I_{ds}\left(V_{ds},V_{gs}\right)-\tau\frac{dI_{ds}}{dV_{gs}}\frac{dV_{gs}}{dt}+\frac{V_{ds}}{R_{ds}}+C_{ds}\frac{dV_{ds}}{dt} \tag{3}$$

where τ accounts for the transit time of the charge carriers under the gate. I_{ds} can be, in turn, described according to the so called quadratic model:

$$I_{ds}\left(V_{ds},V_{gs}\right)=\beta\cdot\left(1+\lambda\cdot V_{ds}\right)\cdot\left(V_{gs}-V_{to}\right)^{2}\cdot tanh\left(\alpha\, V_{ds}\right)\quad per\ V_{gs}>V_{to} \tag{4a}$$

$$I_{ds}\left(V_{ds},V_{gs}\right)=0\quad per\ V_{gs}<V_{to} \tag{4b}$$

in Eqs. (4), β is the transconductance parameter, λ is the channel length modulation parameter, V_{to} is the threshold voltage and α is the saturation voltage parameter.
Substituting 4 into 3 leads to:

$$I_{ds}\left(V_{ds},V_{gs}(t-\tau)\right)=\beta\cdot\left(1+\lambda\cdot V_{ds}\right)\cdot\left(\left(V_{gs}-V_{to}\right)^2-2\cdot\tau\cdot\left(V_{gs}-V_{to}\right)\cdot\frac{dV_{gs}}{dt}\right)\cdot$$
$$\cdot\tanh\left(\alpha\cdot V_{ds}\right)+\frac{V_{ds}}{R_{ds}}+C_{ds}\cdot\frac{dV_{ds}}{dt} \qquad (5)$$

The equations above are incorporated into the FDTD framework by assembling the lumped element network shown in Fig. 2.

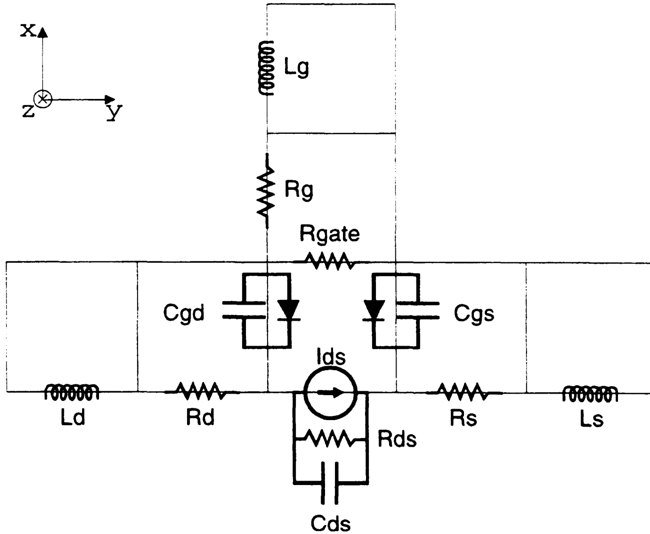

Figure 2: Discretized MeSFET model.

Here, a negligible-value resistor (R_{gate}) appears to join the cells forming the device gate.
Assuming the Yee's standard notation, with the controlled generator placed at position *(i, j+1/2, k)*, the drain junction at position *(1+1/2, j, k)* and the source junction at position *(1+1/2, j+1, k)*, the discretized form of Eq. (5) reads:

$$
\begin{aligned}
J_y^{n+\frac{1}{2}}\left(i,j+\frac{1}{2},k\right) = \frac{\beta}{\Delta x \cdot \Delta z} \cdot \left(1+\lambda \cdot \Delta y \cdot \frac{E_y^{n+1}\left(i,j+\frac{1}{2},k\right)+E_y^{n+1}\left(i,j+\frac{1}{2},k\right)}{2}\right) \cdot \\
\cdot \left(\left(\Delta x \cdot \frac{E_x^{n+1}\left(i+\frac{1}{2},j+1,k\right)+E_x^{n+1}\left(i+\frac{1}{2},j+1,k\right)}{2} - V_{to}\right)^2 - \right. \\
\left. -2 \cdot \tau \cdot \left(\Delta x \cdot \frac{E_x^{n+1}\left(i+\frac{1}{2},j+1,k\right)+E_x^{n+1}\left(i+\frac{1}{2},j+1,k\right)}{2} - V_{to}\right)\right) \cdot \\
\cdot \tanh\left(\alpha \cdot \Delta y \cdot \frac{E_y^{n+1}\left(i,j+\frac{1}{2},k\right)+E_y^{n+1}\left(i,j+\frac{1}{2},k\right)}{2}\right) + \\
+\frac{C_{ds} \cdot \Delta y}{\Delta x \cdot \Delta z} \cdot \frac{E_y^{n+1}\left(i,j+\frac{1}{2},k\right)-E_y^{n+1}\left(i,j+\frac{1}{2},k\right)}{\Delta t} + \\
+\frac{\Delta y}{\Delta x \cdot \Delta z} \cdot \frac{E_y^{n+1}\left(i,j+\frac{1}{2},k\right)+E_y^{n+1}\left(i,j+\frac{1}{2},k\right)}{2 \cdot R_{ds}}
\end{aligned}
\qquad (6)
$$

Eqn (6) can be easily inserted into the FDTD-LE time marching algorithm.

3 Simulation Results

Two simple, yet realistic, examples have been conceived, involving BJTs and MeSFETs. The first one consists of a microstrip transmission line connecting two logic (ECL) gates (Fig. 3) [5]. In particular, a 35 mm-long and 0.8 mm-wide microstrip (the characteristic impedance of which is thus equal to 42 Ω) drives the signal between the two gates.

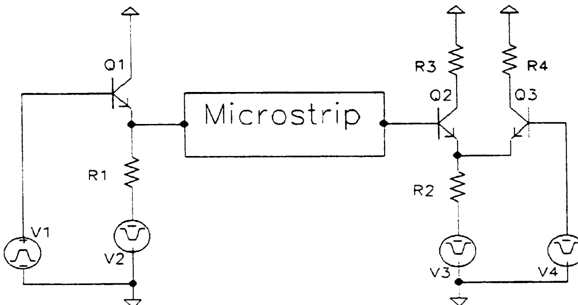

Figure 3: ECL gate interconnection: schematic view of the simulated circuit.

A graded mesh, consisting of 15x21x100 cells, has been used in this case. The cell edge size ranges from 0.1 to 1 mm; in particular, the grid has been refined close to discontinuities and lumped elements, as well as across the dielectric layer using the unidirectional graded mesh scheme [6]. The simulation aims at evaluating the influence of line mismatching on the signal propagation. The digital signal along the microstrip is first settled to its low value; to this purpose, power supplies (V_2,V_3,V_4 in Fig. 3), as well as the signal source V_1, are brought to their regime values through Gaussian voltage ramps. After such a regime has been attained, the input signal switches to its high value, that is, a voltage step ($\Delta V = 0.75$ V, $T_{rise} = 100$ ps) is applied to the base of Q_1.
Fig. 4 refers to the inverting output of the differential pair: propagation effects are made evident by ringing and overshoots of the signal. Computed results are validated against SPICE outputs.

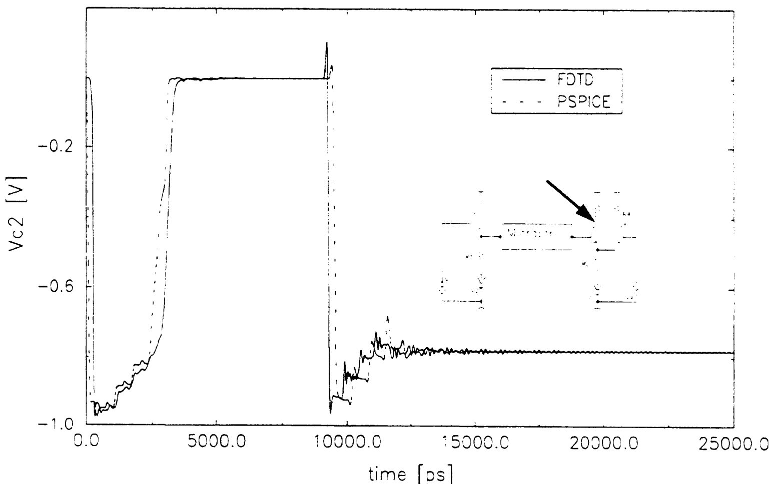

Figure 4: ECL gate interconnection: output signal at the input stage of the receiving gate (see inset).

The second example consists of a simple, microwave amplifier obtained by using a GaAs MeSFET in the common-source configuration with a passive load. Bias and signal generators are inserted into a FDTD uniform mesh (12x13x20 cells, cell size 0.2 mm) bounded by a metallic package.
Fig. 6 shows the result obtained with a sinusoidal input signal having an amplitude of 100 mV and a frequency of 1 GHz. Due to the small signal amplitude, the amplifier response shows no appreciable distortion. A voltage gain of about 7 has been obtained, in excellent agreement with that predicted by a more conventional circuit-analysis tool (HP-MDS). Fig. 7, instead, shows the amplifier response to an input signal having larger amplitude (1 V) and frequency (2 Ghz). In this case, non linearities come into play, and make the output waveform strongly distorted. Moreover, the influence of parasitics

reactances is made evident by the output delay and by the uneven behavior of rising and falling edges of the signal.

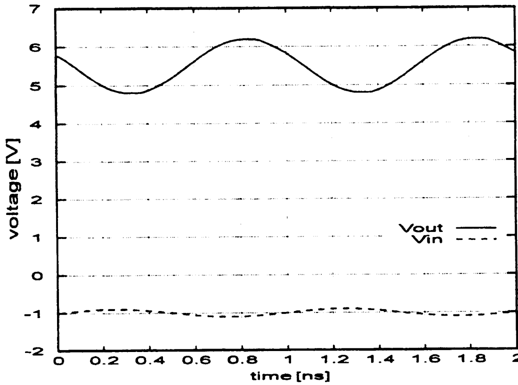

Figure 5: GaAs MeSFET amplifier response. V_{in} =.1 V, f = 1 GHz

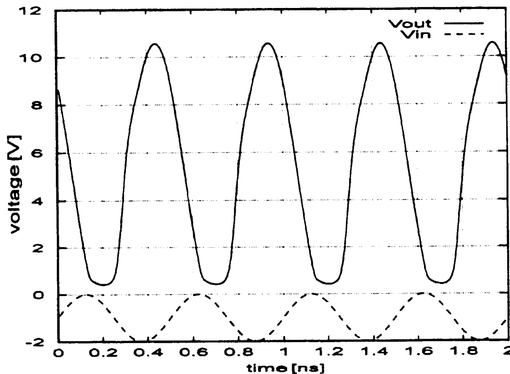

Figure 6: GaAs MeSFET amplifier response. V_{in} =1 V, f = 2 GHz

4 Conclusions

A mixed-mode circuit simulator has been developed, based on the lumped-element FDTD technique. Special care has been devoted to make it suitable for the efficient simulation of realistic circuits. In particular, accurate lumped models of active devices have been taken into account. The code is thus capable of simulating lumped BJTs, *pn* and Schottky junction diodes. Lumped resistors, capacitors and inductors, as well as independent (non ideal) voltage sources are also available In this paper we also report, for the first time, on the incorporation of the large-signal model of a GaAs MESFET into a LE-FDTD code. Simulation examples have been discussed, which highlight some of the code features. Perspective application of such a tool include analysis of several propagation and radiation effects occurring within modern high-speed analog

and digital circuits, some of which are hardly taken into account by conventional circuit CAD tools.

References

1. W. Sui, D. A. Christensen and C. H. Durney, Extending the Two-Dimensional FD-TD Method to Hybrid Electromagnetic Systems with Active and Passive Lumped Elements, IEEE Trans. MTT, vol. MTT-40, Apr. 1992, pp. 724-730.
2. K. S. Yee, Numerical Solution of Initial Boundary Value Problems Involving Maxwell's Equations in Isotropic Media, IEEE Trans. AP, vol. AP-14, May 1966, pp. 302-307.
3. M. Piket-May, A.Taflove and J. Baron, FD-TD Modeling of Digital Signal Propagation in 3-D Circuits with Passive and Active Loads, IEEE Trans. MTT., vol. MTT.-42, Aug. 1994, pp. 1514-1523.
4. V. A. Thomas, K. Ling, M. E. Jones, B. Toland, J. Lin, T. Itoh, FDTD Analysis of an Active Antenna, IEEE MGWL, vol. 4, no. 9, Sep. 1994, pp. 296-298.
5. P. Ciampolini, P. Mezzanotte, L. Roselli, R. Sorrentino, Efficient Simultion of High-Speed Digital Circuits Using Time Adaptive FD-TD Technique, 25th EuMC Proc., vol. 2, pp. 646-640, Bologna I, Sep. 1995.
6. D. H. Choi, W. J. R. Hoefer, A Graded Mesh FD-TD Algorithm for Eigenvalue Problems, 17th EuMC Proc., pp 413-417, Rome I, 1987.
7. W. R. Curtice, A Mesfet Model for Use in the Design of GaAs Integrated circuits, IEEE Trans. MTT., vol. MTT-28, 1980, pp. 488-456.