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Numerical Modeling of Linear Doping Profiles for High Voltage Thin Film SOI Devices

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Abstract

A numerical model for obtaining linear doping profiles in the drift region of high voltage thin film SOI devices is proposed and experimentally verified. Breakdown voltage in excess of 612 V on LDMOS transistors with 0.15 μm SOI layer, 2 μm buried oxide, and 50 μm drift region is designed and demonstrated using this model. Theoretical and experimental dependence of the breakdown voltage on the drift region length are compared. Good agreement between the simulation and experimental results are obtained. Dependence of the breakdown voltage on the doping density and doping concentration slope in the linearly doped drift region is also investigated experimentally. Results indicate that an optimum concentration slope is needed in order to optimize the breakdown voltage in the thin film SOI devices with a linear doping drift region. Finally, a 600 V CMOS compatible thin film SOI LDMOS process is also described.

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I. INTRODUCTION

In recent years, Silicon-On-Insulator (SOI) devices have attracted considerable attention in the area of VLSI applications due to its high speed performance, latchup immunity and superior isolation characteristics [1]. The advantage of superior isolation is also very important for Power Integrated Circuit (PIC) application as low voltage and high voltage devices are put together on the same chip. In addition, high voltage SOI devices exhibit lower on-resistance than junction isolation devices when used in high-side switching applications [2]. As the thickness of the SOI film reduces, it brings more merits to the VLSI device such as easier for isolation, higher packing density [3] and elimination of Kink effect [4]. With all these advantages, thin film SOI technology becomes very promising for PIC applications.

It has been verified theoretically and experimentally that high breakdown voltage can be achieved in thin film SOI devices with a linear doping profile in the drift region[5], [6], [7]. It is therefore important for the device designers to know how to realize the linear doping profile and be able to determine the optimum doping density for optimum breakdown and on-resistance tradeoff. In our previous work, an numerical model was presented to design and implement systematically the linear doping profile in thin film SOI high voltage devices [7]. However, no experimental results were presented for model verification. In this paper, thin film SOI LDMOS transistors designed using the model are fabricated and characterized for model verification. Furthermore, a 600 V CMOS compatible thin film SOI-LDMOS process for fabricating the devices will also be presented.

II. NUMERICAL MODELING

It was found that a continuous lateral doping profile can be achieved by using the lateral variation doping technique [8]. This technique uses a layer of oxide or photoresist with a

sequence of slit openings for masking of the impurity implantation. These slits are increasingly smaller towards the P/N^- voltage blocking junction from the N side as shown in Fig.1. The N type dopants implanted through the slits act as sources in the subsequent drive-in process. If the drive-in time is long enough, the implanted dopants will be smeared out, resulting in a continuous lateral doping profile. By optimizing the location and size of these small silt openings, a linear doping profile for high breakdown voltage can be achieved.

In order to understand the effect of the impurity distribution of a finite width impurity source described above after a diffusion process, an one-dimensional analytical model was developed [7]. The model was developed by first considering a constant total dopant Q_T of an infinitely small slit in a diffusion process with constant diffusivity. Solving the diffusion equation for the line source gives [9]

$$C_t(x,t) = \frac{Q_T}{\sqrt{\pi \times D_{Si} \times t}} \times \exp\left(\frac{-x^2}{4 \times D_{Si} \times t}\right) \tag{1}$$

where $C_t(x,t)$ is the impurity distribution along the drift region for the line source after time t, and D_{Si} is the constant diffusivity of the impurity in silicon. For a finite width impurity source, the impurity distribution $C_f(x,t)$ after drive-in can be expressed as a continuous summation of the diffusion profiles of several line sources, and each line source has a constant dopant density $N_0 d\xi$ where N_0 is the implanted impurity concentration before drive-in, $d\xi$ is the width of the line source, and ξ is the distance from the finite width impurity source. For an impurity source with a slit width of $2x_0$, impurity distribution of a finite width impurity source can be expressed as

$$C_f(x,t) = \frac{N_0}{\sqrt{\pi \times D_{Si} \times t}} \times \int_{x-x_0}^{x+x_0} \exp\left(\frac{-\xi^2}{4 \times D_{Si} \times t}\right) d\xi$$

$$= \frac{N_0}{2} \times erf\left(\frac{x + x_0}{2 \times \sqrt{D_{Si} \times t}}\right) - \frac{N_0}{2} \times erf\left(\frac{x - x_0}{2 \times \sqrt{D_{Si} \times t}}\right) \quad (2)$$

If there are more than one slit opening on the oxide mask, the resultant impurity distribution profile will be equal to R(x,t) which is the summation of all the finite impurity source, and can be expressed as

$$R(x,t) = C_{f0}(x,t) + \sum_{1}^{n} C_{fi}(x,t)$$

$$= \frac{N_0}{2} \times erf\left(\frac{x + x_0}{2 \times \sqrt{D_{Si} \times t}}\right) - \frac{N_0}{2} \times erf\left(\frac{x - x_0}{2 \times \sqrt{D_{Si} \times t}}\right) +$$

$$\sum_{1}^{n} \frac{N_0}{2} \times erf\left(\frac{x - x_0 - A_{i-1}}{2 \times \sqrt{D_{Si} \times t}}\right) - \frac{N_0}{2} \times erf\left(\frac{x - x_0 - A_{i-1} - x_i}{2 \times \sqrt{D_{Si} \times t}}\right) \quad (3)$$

where A_{i-1} is the distance between two adjacent slits, x_i is the size of the i-th slit opening as shown in Fig.1a, $C_{f0}(x,t)$ and $C_{fi}(x,t)$ are the impurity concentration of the first and the i-th impurity source after diffusion time t. Using the lateral variation doping technique, an impurity profile can be obtained as described by Eq.(3).

An algorithm was developed to obtain systematically the design parameters (i.e. x_i, A_{i-1}, and the number of slits) for implementing the optimum linear doping profile [7]. The design parameters can be obtained by matching the resultant impurity distribution profile R(x,t) from Eq.(3) with an ideal doping profile $C_{opt}(x)$ for all values of x. To implement this matching methodology, a computer program was developed [7]. The program is divided into three parts. The first part of the program determines the design parameters for the first and second slits. The second part is then used to determine the design parameters for the other slits except the last one. Finally, the program will determine the design parameters for the last slit. Once the optimum linear doping profile is obtained, breakdown voltage of the device can be obtained

either numerically by MEDICI [10] or experimentally. Values of the design parameters obtained from the program for implementing the linear doping profiles for devices with different drift region lengths are listed in Table 1.

III. FABRICATION PROCESS

A 600 V CMOS compatible thin film SOI LDMOS process is designed and implemented. The various processing steps are designed using the two-dimensional simulator TSUPREM [11]. The starting SOI substrates have a 0.15 μm thick silicon layer and a 2 μm thick buried oxide. The background doping concentration of the silicon layer is 1×10^{15} cm^{-3} . The simplified process flow is illustrated in Fig.2 and described as follows.

The process begins by silicon mesas formation using reactive ion etching. After that, a 0.1 μm thick LTO (lower temperature oxide) is deposited, and following that is photoresist deposition. The drift region mask is then used to define the slit width and slit spacing on the photoresist as shown in Fig.2a. Following that is the phosphorous implantation into the SOI layer to form the drift region. The implantation energy is 60 KeV, and different dosages are selected to determine experimentally the dependence of the breakdown voltage on the doping density in the linearly doped drift region. The dosages used are ranging from 3.6×10^{12} cm^{-2} to 6×10^{12} cm^{-2}. After photoresist striping, a 0.4 μm thick LTO is deposited to prevent impurity out-diffusion into the ambient during the drive-in step. The drive-in step is performed in an inert ambient for 580 minutes at 1200^0C to smear-out the impurity for obtaining a linear doping profile along the drift region.

After the drift drive-in, the gate region is defined along with the opening of the drain region. A gate oxide of 500 Å is then grown thermally. Following that, a 0.5 μm Poly-Si for gate electrode is deposited by LPCVD. After the gate is defined, the P channel region is

formed by a self-aligned boron implantation and a subsequent drive-in step as shown in Fig.2b. The dose and energy for the boron implantation are 4×10^{12} cm^{-2} and 33 KeV, respectively, and the temperature and time for the drive-in are 1100^0C and 120 minutes, respectively. Next, a phosphorous implantation is carried out to dope the drain and source regions. The dose and energy are 7×10^{14} cm^{-2} and 90 KeV, respectively. After this, the P^{++} region is defined, and boron is implanted to form segmented source for the P-channel region contact as shown in Fig.2c. The dose and energy are 4×10^{15} cm^{-2} and 33 KeV, respectively.

Finally, a 0.5 μm thick LTO is deposited, and the contact holes to gate, source, and drain are defined after the LTO densification at 950^0C for 30 minutes. The metallization is followed by sputtering of Al/Si (99:1) to form metal electrodes as shown in Fig.2d. The wafers are then sintered at 400^0C for 30 minutes.

IV. RESULTS AND DISCUSSION

Fig.3 shows the micrograph of an experimental thin film SOI LDMOS transistor fabricated using the above process. Transistors with drift region lengths of 30, 40, and 50 μm are obtained. Fig.4 shows the forward conduction characteristics of the LDMOS transistor with a drift region length of 50 μm, SOI thickness of 0.15 μm, and buried oxide thickness of 2 μm. The transistor has a threshold voltage of 1.6 V, an active area of 0.12 mm^2, and a specific on-resistance of about 50 $\Omega.mm^2$. The drain to source breakdown characteristic of the transistor is shown in Fig.5 with a breakdown voltage in excess of 612 V.

Fig.6 shows the experimental dependence of the breakdown voltage on the drift region length. The breakdown voltage of the transistors with drift region lengths of 30, 40, and 50 μm are 421, 540, and 612 V, respectively. All the transistors are with a SOI thickness of 0.15 μm and buried oxide thickness of 2 μm. The simulated breakdown voltages obtained using the

model in Section II are also shown for comparison. Very good agreement between experimental and simulation results are obtained. These results are also consistent with those reported in earlier works [5], [12].

Fig.7 shows the experimental dependence of the breakdown voltage on the doping density in the linearly doped drift region with drift lengths of 30, 40, and 50 μm. The doping density in the drift region was calculated by multiplying the total implantation dose with the ratio of the slit width to the total drift length. It can be seen from Fig.7 that breakdown voltage increases with the increase in the doping density in the drift region up to a maximum value, and then reduces with further increase in the doping density. On the other hand, the slope of the linear doping profile, G, in the drift region can be expressed by obtaining the area under the concentration versus distance plot (Fig.1b) as

$$G = \frac{2}{W}\left(\frac{Q_d}{t_s}\right) \tag{4}$$

where Q_d is the doping density in the drift region, W is the drift region length and t_s is the SOI film thickness. Since the background doping in the drift region is much less than Q_d, it is ignored in the above expression. Fig.8 shows the experimental dependence of the breakdown voltage on the slope of the linear profile, G, for drift lengths of 30, 40, and 50 μm. Results indicate that the optimum breakdown voltage for the different drift lengths are obtained at a similar concentration slope. The relationship between the breakdown voltage and the doping density (also the concentration slop) can be explained as follows.

A cross section of the transistor defining the various dimensions is shown in Fig.9. This structure is used to obtain the dependence of the lateral electric field in the drift region on the doping density and the slope of the linear doping profile. The vertical component of the electric field $E_y(x,y)$ in the drift region and the potential ψ (x,0) at the top surface of the drift

region can be expressed as [5]

$$E_y(x,y) = \frac{qN(x)}{K_s \varepsilon_o} y \quad , \quad \text{and} \tag{5}$$

$$\psi(x,0) = (\frac{t_s}{2} + \frac{K_s}{K_{ox}} t_{ox}) E_y(x,t_s) \, , \tag{6}$$

respectively, for $0<x<W$ and $0<y<t_s$. K_s and K_{ox} are the relative permitivities of silicon and silicon dioxide, respectively, N(x) is the impurity concentration in the drift region, and t_s and t_{ox} are the thickness of the SOI and buried oxide layers, respectively. From Eq.(5), we have

$$E_y(x,t_s) = \frac{qN(x)}{K_s \varepsilon_o} t_s \tag{7}$$

Substituting Eq.(7) into (6) we have

$$\psi(x,0) = \frac{qN(x)}{K_s \varepsilon_o} (\frac{t_s}{2} + \frac{K_s}{K_{ox}} t_{ox}) t_s \tag{8}$$

Differentiating Eq.(8) we have

$$E_x(x,0) = \frac{qt_s}{K_s \varepsilon_o} (\frac{t_s}{2} + \frac{K_s}{K_{ox}} t_{ox}) \frac{d}{dx} N(x) \tag{9}$$

Since dN(x)/dx is the slope of the doping profile (G) in the drift region, $E_x(x,0)$ is proportional to the slope of the doping profile, and also proportional to the doping density in the linearly doped drift region as defined in Eq.(4). Thus when the doping density is low, the lateral electrical field established along the drift region will cause the depletion layer to extend to the N^+ drain region at a relatively lower voltage. After the depletion layer reaches the N^+ region, a high electric field is established at the N/N^+ junction due to field crowding at the N^+ region. Further increase in the applied voltage will cause device breakdown, resulting in a low breakdown voltage. On the other hand, as the doping density is increased, a higher and uniform electric filed can be established along the drift region. Thus, a higher breakdown

voltage can be obtained. The doping density should be high enough so that optimum breakdown is occurred when the depletion layer reaches the N^+ drain. Any increase in doping density beyond this value will result in a high electric field built up along the drift region (as given by Eq.(9)). In such case, breakdown occurs before the depletion region reaches the N^+ drain region, again resulting in a non-optimum breakdown voltage.

V. CONCLUSION

A systematic approach to design and implement high voltage thin-film SOI devices with linear doping profile in the drift region is proposed. The validity of the approach is verified experimentally in this work. Breakdown voltages in excess of 612, 540, and 425 V are obtained for the LDMOS transistors with drift region length of 50, 40, and 30 μm, respectively. All of the transistors are with a SOI thickness of 0.15 μm and buried oxide thickness of 2 μm. Dependence of the breakdown voltage on the doping density and concentration slope in the linearly doped drift region are investigated. The results indicate that in order to obtain the optimum breakdown voltage, the doping density or concentration slope in the drift region has to be optimized. The systematic approach provided in this paper allows this optimization to be done efficiently.

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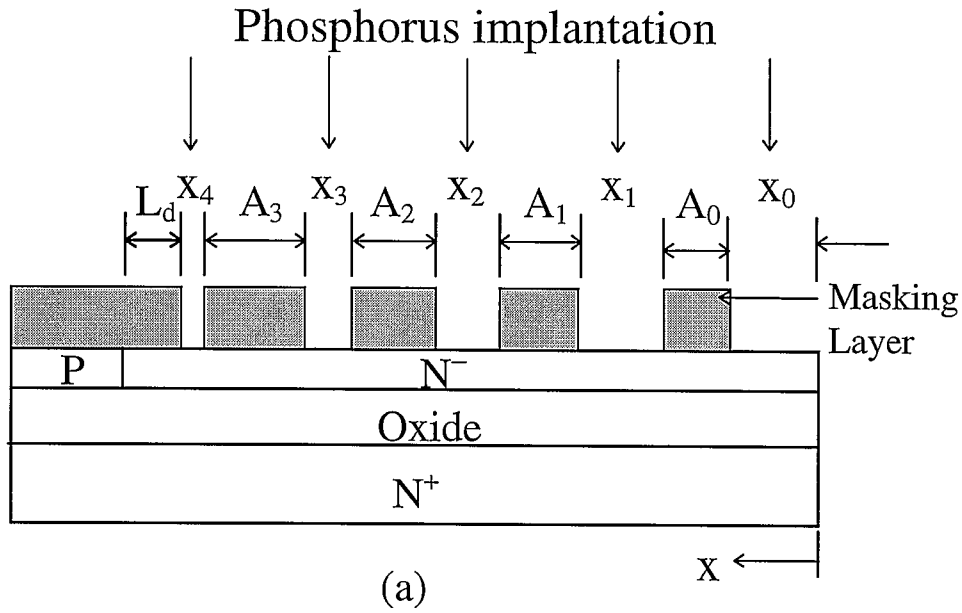
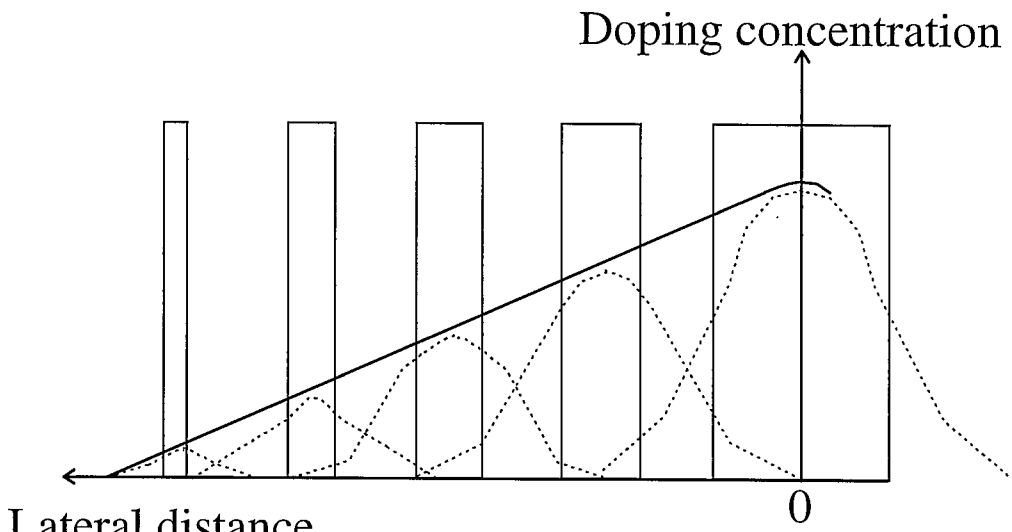
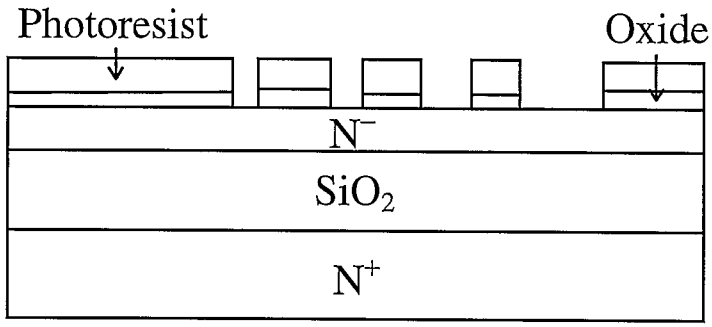

Phosphorus implantation
L_d
x_4
A_3
x_3
A_2
x_2
A_1
x_1
A_0
x_0
Masking Layer
P
N^-
Oxide
N^+
x

(a)

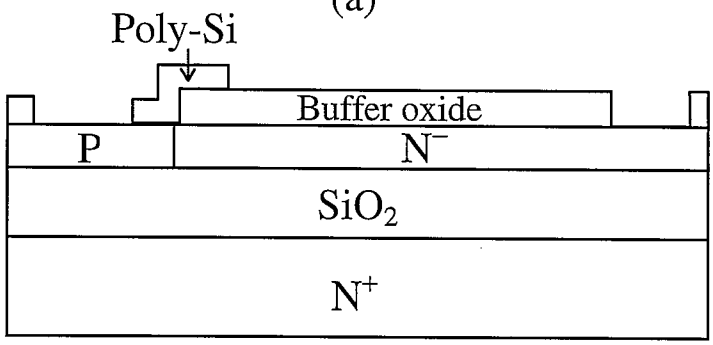

Doping concentration
Lateral distance
0

(b)

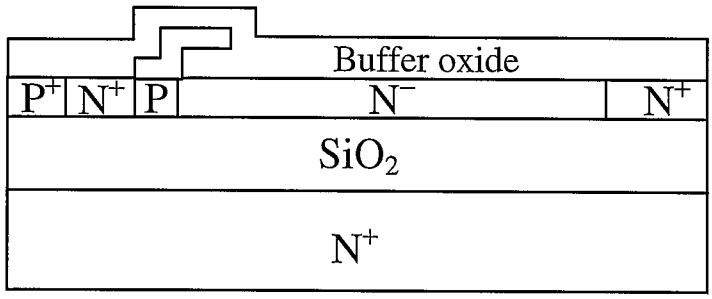
Fig. 1


Photoresist
Oxide
N⁻
SiO2
N+

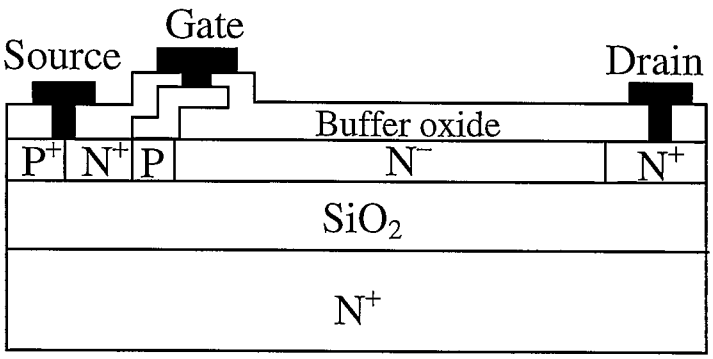
(a)


Poly-Si
Buffer oxide
P
N⁻
SiO2
N+

(b)


Buffer oxide
P+
N+
P
N⁻
N+
SiO2
N+

(c)


Gate
Source
Drain
Buffer oxide
P+
N+
P
N⁻
N+
SiO2
N+

(d)

Fig. 2

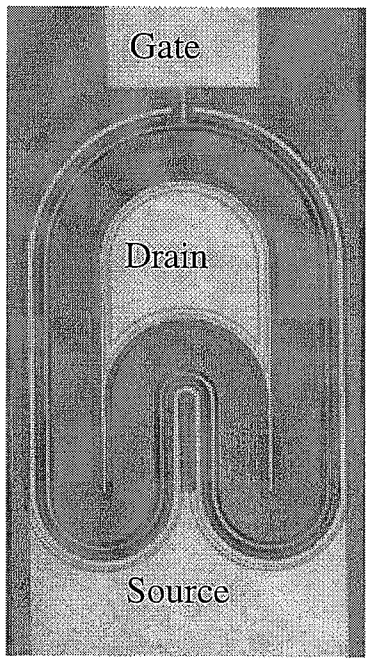


Fig. 3

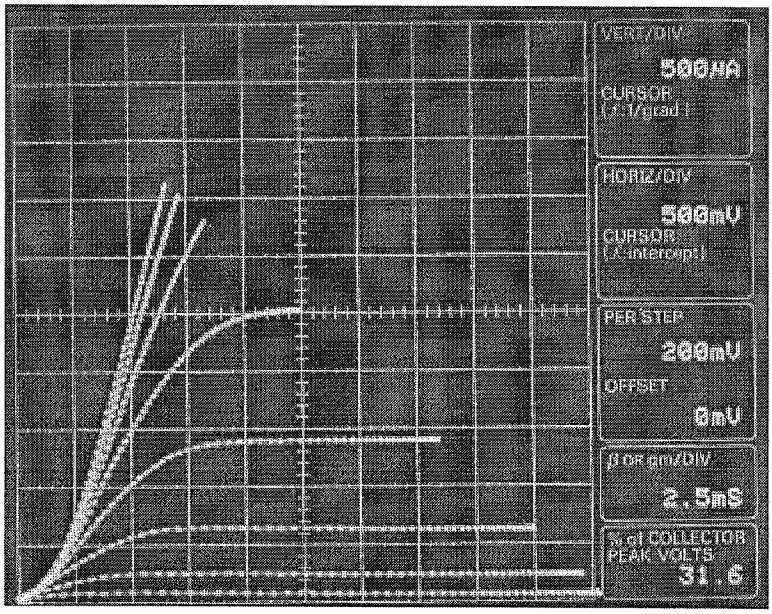
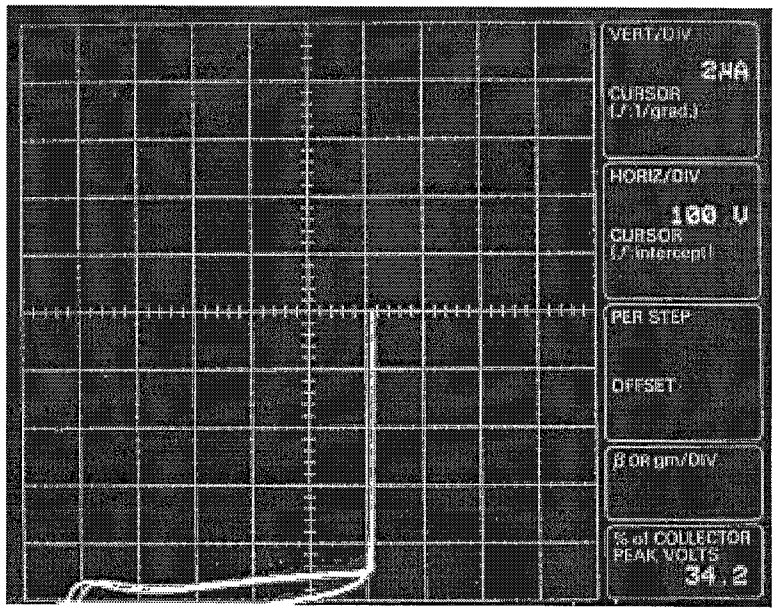

VERT/DIV
500uA
CURSOR
HORIZ/DIV
500mV
CURSOR
PER STEP
200mV
OFFSET
0mV
2.5mS
COLLECTOR
PEAK VOLTS
31.6

Fig. 4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2mA
CURSOR
[/1/grad.]
HORIZ/DIV
100 V
CURSOR
[/ Intercept]
PER STEP
OFFSET
β OR gm/DIV
COLLECTOR
PEAK VOLTS
34.2

Fig. 5

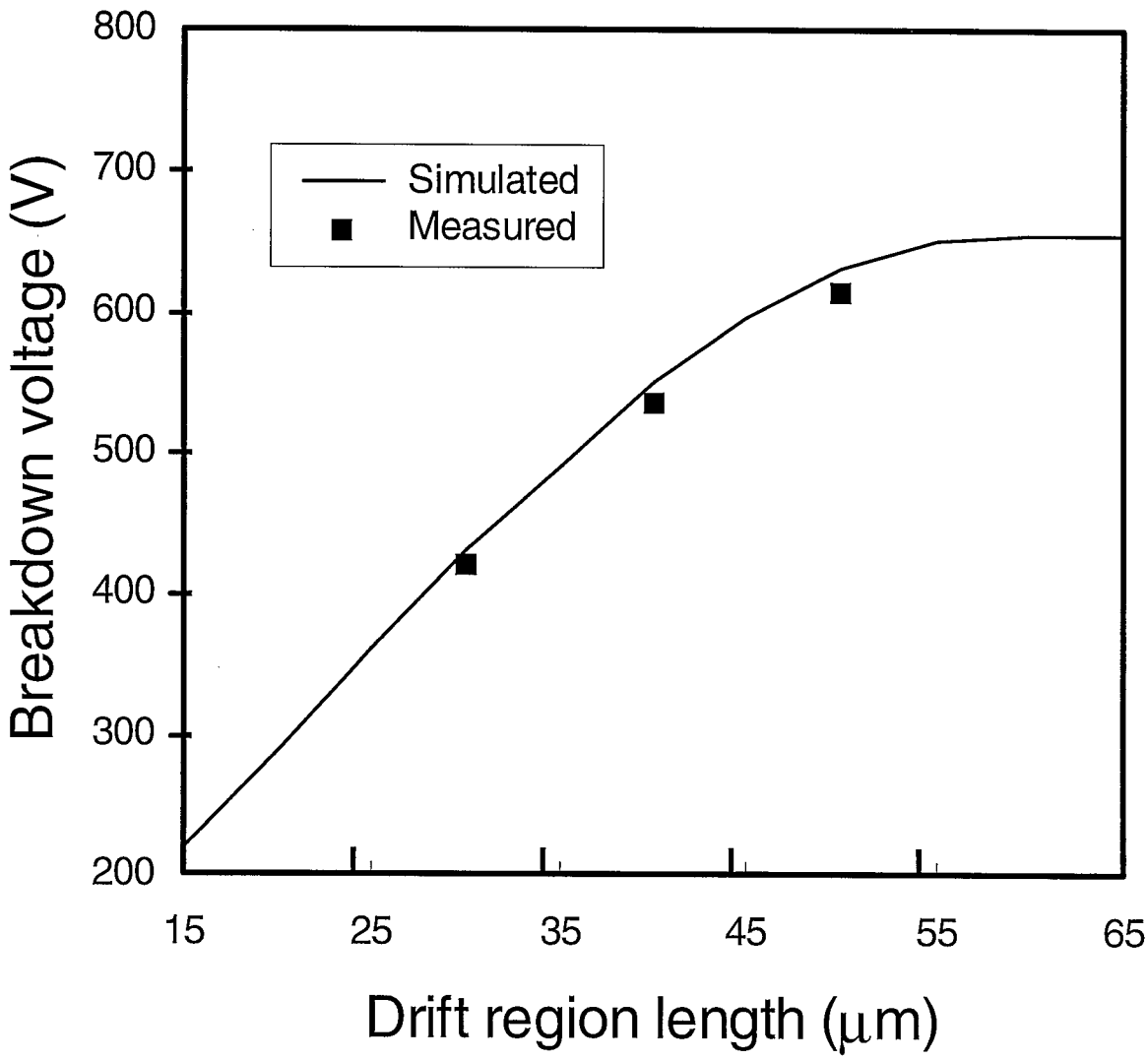
800
700
600
500
400
300
200
Breakdown voltage (V)
Simulated
Measured
15
25
35
45
55
65
Drift region length (μm)

Fig. 6

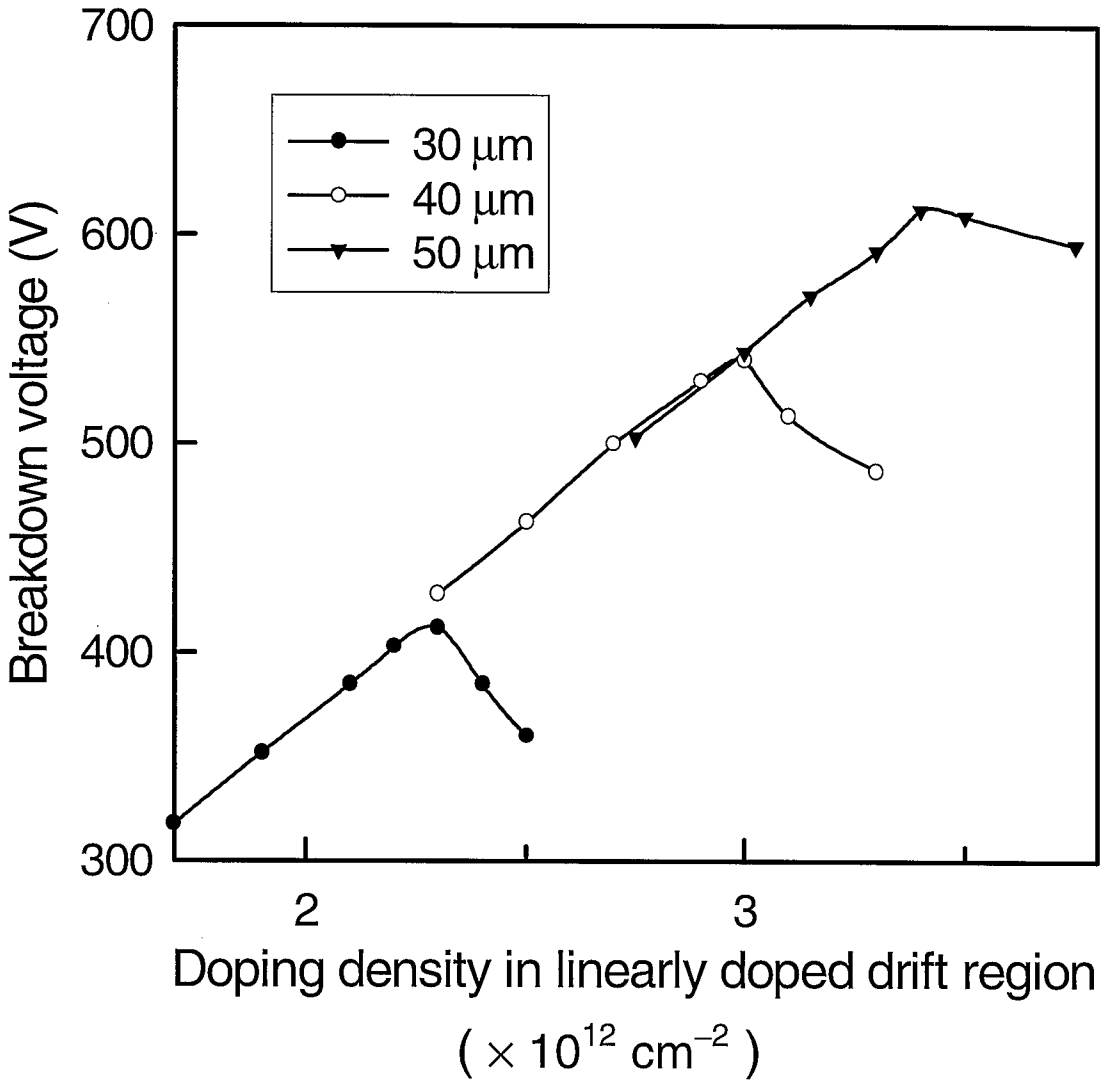
700
600
500
400
300
Breakdown voltage (V)
30 μm
40 μm
50 μm
2
3
Doping density in linearly doped drift region
(× 10^12 cm^−2)

Fig. 7

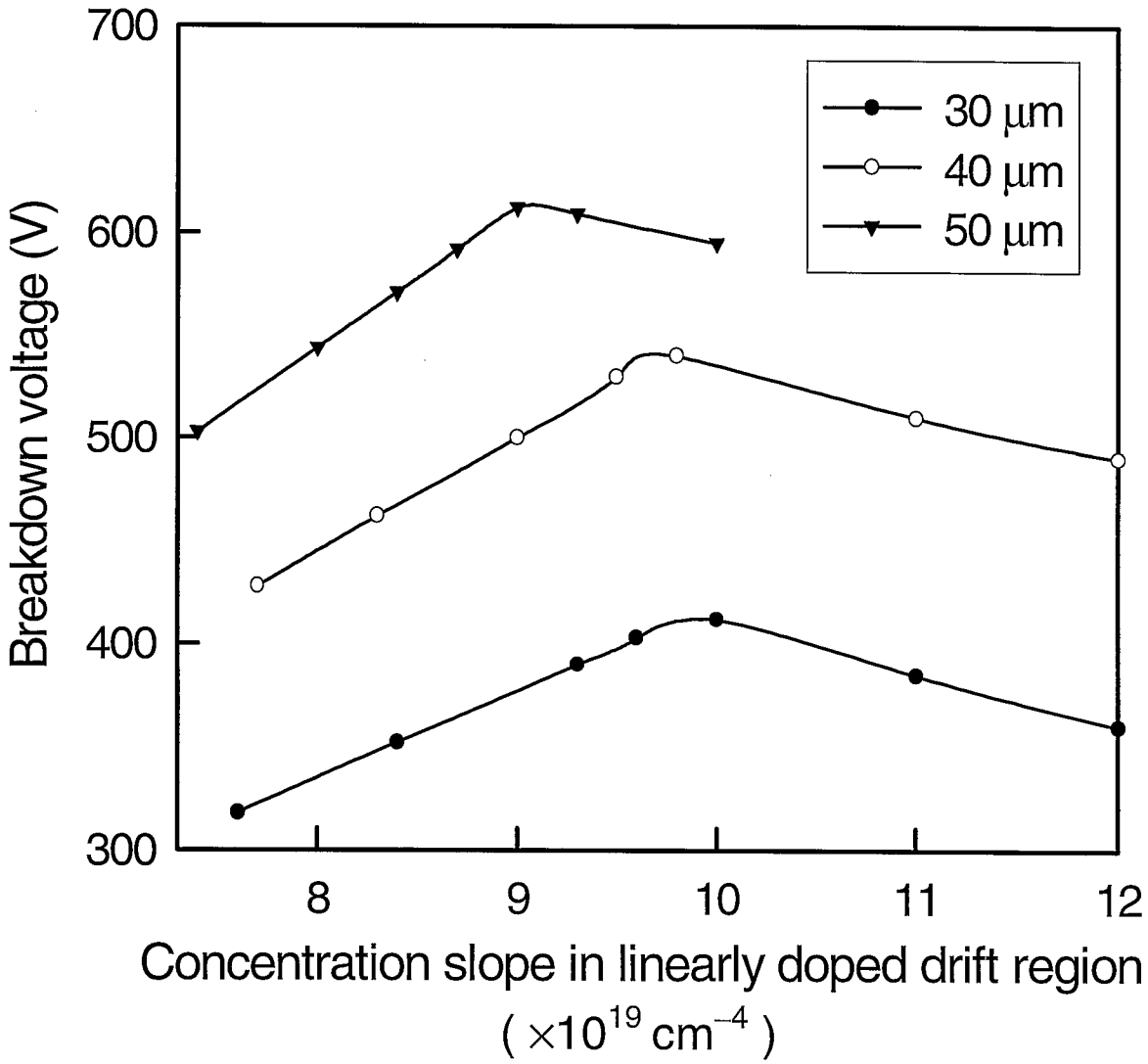
700
600
500
400
300
Breakdown voltage (V)
30 μm
40 μm
50 μm
8
9
10
11
12
Concentration slope in linearly doped drift region
(×10^19 cm^-4)

Fig. 8