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Observation of Dynamic V TH of p-GaN Gate HEMTs by Fast Sweeping Characterization

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Observation of Dynamic V_{TH} of p-GaN Gate HEMTs by Fast Sweeping Characterization

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***Abstract*— In this work, fast sweeping characterization with an extremely short relaxation time was used to probe the V_{TH} instability of p-GaN gate HEMTs. As the I_D-V_G sweeping time deceases from 5 ms to 5 μs, the V_{TH} dramatically degenerates from 3.13 V to 1.76 V, meanwhile the hysteresis deteriorates from 22.6 mV to 1.37 V. Positive bias temperature instability (PBTI) measurement by fast sweeping shows the V_{TH} features a very fast shifting process but a slower recovering process. D-mode HEMTs counterpart without Mg contamination demonstrates a negligible V_{TH} shift and hysteresis, proving the V_{TH} instability is probably due to the ionization of acceptor-like traps in the p-GaN depletion region. Finally, the V_{TH} instability is verified by a GaN circuit under switching stress. The V_{TH} instability under different sweeping speed uncovers the fact that the high V_{TH} by conventionally slow DC measurements is probably artificial. The DC V_{TH} should be high enough to avoid HEMT faulty turn-on.**

***Index Terms*— p-GaN gate HEMT, fast sweeping, V_{TH} shift, PBTI.**

I. Introduction

ENHANCEMENT-MODE p-GaN gate HEMTs featuring a low gate charge Q_g, a low on-resistance, and a fast switching capability have been penetrating the market of power electronics for years [1]–[3]. GaN power HEMTs are however vulnerable to faulty turn-on because of the fast switching characteristics. As shown by the bootstrap half-bridge circuitry in Fig. 1, after the low side (LS) switches OFF and the high side (HS) switches ON, the V_{DS} of the LS switch will quickly soar to $\sim V_{IN}$ from 0 V within tens of nanoseconds. This swift voltage transient creates a miller current through the Miller capacitor C_{DG} and the gate loop, inducing a gate voltage spike that in turn can falsely switch ON the LS switch [4].

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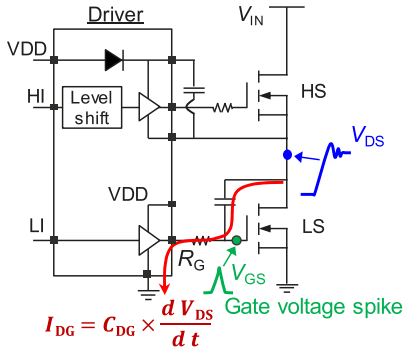

Fig. 1. Schematic of a bootstrap half-bridge configuration, and the fast switching transient of HS device induces miller current that can result in faulty turn-on of the LS.

Suppressing the faulty turn-on necessitates a high threshold voltage V_{TH}, therefore some Schottky gate HEMTs have been adopted to boost the V_{TH} to above 2.5 V. Nevertheless, the V_{TH} instability of the Schottky gate has been widely reported [5]–[9]. Generally, the V_{TH} instability is ascribed to several competing mechanisms occurring in the p-GaN/AlGaN stack, i.e., electron trapping, hole injection, and hole depletion. Tang *et al.* reported a V_{TH} positive shift at < 7 V V_{GS} stress due to electron trapping at the p-GaN/AlGaN interface, and V_{TH} decreases at > 7 V V_{GS} stress because of the hole injection/electroluminescence (EL) [10]. Similar phenomena have also been observed with fast sweeping technique by Stockman *et al.* who claimed the electron trapping happens at the AlGaN/GaN interface whereas holes accumulate at the p-GaN/AlGaN interface or are trapped in the barrier layer [11]. He *et al.* [12] however demonstrated a monotonous positive V_{TH} shift with fast-dynamic-stress method by a resistive-load setup [13]. Recently, more attention has been paid to use fast speed characterization to probe the V_{TH} instability [5], [11].

In this work, the V_{TH} instability will be investigated by a new fast sweeping characterization. The I_D-V_G hysteresis, V_{TH} shifting and recovery process, and the positive bias temperature instability (PBTI) will all be precisely probed, which provides some novel results undiscovered by conventional DC sweeping characterization.

II. Epitaxy, Fabrication, and Circuit

The pGaN/AlGaN/GaN structure was epitaxially grown using a metalorganic chemical vapor deposition (MOCVD) on 200 mm GaN-on-Si substrates. The epi stack consists of a 200 nm AlN nucleation layer, a 1.65 μm (Al)GaN superlattice

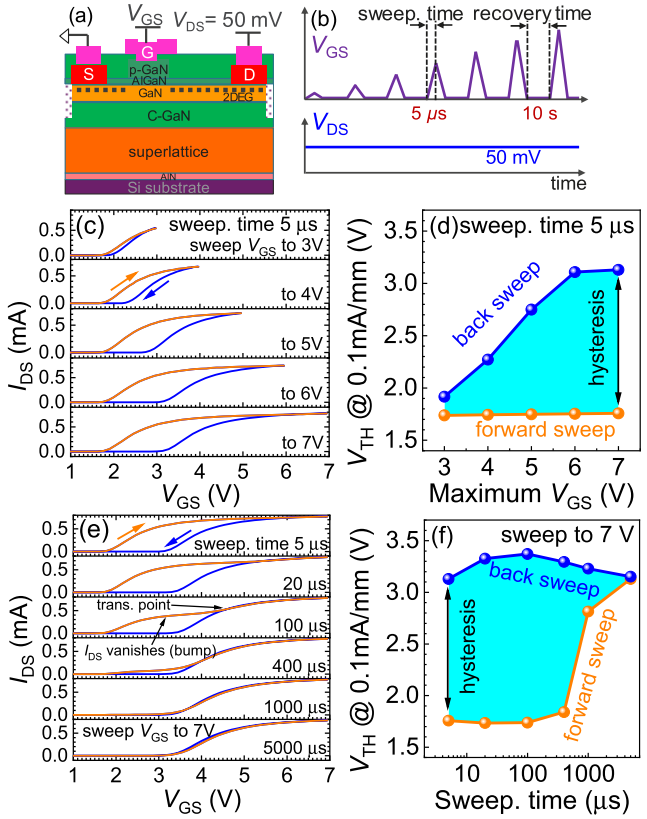

Fig. 2. (a) Cross-sectional schematic of the measured p-GaN gate HEMTs, (b) test waveforms, (c) I_D-V_G curves and (d) V_{TH} of the devices swept to various maximum V_{GS}, and (e) I_D-V_G curves and (f) V_{TH} of the devices under various sweeping times of 5 μs, 20 μs, 100 μs, 400 μs, 1000 μs, and 5000 μs.

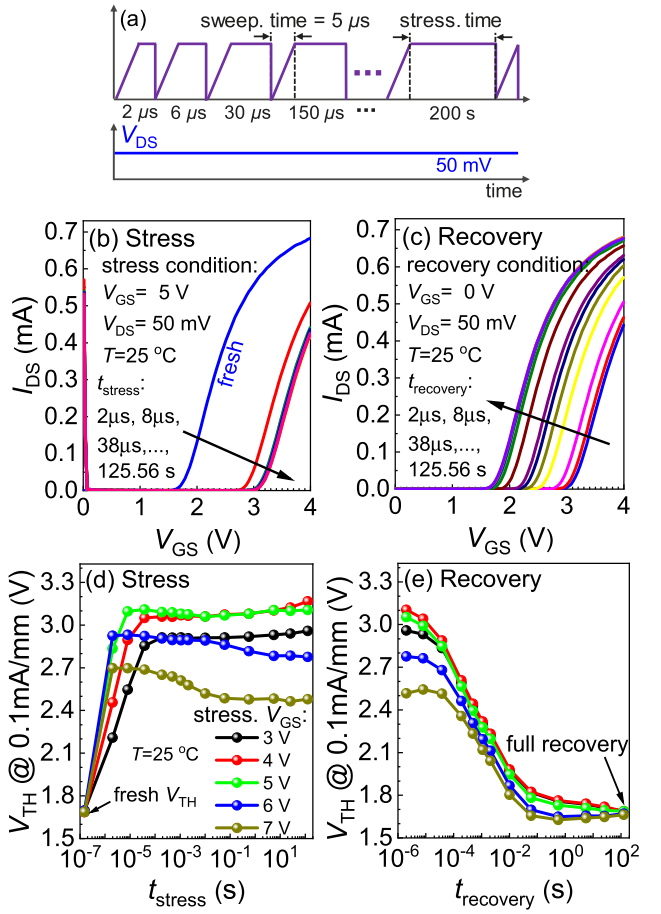

Fig. 3. (a) Sketches of PBTI measurement sequences by fast sweeping of 5 μs in this work, I_D-V_G curves during the (b) stress phase and (c) recovery phase by stress V_{GS} of 5 V, and V_{TH} evolution under different stress V_{GS} from 3 to 7 V during the (d) stress phase and (e) recovery phase at 25 °C. The sensing V_{GS} sweeps from 0 to 4 V in 5 μs.

layer, a 1 μm carbon-doped GaN back barrier, a 400 nm undoped GaN channel layer, a 12.5 nm $Al_{0.235}GaN$ barrier layer, and a 80 nm Mg-doped p-GaN layer with a dopant concentration of $\sim 3\times10^{19}$ cm^{-3}. The processing details have been elaborated in [14]–[16]. The measured p-GaN gate HEMTs as shown in Fig. 2(a) have a gate width W_G of 100 μm, a gate length L_G of 1.3 μm, a gate-source distance L_{GS} of 0.5 μm, and a gate-drain distance L_{GD} of 5.75 μm. The fast sweeping characterization is performed using a Keysight B1530A WGFMU (Waveform Generator/ Fast Measurement Unit). Fig. 2(b) documents an example of the test waveform: the ultra-fast transient (down to ~2 μs) is enabled by a 50 Ω output impedance in WGFMU which prevents reflection-induced waveform degradation. The function generator is an Agilent 81110A and the oscilloscope is a LeCroy HDO6054.

III. Results and Discussion

The HEMTs were first subjected to double fast sweeping characterization. Fig. 2 (b) shows the V_{DS} was fixed at 50 mV and the V_{GS} swept from 0 V to a higher voltage and then back to 0 V. Between each double sweeping, 10 s relaxation time was inserted to ensure a full recovery of the V_{TH} shift. Sweeping speeds are defined by the single sweeping time ranging from 5 μs to 5000 μs. Fig. 2 (c) and (d) show that a significant V_{TH} hysteresis of up to 1.37 V is observed for the maximum V_{GS} of 7 V, for the sweeping time of 5 μs. By increasing the sweeping time, a transition point emerges on the forward sweep curve as shown in Fig. 2 (e), inducing a current bump observed previously [17]. The high current before this point gradually vanishes when sweeping time reaches 1000 μs, thus inducing an arbitrarily high V_{TH} as the conventional DC sweeping.

PBTI measurements were then conducted to investigate the V_{TH} behavior during the gate stress and recovery phases by the fast sweeping characterization. During the measurement, as demonstrated in Fig. 3(a), the stress was periodically interrupted to measure the I_D-V_G characteristics by sweeping the V_{GS} from 0 to 4 V in 5 μs (Fig. 3 (b)). The recovery behavior was monitored similarly except the V_{GS} was 0 V. The V_{TH} relaxation is ubiquitous in BTI stressing [18]. Improper sampling precision might induce a fake conclusion [12]. In this work, the relaxation time between the stress and sense was limited to as short as 50 ns. Fig. 3 (d) shows that the V_{TH} under lower stress V_{GS} of 3 V takes ~200 μs to saturate. In contrast, only ~2 μs has been enough for the stress V_{GS} of 6 V. Compared with the shifting process, the recovery process is much slower. Importantly, the V_{TH} shift is fully recoverable as shown in Fig. 3(e). It is worth to mention that

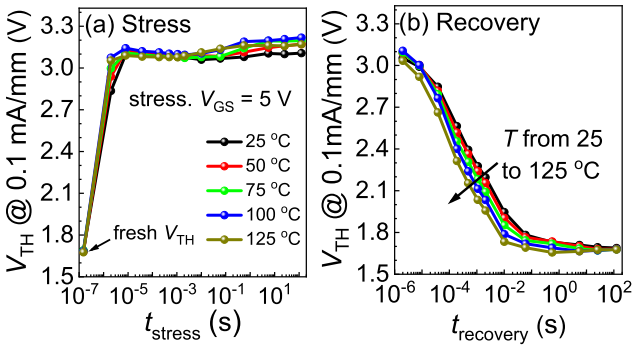

Fig. 4. Temperature-dependent V_{TH} evolution under stress V_{GS} of 5 V during the (a) stress and (b) recovery phases at the temperatures from 25 to 125 °C. The sensing V_{GS} sweeps from 0 to 4 V in 5 μs.

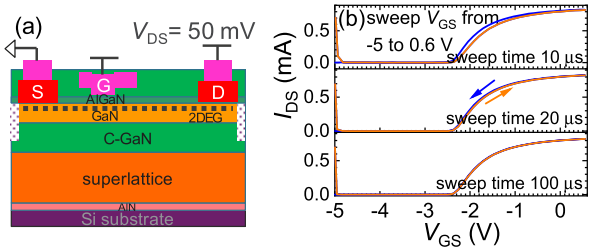

Fig. 5. (a) Cross-sectional schematic and (b) double-sweep I_D-V_G curves on the D-mode HEMTs on a D-mode epitaxy wafer without Mg contamination.

the V_{TH} will be very stable after the initial stress in application before shutdown, considering the operation V_{GS} in power ICs is around 5 V.

Temperature-dependent PBTI measurement results are demonstrated in Fig. 4. The impact of temperature on the V_{TH} shift is not clearly discernable because of the very fast trapping process as shown in Fig. 4(a). Fig. 4 (b) shows that the recovery can be facilitated by high temperatures.

Locating the cause for the dynamic V_{TH} is very challenging. Counterpart depletion-mode (D-mode) HEMTs on a D-mode epitaxy wafer were characterized, as shown in Fig. 5(a). The D-mode wafer has a similar superlattice buffer layer, but the epitaxy terminates after the AlGaN barrier and a thin GaN cap layer, without the p-GaN layer nor Mg out-diffusion in the AlGaN barrier and GaN channel [19]. Fig 5(b) shows a negligible hysteresis and V_{TH} shift, proving that the V_{TH} instability is a signature of the p-GaN, probably via the trapping by Mg or related impurities/complexes.

There have been plenty of reports about the enormous acceptor-like traps in the p-GaN layer above the top of the valence band [20]–[24], which are however ignored by the previous research on p-GaN gate HEMTs. Activated but unionized Mg, Mg-H complex, Mg-N-H complex, and other Mg-related traps are all possibly responsible for the V_{TH} shift. As shown in Fig. 6, when the gate is positively biased and the depletion region extended, those acceptor-like traps in the p-GaN depletion region will be quickly ionized and release holes to the valence band. After the positive bias is removed, these ionized traps cannot be quickly deionized, inducing a positively shifted V_{TH}. The V_{TH} decrease for stress V_{GS} of 6 and 7 V is possibly due to donor traps ionization or hole accumulation.

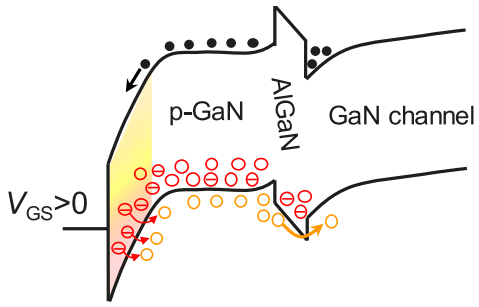

Fig. 6. Schematic band diagram of the metal/p-GaN/AlGaN/GaN gate-stack under a positive gate bias. The acceptor-like traps in the depletion region (shaded region) will be ionized and induce net negative charges in the p-GaN layer, after removing the gate bias these traps cannot be quickly deionized.

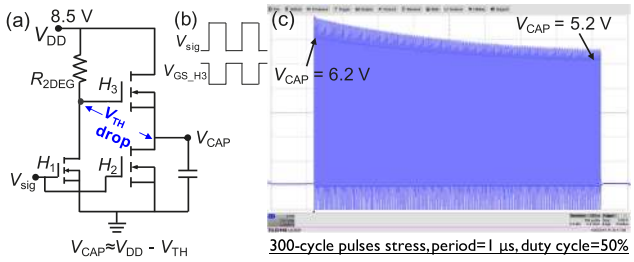

Fig. 7. (a) Schematic of the GaN IC to test the V_{TH} evolution under 1 MHz switching stress, (b) waveforms of the V_{sig} and V_{GS_H3}, and (c) switching waveform of V_{CAP} during the 1 MHz, 300 μs stress shows the V_{CAP} decrease from 6.2 to 5.2 V.

A GaN IC as sketched in Fig. 7(a) was submitted to a 1 MHz and 50% duty cycle switching stress test to verify the appearance of a dynamic V_{TH} in a realistic application. This GaN IC is an integrated push-pull gate driver [25]. The IC was powered by V_{DD} of 8.5 V and the small signal V_{sig} was sent to the IC, such that the H_3 was periodically stressed as shown in Fig. 7(b). The capacitor voltage V_{CAP} was monitored so that the V_{TH} evolution can be estimated by V_{DD}-V_{CAP}. Fig. 7 (c) shows that the V_{CAP} gradually decreased from 6.2 to 5.2 V after 300 μs stress, indicating that the V_{TH} evolved from an initial value of 2.3 V to a stable value of 3.3 V. The saturation time of 300 μs is longer than that of the stress V_{GS} of 3 V in Fig. 3(d), because the initial stress V_{GS} in Fig. 7 is even lower than 3 V. This test directly demonstrates the evolution of the dynamic V_{TH} of p-GaN gate HEMTs.

IV. Conclusion

A new methodology of fast sweeping characterization with a short relaxation time of 50 ns has been implemented to characterize the V_{TH} instability of p-GaN gate HEMTs. The V_{TH} decrease and I_D-V_G hysteresis deterioration are more significant than ever reported, showing that the conventional DC sweeping gives an artificially high V_{TH} and small hysteresis. PBTI measurements indicate the p-GaN gate has a fast V_{TH} shifting process and a slower recovery process. The V_{TH} shift has been proved to be fully recoverable. The fast shifting behaviors however guarantee the stability of p-GaN gate HEMTs in applications after a short initial stress by V_{GS} of 5 V before circuit shutdown. Nevertheless, the low fresh V_{TH} at the starting phase can trigger faulty turn-on, which poses a challenge to the gate driver design.

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