Observation of quantum effects and Coulomb blockade in silicon quantum-dot transistors at temperatures over 100 K

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We report the fabrication and characterization of lithographically defined nanoscale silicon quantum-dot transistors that operate at temperatures over 100 K and a bias higher than 0.07 V. In the tunneling regime, these transistors show strong current oscillations due to quantum confinement and single-electron charging effects. In the propagating regime, a different kind of current modulation has been observed, which is attributed to the interference between different modes of quantum waves in a cavity. Proper scaling of these transistors should lead to operation at room temperature and a bias of 0.3 V. © *1995 American Institute of Physics.*

Quantum and single electron charging effects are bringing new functionalities into transistors. The new transistors can reduce the number of transistors per circuit function and open up opportunities for innovative architectures.[1,2] However, in field effect transistors, manifestation of quantum effects and single-electron Coulomb blockade usually requires extremely low temperatures such as sub-liquid helium temperatures. Furthermore, the quantum effect and Coulomb blockade transistors are typically fabricated in III–V compound semiconductors instead of Si—the backbone material of the integrated circuit (IC) industry. To make the quantum effects and single-electron Coulomb blockade transistors practical for circuits application, the room-temperature operation and made-in-silicon are essential. This can be achieved if the silicon transistors have a feature size of about 10 nm. Here, we report the fabrication and characterization of lithographically defined nanoscale silicon quantum-dot transistors (QDT) that demonstrate quantum effects as well as single electron Coulomb blockade at temperatures over 100 K. They are also the first Si transistor that shows interference between different modes of quantum waves in a cavity. Proper scaling of such quantum-dot transistors should lead to room-temperature operation.

As shown in Fig. 1, the transistors were fabricated on (100) SIMOX (separation by implanted oxygen) silicon wafers with the top silicon layer of 60 nm thick. The channel, having an abacus bead shape, was etched into the top Si layer with chlorine based RIE (reactive ion etching) after EBL (*e*-beam lithography). PMMA (polymethylmethacrylate) resist was used for the EBL. The bead defines the quantum dot which is connected to the source and the drain through two constrictions. The channel has a similar shape as that of the QDT in III–V compound semiconductors.[3] By using *e*-beam lithography instead of stress dependent oxidation to define the quantum dot,[4] the size and shape of the dot can be better controlled. Following the 400 Å gate oxide growth at 1000 °C, which reduced the size of the silicon quantum dot and constrictions, a rectangular plain polysilicon gate was fabricated to cover the entire abacus bead channel. The high-temperature oxidation also annealed any damages that occurred during RIE. QDTs with various sizes were fabricated; the smallest Si dot diameter achieved after oxidation is estimated to be 20 nm from the scanning electron microscopy (SEM) pictures.

The transistors have two operation regimes. First is the tunneling regime. When the gate voltage is not significantly larger than the transistor's threshold voltage, the Fermi level is below the potential barriers of the double constrictions. Thus the silicon quantum dot is separated from the source and the drain by two potential barriers, and the source-drain current is due to tunneling through the discrete levels in the quantum dot. The other is the propagation regime. When the gate voltage is sufficiently higher than the threshold voltage, the Fermi level is pushed above the potential barriers that separate the quantum dot from the source and the drain. Electron waves can then propagate through the entire channel without tunneling. In this case, the quantum dot acts like a cavity in a waveguide, which will cause conductance variations due to wave interference effect.

The transistors were measured in a chamber in which the

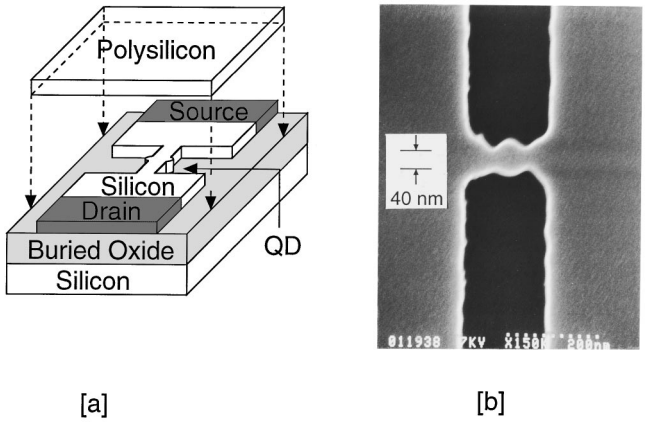

FIG. 1. (a) Schematic of a Si quantum-dot transistor where the channel having an abacus bead shape was etched into the top Si layer of a SIMOX wafer. The bead defines the quantum dot that is connected to the source and drain through two constrictions. The rectangular polySi gate covers the entire quantum dot (QD). (b) SEM micrograph of the abacus bead channel etched into the top Si layer before oxidation. The dot size and the constriction width are further reduced during the gate oxide growth at high temperature.

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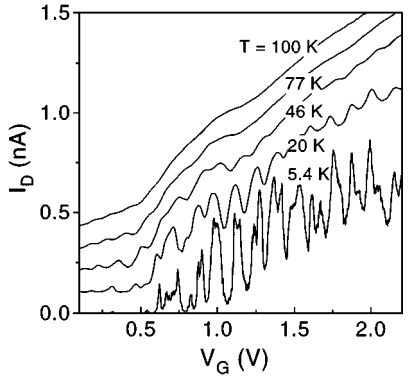

FIG. 2. The drain current I_D vs the gate voltage V_G of a Si QDT with 20 nm dot at different temperatures up to 100 K (curves are displaced for clarity). The V_{DS} was kept at 50 μV to prevent the drain bias from broadening the oscillations at 5.4 K significantly.

sample temperature can be controlled from 0.3 K up to 300 K. Figure 2 shows the drain current, I_D, of the QDT that has a 20 nm diam Si dot as a function of the gate voltage at five different temperatures from 5.4 K to 100 K. It demonstrates strong oscillations in drain current. Some oscillations have persisted even at temperatures above 100 K. In the measurement, the drain voltage (V_D), is kept at 50 μV to minimize the bias heating effect which could significantly alter the current–voltage ($I-V$) characteristics at 5.4 K. The temperature dependence study of the peak width indicates the oscillation is due to the electron tunneling through a discrete energy level in the quantum dot and gives an energy spacing between the levels of ~40 meV. It was also found that the larger the diameter of the lithographically defined Si dot, the smaller the oscillation period.

To further investigate the energy level spacing, the drain current of the transistor versus the gate voltage was measured as a function of the drain voltage at 0.5 K using a direct-current setup, as shown in Fig. 3. As the drain voltage increases, the peaks are broadened; however, they are still visible at biases over 70 mV. The energy spacing can be estimated from a three-dimensional plot, as shown in Fig. 4, where the differential conductance ($\partial I_D/\partial V_{DS}$) represented by the gray scale is plotted as function of drain bias (on x axis) and the gate voltage (on y axis). The diamond-shaped valley is a typical characteristic of the electron tunneling

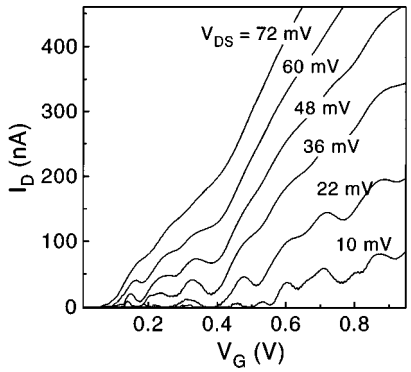

FIG. 3. The drain current I_D vs the gate voltage V_G of the same Si QDT as in Fig. 2 at 0.5 K with different source-drain voltages V_{DS} up to 72 mV.

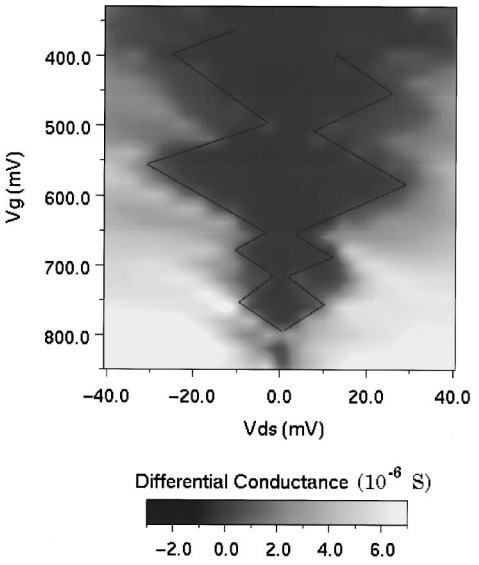

FIG. 4. The differential conductance, $\partial I_D/\partial V_{DS}$, represented by the gray scale is plotted as a function of drain bias (in x axis) and the gate voltage (in y axis). The guidelines are inserted to delineate the diamond-shaped valley current.

through the discrete levels.[5] Using Fig. 4, the maximum width of the diamond gives an energy gap of ~40 meV, agreeing with the temperature dependent measurement. Most measurement were made using HP4145B, except for low source drain biases where a low-frequency lock-in amplifier was used.

One key question in understanding the device operation is what makes the energy gap so large? If we approximate the Si dot by a sphere with hard-wall confining potential, we can estimate the quantum energy E_Q and single-electron charging energy E_C for a Si dot of 20 nm diameter. The results are $E_Q=24$ meV, $E_C=14$ meV, giving a total energy of ~38 meV, consistent with the measurements. This calculation indicates that quantum energy and single-electron charging energy are comparable in the Si QDTs; in this case both would contribute to the observed energy spacing. This interplay is also evident from the fine features in the drain current oscillations that will be discussed elsewhere. The interplay between the quantum effect and single-electron charging has been reported in the III–V compound semiconductor based QDTs,[3] but often neglected in analyzing other QDTs.[4]

We believe that the Si QDTs operation temperature and bias can be tripled by further reducing the dot size, probably by a factor of 2. At that size, the quantum effect will be the dominant effect responsible for the discrete energy levels, since the quantum energy is inversely proportional to the square of dot size while the Coulomb energy is merely inversely proportional to the dot size.

We did not force the 20 nm diameter Si dot transistor to operate in the propagating regime, because it would require a gate voltage close to the oxide breakdown voltage. Instead, we studied a QDT that has a larger dot size and wider constrictions, and therefore, a lower gate voltage needed for operating in the propagating regime. Figure 5 shows that the drain current versus the gate voltage of a Si QDT with a ~40

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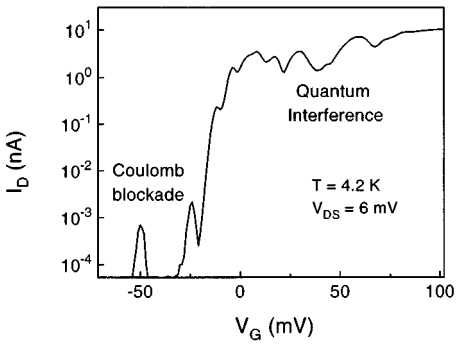

FIG. 5. Semilog plot of the current vs the gate voltage of the transistors of 40 nm dot at 4.2 K. It clearly indicates two types of the features; single-electron Coulomb blockade near the threshold voltage and interference between different modes of quantum waves in the cavity.

nm dot diameter. Clearly, there are two very different regimes. One has a very low current level but large current modulation (i.e., large ratio of ''on'' current to ''off'' current) caused by electron tunneling through the quantum dot. The other is featured by a much higher current level and smaller current modulation caused by the interference between different modes of quantum wave in a cavity. Similar quantum interference was observed in a GaAs quantum dot.[6]

It should be pointed out that, after the submission of the letter, we have achieved Si QDT operating up to a temperature of 170 K and a single hole QDT operating up to 110 K. These results will be published elsewhere.[7]

In summary, we have observed drain current oscillations in nanoscale silicon quantum-dot transistors above the 100 K. The study of the temperature dependence and the drain bias dependence indicate that the largest energy spacing in a ~20 nm diameter Si dot is about ~40 meV. Theoretical analysis shows that the large energy spacing is due to the interplay of quantum and electron charging effects. Finally, current oscillation due to the interference between different modes of quantum waves in a cavity has been observed. We believe that using our current nanolithography capability the dot size can be further reduced and this should lead to possible room-temperature operation.

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