CrossMark
click for updates

Observing the semiconducting band-gap alignment of MoS_2 layers of different atomic thicknesses using a $MoS_2/SiO_2/Si$ heterojunction tunnel diode

Katsuhiko Nishiguchi,[1,a)] Andres Castellanos-Gomez,[2,b)] Hiroshi Yamaguchi,[1] Akira Fujiwara,[1] Herre S. J. van der Zant,[2] and Gary A. Steele[2]
[1]*NTT Basic Research Laboratories, 3-1 Morinosato Wakamiya, Atsugi, Kanagawa 243-0198, Japan*
[2]*Kavli Institute of Nanoscience, Delft University of Technology, Lorentzweg 1, 2628CJ Delft, The Netherlands*

(Received 23 February 2015; accepted 12 June 2015; published online 3 August 2015)

We demonstrate a tunnel diode composed of a vertical $MoS_2/SiO_2/Si$ heterostructure. A MoS_2 flake consisting four areas of different thicknesses functions as a gate terminal of a silicon field-effect transistor. A thin gate oxide allows tunneling current to flow between the n-type MoS_2 layers and p-type Si channel. The tunneling-current characteristics show multiple negative differential resistance features, which we interpret as an indication of different conduction-band alignments of the MoS_2 layers of different thicknesses. The presented tunnel device can be also used as a hybrid-heterostructure device combining the advantages of two-dimensional materials with those of silicon transistors. © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4927529]

Downsizing of Si field-effect transistors (FETs) has allowed ever-advancing performance and integration of electrical circuits. The downsizing also provides Si with unique characteristics including band-gap opening,[1,2] energy-level quantization,[3,4] and valley splitting,[5,6] which open ways for fascinating applications, e.g., a resonant tunneling diodes,[3] a light emitting diodes,[6,7] and a tool for tunneling spectroscopy.[4] In particular, tunneling spectroscopy, which is typically done using a scanning tunneling microscopy (STM), provides not only information about energy quantization, not observable in conventional current characteristics of FETs, but also can be used to implement light emitting devices.[8] These approaches promise for "More than Moore," which expands functions of Si FETs and their circuits. However, since Si has indirect band gap and heavy electron mass, applications utilizing band-diagram engineering have limitations compared to compound semiconductors.

Two-dimensional materials, on the other hand, have recently emerged as a candidate to substitute Si in "Beyond CMOS." With direct bandgaps and lighter electron masses, two-dimensional materials have attracted much attention because of their potential for electronic and optical applications as well as physics. The research on the two-dimensional materials had been boosted by the pioneering works on graphene[9,10] and has covered other materials including transition-metal dichalcogenides MX_2 and black phosphorous.[11–13] These two-dimensional materials are composed of layers with strong in-plane bonds and with weak van der Waals force mediated interlayer interactions, making possible to exfoliate them into atomically thin layers. MoS_2, one of the layered MX_2 materials, has been studied widely for various applications such as transistors,[14,15] photo sensors,[16,17] and valleytronics and spintronics devices.[18,19] In analogy with other two-dimensional materials, the band gap of MoS_2 is modulated by the number of MoS_2 layers, showing an indirect band gap of 1.28 eV in bulk that increases while reducing the number of layers. In the single-layer limit, MoS_2 exhibits a direct band gap of 1.9 eV,[20,21] promising for light-emitting diodes.[22,23] In any applications using two-dimensional materials, the energy-band structure and the relative band alignments are crucial inputs for designing and understanding devices.

In this work, we present a tunnel diode based on a combination of an MoS_2 gate with a Si FET. Using a n-type-MoS_2/SiO_2/p-type-Si heterostructure, we observe current characteristics with multiple negative differential resistance (NDR) peaks. The appearance of the multiple NDR peaks suggests a signature of different conduction-band alignments of the different numbers of the MoS_2 layers, which is then observed in the tunneling spectroscopy in a solid-state device. The combination of Si with two-dimensional materials also promises for providing functionality taking advantage of Si FETs and two-dimensional materials.

A Si FET is fabricated from a silicon-on-insulator (SOI) wafer [Fig. 1(a)]. The SOI channel has two areas with thicknesses of 30 and 65 nm [see Figs. 1(b) and 2(a)], which are used for restricting an area through which tunnel current can flow (see detailed discussion later). The SOI channel is covered with 6-nm-thick thermal oxide. A Si substrate is used as a back gate. Since the source and drain terminals are lightly doped with boron impurities, the device functions as a pseudo FET, and negative back-gate voltage V_G makes the MOSFET characteristics p-type. In the next step, AuPd(70 nm)/Ti(10 nm) electrodes for electrical contact to an MoS_2 flake are patterned by electron-beam lithography on a buried oxide (BOX) as shown in Figs. 1(b) and 2(b). In order to transfer the MoS_2 flake precisely onto the thinner part of the SOI channel and onto the AuPd/Ti electrodes, we used an all-dry deterministic transfer technique,[24] which can place the flake with spatial precision of a few micrometers, as shown in Figure 1(a). Finally, the device is annealed in a mixture of Ar (200 sccm) and H_2 (50 sccm) at 200 °C for 2 h

[a)]E-mail: nishiguchi.katsuhiko@lab.ntt.co.jp
[b)]Present address: Instituto Madrileño de Estudios Avanzados en Nanociencia (IMDEA-Nanociencia), 28049 Madrid, Spain.

 © 2015 AIP Publishing LLC

This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 131.180.131.242 On: Tue, 18 Aug 2015 07:20:18

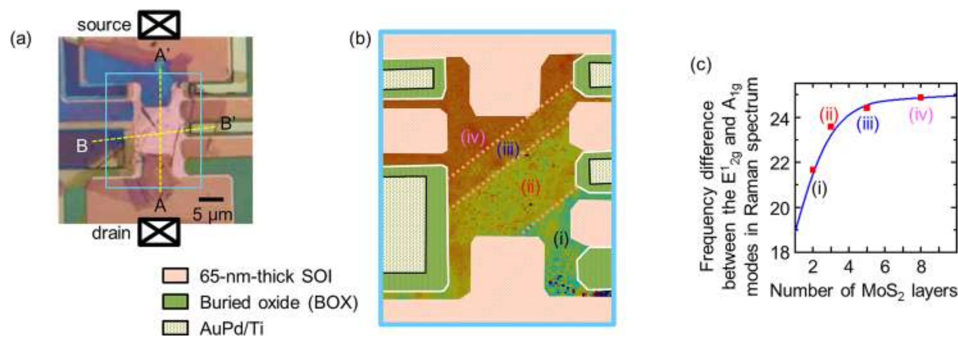

FIG. 1. (a) Photograph of a Si MOSFET, partially covered with an MoS_2 flake. The transparent and dark-contrast area depicts the MoS_2 flake. The dotted lines (A-A' and B-B') indicate linecuts for cross-sectional views shown in Figs. 2(a) and 2(c). (b) A schematic view of the area surrounded by a solid line in (a). The false-color areas depict buried oxide, AuPd/Ti electrodes, and a 65-nm-thick SOI channel. The rest of the area showing a color mapping is a 30-nm-thick SOI channel. The color mapping indicates the frequency difference between the E^1_{2g} and A_{1g} modes in a Raman spectrum. According to the number of MoS_2 layers, the area can be divided into four areas as shown by the broken lines. (c) Frequency difference between the E^1_{2g} and A_{1g} modes as a function of the number of the MoS_2 layers. The solid line shows values from Ref. 25. The wavelength of the light source is 515 nm. Roman numerals indicate areas shown in (b). Because of the small change in frequency difference at (iv), the layer number at (iv) is estimated to be 8 ± 1.

to improve the electrical contact between the MoS_2 and the AuPd electrodes. Once fabricated, Raman spectroscopy is used to determine the number of MoS_2 layers in each region of the device. A comparison of the frequency difference between the E^1_{2g} and A_{1g} modes with the results reported in Ref. 25 enables us to identify the number of MoS_2 layers as shown in Figs. 1(b) and 1(c). From the Raman measurements, we find that the MoS_2 flake is composed of four areas with different number of layers.

In Fig. 2, we present the principle of operation of the device. In order to operate the p-insulator-n tunnel heterostructure, the carrier densities and conductivities of the MoS_2 layer and the Si channel must be optimized. The conductance of both can be tuned using a global back gate formed from the doped silicon substrate of the device. Figures 2(a) and 2(b) show the gate dependence of the conductance of the silicon channel and of the MoS_2 layer, respectively. At negative gate voltages, the silicon channel is conducting, and for positive voltages in this voltage range, the silicon channel is depleted, consistent with the bulk p-doping of the channel layer. In contrast, the MoS_2 layer is conductive for positive gate voltages and becomes insulating for negative gate voltage, consistent with the background n-type doping commonly observed for MoS_2 flakes. Since the parts of the MoS_2 flakes on the top surface of the BOX are closer to the back gate than the other parts of the MoS_2 flakes on the SOI, the former MoS_2 has resistance lower that the latter, which means that measured current characteristics originate from the part of the MoS_2 flakes on the SOI channel. The relatively small on-off current ratio ($\sim$10) of the MoS_2 layer compared to other reports[14,15] is likely due to electron tunneling from the MoS_2 flake to the floating Si channel which then limits our ability to achieve high electron density induced in the flake.

Figure 2(c) shows the tunnel current through the device when operated as a heterostructure tunnel diode for different gate voltages. We experimentally confirmed that the tunnel current originates only from the active area of the device where the Si-channel is 30-nm thick by confirming that no tunnel current is observed in another device without the

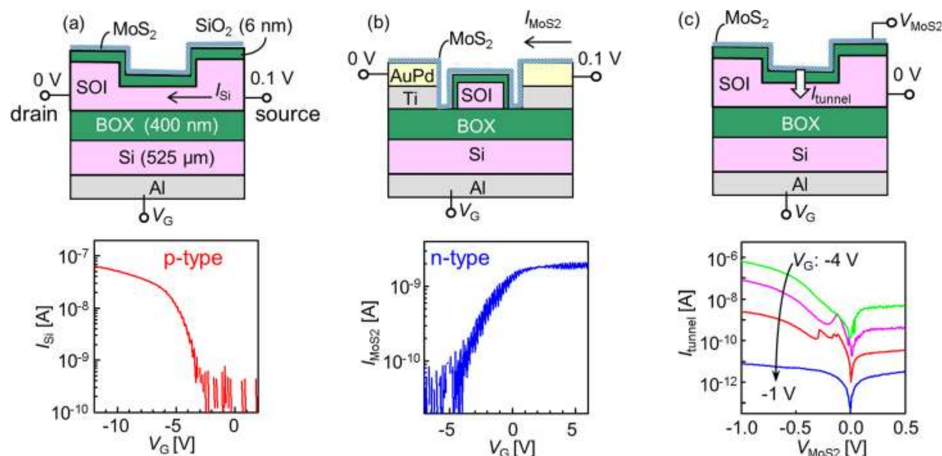

FIG. 2. (a) (Upper) A cross-sectional view along the dotted line (A-A') in Fig. 1(a). Thicknesses of the thicker and thinner SOI channels are 65 and 30 nm, respectively. (Lower) Current (I_{si}) characteristics of the SOI channel as a function of back-gate voltage (V_G). Voltages applied to the channel are shown in the upper figure. The MoS_2 flake is electrically floated, i.e., disconnected from voltage supplies, in order to prevent current from flowing between the SOI channel and MoS_2 flake. (b) (Upper) A cross-sectional view along the dotted line (B-B') in Fig. 1(a). (Lower) Current (I_{MoS2}) characteristics of the MoS_2 flake as a function of back-gate voltage (V_G). Voltages applied to the channel are shown in the upper figure. The SOI channel is electrically floated, i.e., disconnected from voltage supplies, in order to prevent current from flowing between the SOI channel and MoS_2 flake. (c) (Upper) Schematic of a tunnel diode. (Lower) Current (I_{tunnel}) characteristics as a function of MoS_2 voltage (V_{MoS2}) at various V_Gs. For illustration purposes, each curve is shifted vertically by a factor of 10.

This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 131.180.131.242 On: Tue, 18 Aug 2015 07:20:18

30-nm-thick region. This absence of tunnel current from the 65-nm-thick regions is because holes are induced at the bottom of the Si channel, and the hole wavefunction in the 65-nm-thick Si-channel regions does not extend fully to the top surface of the SOI channel facing the MoS_2. On the other hand, in the 30-nm-thick channel regions, holes are induced at both the top and bottom of the channel, which makes the whole 30-nm-thick channel conductive. From this, we conclude that the measured current originates from the tunneling between the MoS_2 flake and 30-nm-thick Si-channel [Fig. 1(b)]. The SOI channel and MoS_2 flake also act as gates for each other: carrier densities in the SOI and MoS_2 layers are modulated by the MoS_2 flake and SOI channel voltages, respectively. At $V_G = -4$ V (green trace), although the MoS_2 flake seems to be depleted as shown by Fig. 2(b), voltage (0 V) applied to the SOI channel generates electrons in MoS_2. Similarly, at $V_G = -2$ V (red trace), V_{MoS2} generates holes in the SOI channel. Since carriers are also modulated by V_G, mechanism of current characteristics is complicated, but nonetheless they are modulated clearly by V_G as shown in Fig. 2(c). At $V_G = -1$ and -4 V, since carriers are not sufficiently generated for channel inversion, current is monotonically changed by V_{MoS2}. At $V_G = -2$ V (red trace), a sufficient density of holes and electron are induced in the silicon channel and MoS_2 layer, respectively. At this gate voltage, we now also observe additional features in the tunnel current that are not present in the other two configurations.

Figure 3(a) shows a zoomed plot of the tunnel current in the region of these additional features. The data show four clear peaks in tunnel conductance occurring at different bias voltages. We interpret these four features as corresponding to the bias voltage across the p-insulator-n heterojunction aligning to conduction band edge corresponding to the four different thicknesses of MoS_2. This is illustrated schematically in Figure 3(b). At zero bias voltage, the Fermi levels of the MoS_2 layer and the Si channel are aligned. From the in-plane conductance of the device [Figs. 2(a) and 2(b)], we know that the silicon channel and MoS_2 layer have p-type and n-type characteristics, respectively. Although I_{mos2} is very small at V_G of -4 V as shown in Fig. 2(b), electrons are sufficiently induced in the MoS_2 layer by voltage (0 V) applied to the silicon channel, instead of V_G. From this, we conclude that the Fermi levels of the MoS_2 layer and the Si channel are located over the conduction band of the MoS_2 and under the valence band of the silicon, respectively, as shown in Fig. 3(b). The conductance measurements also indicate that the in-plane resistance of the silicon channel and MoS_2 layers is lower than that from the tunnel barrier SiO_2, ensuring that the voltage bias is dropped dominantly over the insulating tunnel barrier. As the bias voltage across the tunnel junction is swept, the electrons over the conduction band in the MoS_2 layer tunnel between the valence band and Fermi level of the silicon channel. As the applied bias voltage is made more negative, the valence band of the Si tunnel contact passes through the edge of the conduction band of the MoS_2 layer, giving first a peak in current characteristics, followed by a drop as the valence band of the Si channel is aligned inside the band gap of the MoS_2 layer. From this reasoning, the voltage at which the NDR peak

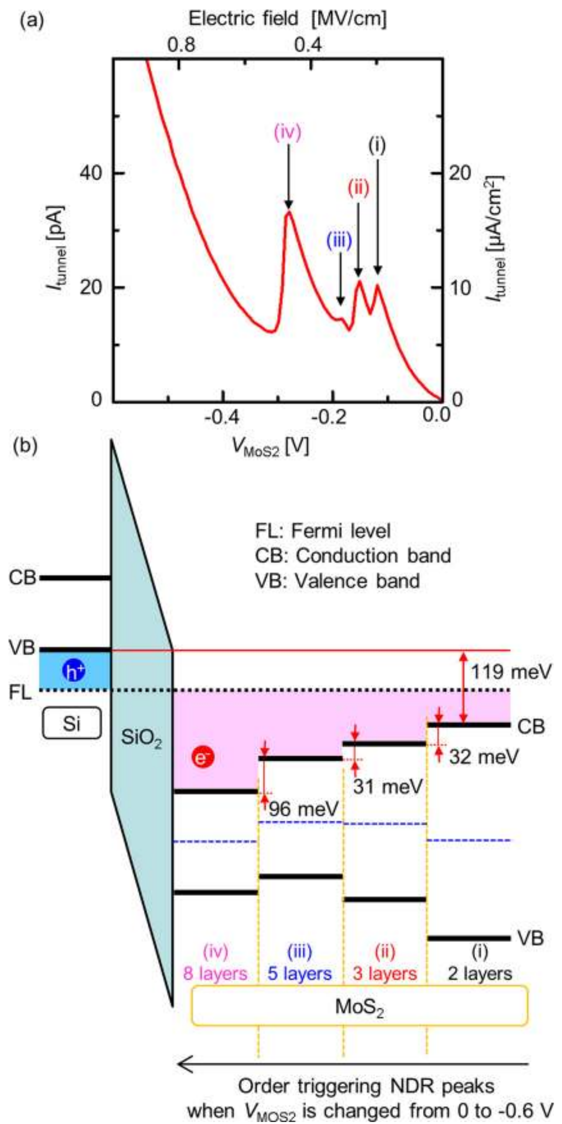

FIG. 3. (a) I_{tunnel} characteristics as a function of V_{MoS2} at V_G of -2 V. The arrows indicate negative differential conductance. (b) Energy-band diagram at V_{MoS2} of 0 V. Although all MoS_2 areas face the SiO_2 layer, the MoS_2 areas are shifted horizontally in the illustration. The horizontal arrow at the bottom shows the order in which each MoS_2 layer triggers a NDR peak when the gate is swept from 0 to -0.6 V. In the Si (MoS_2) layer, the channel is filled from the valence band (VB) (conduction band (CB)) to the Fermi level (FL) with holes (electrons). From optical measurements,[21] band gaps of 2, 3, and 5 MoS_2 layers are assigned as 1.62, 1.47, and 1.39 eV, respectively. A band gap of 8 MoS_2 layers is expected to be around 1.34 eV from Ref. 21. The broken lines in the band gaps depict centers of the gaps. In (a) and (b), the Roman numerals indicate areas shown in Fig. 1(b).

occurs is a measure of the energy difference between the conduction band of the MoS_2 and the valence band of the silicon channel. The height of the NDR peaks depends on tunnel resistance of 6-nm-thick SiO_2 and a surface area of the MoS_2 contacting the silicon channel. This mechanism for such NDR peaks feature is the same as a conventional tunnel diode,[26] except for existence of the tunnel barrier in our device instead of a depletion region.

As already noted, the data show four clear NDR features. In contrast to the single NDR observed in a conventional tunnel diode, the origin of four peaks here lies in the fact that tunneling from the Si channel is probing four areas of MoS_2 of different thicknesses. It is well-established that

This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 131.180.131.242 On: Tue, 18 Aug 2015 07:20:18

MoS_2 undergoes significant changes in its electronic band gap as a function of layer thickness. Although other experimental and theoretical studies to date have focused on changes in band gap, it is likely that these changes in band gap alignment itself also change as the number of layers is changed. In the context of the tunneling experiment in Fig. 3(a), this would result in four distinct NDR features: they appear one by one as the top of the valence band of the Si channel aligns with the bottom of the conduction bands of MoS_2 layers of different thicknesses. Using this, we can extract the relative band alignment of MoS_2 layers of different thicknesses from the position of the peaks in bias voltage. Figure 3(b) shows a summary of the alignments obtained in our experiment, combined with bandgap measurements from optical measurements.[21] We find that there are band offsets in conduction bands among four MoS_2 areas and that valence bands and centers of the bad gaps are also misaligned. These misalignments can be extracted by a combination of optical measurements from the literature with the tunneling spectroscopy presented here. We also note that since the NDR peaks occur at positions corresponding to when the bottom of the MoS_2 conduction band crosses the top of the Si valance band, the NDR peak position is also independent of the doping level of both the Si and MoS_2 channels, so long as they are all sufficiently highly doped that the in-plane resistances are all lower than the tunnel barrier resistance. We also note that our measurements imply that the regions of different MoS_2 thicknesses have different doping levels due to the different contact potential between each and the Si channel below.

Similar tunneling devices can be formed using only two-dimensional materials,[27–29] allowing to make a tunneling layers only few-atoms thick and thus to increase tunneling current. However, a tunnel device based on an FET advantages from fabrication techniques compatible with well-established ones for microelectronics. Particularly, since both n-type and p-type channels can be easily formed by changing V_G in a pseudo FET as our experiments or by using doped Si wafers, a p/insulator/n heterojunction can be easily constructed for any two-dimensional materials regardless n-type and p-type. Additionally, while analysis using photoluminescence is sensitive to a direct/indirect band gap and gap size because of limited light source and/or detection, our tunnel diode can provide information of the band structure for two-dimensional semiconducting materials regardless the gap size and direct/indirect nature of the gap. Although an STM is also a powerful tool to analyze an energy band structure,[30] our tunneling device needs no vacuum condition unlike the STM. Measurements at very low temperature[4,8] and high magnetic field are also easier in our device with respect to optical spectroscopy techniques and the STM. More interestingly, the p/insulator/n heterojunction allows electron or hole injection from Si to the two-dimensional materials, and photoemission from the two-dimensional materials having a direct band gap will be possible using a Si-based device although Si itself does not emit photon, which means that such hybrid of Si and two-dimensional materials expands their functionalities.

In summary, we demonstrated a tunnel diode composed of a single and few-layer MoS_2 flake and a Si FET. Vertical tunneling in the heterostructure displays a series of NDR peaks. We attribute to the onset of tunneling into MoS_2 areas composed of different thicknesses and extract a measure of the relative band alignment in MoS_2 as a function of the number of atomic layers. The results provide information into the band structure of MoS_2 that is not accessible with optical techniques and demonstrate a unique electrical tool for the analysis of energy-band structures of two-dimensional materials.

The authors thank J. Noborisaka of NTT and M. Buscema of Delft University of Technology for support in experiments and discussions.

[1] Y. Omura, S. Horiguchi, M. Tabe, and K. Kishi, IEEE Electron Device Lett. **14**, 569 (1993).
[2] H. Majima, Y. Saito, and T. Hiramoto, Tech. Dig. - Int. Electron Devices Meet. **2001**, 733.
[3] A. Zaslavsky, C. Aydin, S. Luryi, S. Cristoloveanu, D. Mariolle, D. Fraboulet, and S. Deleonibus, Appl. Phys. Lett. **83**, 1653 (2003).
[4] J. Noborisaka, K. Nishiguchi, H. Kageshima, Y. Ono, and A. Fujiwara, Appl. Phys. Lett. **96**, 112102 (2010).
[5] K. Takashina, Y. Ono, A. Fujiwara, Y. Takahashi, and Y. Hirayama, Phys. Rev. Lett. **96**, 236801 (2006).
[6] J. Noborisaka, K. Nishiguchi, and A. Fujiwara, Sci. Rep. **4**, 6950 (2014).
[7] S. Saito, D. Hahimoto, H. Shimizu, H. Hmamura, R. Tsuchiya, Y. Matsui, T. Mine, T. Arai, N. Sugii, K. Torii, S. Kimura, and T. Onai, Jpn. J. Appl. Phys., Part 2 **45**, L679 (2006).
[8] J. Noborisaka, K. Nishiguchi, Y. Ono, H. Kageshima, and A. Fujiwara, Appl. Phys. Lett. **98**, 033503 (2011).
[9] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, M. I. Katsneison, I. V. Grigorieva, S. V. Dubonos, and A. A. Firsov, Nature **438**, 197 (2005).
[10] Y. Zhang, Y.-W. Tan, H. L. Stormer, and P. Kim, Nature **438**, 201 (2005).
[11] A. Kuc, N. Zibouche, and T. Heine, Phys. Rev. B **83**, 245213 (2011).
[12] Q. H. Wang, K. Kalantar-Zadeh, A. Kis, J. N. Coleman, and M. S. Strano, Nat. Nanotechnol. **7**, 699 (2012).
[13] L. Li, G. J. Ye, Q. Ge, X. Ou, H. Wu, D. Feng, X. H. Chen, and Y. Zhang, Nat. Nanotechnol. **9**, 372 (2014).
[14] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, Nat. Nanotechnol. **6**, 147 (2011).
[15] Y. Yoon, K. Ganapathi, and S. Salahuddin, Nano Lett. **11**, 3768 (2011).
[16] Z. Yin, H. Li, H. Li, L. Jiang, Y. Shi, Y. Sun, G. Lu, Q. Zhang, X. Chen, and H. Zhang, ACS Nano **6**, 74 (2012).
[17] H. S. Lee, S.-W. Min, Y.-G. Chang, M. K. Park, T. Nam, H. Kim, J. H. Kim, S. Ryu, and S. Im, Nano Lett. **12**, 3695 (2012).
[18] D. Xiao, G. B. Liu, W. Feng, X. Xu, and W. Yao, Phys. Rev. Lett. **108**, 196802 (2012).
[19] K. F. Mak, K. He, J. Shan, and T. F. Heinz, Nat. Nanotechnol. **7**, 494 (2012).
[20] A. Splendiani, L. Sun, Y. Zhang, T. Li, J. Kim, C. Y. Chim, G. Galli, and F. Wang, Nano Lett. **10**, 1271 (2010).
[21] K. Mak, C. Lee, J. Hone, J. Shan, and T. F. Heinz, Phys. Rev. Lett. **105**, 136805 (2010).
[22] R. S. Sundaram, M. Engel, A. Lombardo, R. Krupke, A. C. Ferrari, Ph. Avouris, and M. Steiner, Nano Lett. **13**, 1416 (2013).
[23] Y. Ye, Z. Ye, M. Gharghi, H. Zhu, M. Zhao, Y. Wang, X. Yin, and X. Zhang, Appl. Phys. Lett. **104**, 193508 (2014).
[24] A. Castellanos-Gomez, M. Buscema, R. Molenaar, L. Jansen, H. S. J. van der Zant, and G. A. Steele, 2D Mater. **1**, 011002 (2014).
[25] C. Lee, H. Yan, L. E. Brus, T. F. Heinz, J. Hone, and S. Ryu, ACS Nano **4**, 2695 (2010).
[26] L. Esaki, Phys. Rev. **109**, 603 (1958).
[27] W. J. Yu, Y. Liu, H. Zhou, A. Yin, Z. Li, Y. Huang, and X. Duan, Nat. Nanotechnol. **8**, 952 (2013).
[28] K. Roy, M. Padmanabhan, S. Goswami, T. P. Sai, G. Ramalingam, S. Raghavan, and A. Ghosh, Nat. Nanotechnol. **8**, 826 (2013).
[29] W. Zhang, C. P. Chuu, J. K. Huang, C. H. Chen, M. L. Tsai, Y. H. Chang, C. T. Liang, Y. Z. Chen, Y. L. Chueh, J. H. He, M. Y. Chou, and L. J. Li, Sci. Rep. **4**, 3826 (2014).
[30] C. Zhang, A. Johnson, C. L. Hsu, L. J. Li, and C. K. Shih, Nano Lett. **14**, 2443 (2014).

This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 131.180.131.242 On: Tue, 18 Aug 2015 07:20:18