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Odd/Even Order Sampling Soft-Core Architecture Towards Mixed Signals Fourth Industrial Revolution (4IR) Applications

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Abstract: Digitization is at the center of fourth industrial revolution (4IR) with previously analog systems being digitized through an analog-to-digital converter. In addition, 4IR applications such as fifth generation (5G) Cellular Networks Technology and Cognitive Electronic Warfare (EW) at some point interface digitally through an analog-to-digital converter. Efficient use of digital resources such as memory, largely depends on the signal sampling design of analog-to-digital converters. Existing even order sampling has been found to perform better than traditional sampling techniques. Research on the efficiency of a digital interface with a 4IR platform is still in its infancy. This paper presents a performance study of three sampling techniques: the proposed new and novel odd/even order sampling architecture, existing Mod-Δ, and traditional 1st order delta-sigma, to address this. Step-size signal-to-noise (SNR), dynamic range, and sampling frequency are also studied. It was found that the proposed new and novel odd/even order sampling achieved an SNR performance of 6 dB in comparison to 18 dB for Mod-Δ. Sampling frequency findings indicated that the proposed new and novel odd/even order sampling achieved a sampling frequency of 2 kHz in comparison to 8 kHz from a traditional 1st order sigma-delta. Dynamic range findings indicated that the proposed odd/even order sampling has achieved a dynamic range of 1.088 volts/ms in comparison to 1.185 volts/ms from a traditional 1st order sigma-delta. Findings have indicated that the proposed odd/even order sampling has superior SNR and sampling frequency performances, while the dynamic range is reduced by 8%.

Keywords: soft-core architecture; odd order sampling; even order sampling; analog to digital converter (ADC)

1. Introduction

1.1. Background

Analog-to-digital converters are the heart of digitization and they are the main requirement in 4IR applications. Odd/even order sampling was studied, using step-size signal-noise-ratio (SNR), dynamic range, and sampling frequency as performance parameters. Even order sampling has been applied to multiple signal sampling while achieving an SNR of 64 decibels relative to full scale(dBFS) [1]. With the increasing need for digitization over the years, other ordered sampling techniques for multiple signal sampling have been introduced [2]. In an attempt to maintain received signal power, complexities in dynamic range resolution in relation to quantization and phase errors were studied [3]. A methodology to address complexities in dynamic range resolution was developed, which used experimental measurements of mean square error (MSE) on different quantization resolutions to analyze bit stream performance. The results produced indicated that 1-bit quantization resolution has the worst phase

MSE performance. To optimize the digital resolution of analog-to-digital converter, a quantization encoder architecture was designed [4]. A sample and hold circuit was studied in an attempt to improve memory performance by extending the input signal dynamic range [5]. In a similar study, high input voltages tolerance was investigated on an NI Multisim simulation platform [6].

1.2. Literature Review

Advances in solutions that address digital formation have led to the development of complementary metal-oxide-semiconductor (CMOS) technology sampling prototypes [7–12]. Emerging attempts to address optimization of dynamic range resolution have led to the development of a modulo analog-to-digital converter [13]. A traditional delta-sigma sampling technique has been modified in an attempt to reduce signal crosstalk in multi-channel digital converters [14]. Its application in Synthetic Aperture Radar (SAR) has led to the development of high-performance digital to analog converter (DAC) approximated analog-to-digital converter architecture, which allows for a switch between positive and negative quantization [15,16]. An analog-to-digital converter with a high effective number of bits was presented with an effective resolution of 6.8 bits. The analog-to-digital converter architecture has an M comparator array, N bits of majority elements quantizer and a low bit encoder [17]. This architecture was implemented using 90 nm CMOS technology as an 8-bit Flash analog-to-digital converter(ADC) [17]. A separate study on capacitive analog-to-digital converters takes a different point of view when addressing the issue of increasing the dynamic range. This study takes advantage of the charging behavior of a capacitor to develop a sample and hold circuit design [18,19]. A multi-stage noise shaping switching capacitor delta-sigma analog-to-digital converter was designed, while signal-to-noise ratio (SNR) and dynamic range (DR) investigations were conducted [20]. Even a sampling architecture time-to-digital converter for applications in high energy physics and a time-to-digital converter were implemented on an field programmable gate array(FPGA) platform [21]. In related fields such as control systems, the analog-to-digital stage is very important in maintaining a high-quality control feedback signal [22]. In other related fields such as interferometric aperture, synthesized passive millimeter wave high resolution images can be produced using a 1-Bit/2-level comparator quantizer [23].

Cutting-edge research and development efforts towards the design of analog-to-digital are starting to move towards the use of machine learning methodologies such as neural networks. A study to develop a non-linear 16-bit quantizer with a 3 stage neural network was conducted on Simulink. Experimental results indicated a good performance for signals with low dynamic range and an average performance for signals with a high dynamic range [24,25]. A similar study to develop an under-sampling/over-sampling quantizer using a deep learning activation function was conducted [26]. In the digital fabrication industry, Xilinx has invested a decade of research and development working towards a fully programmable heterogeneous computing platform with Scalar and Vector processing units optimized for Artificial Intelligence (AI) plus Digital Signal Processing (DSP) [27].

1.3. Contributions and Paper Organization

This paper contributes to the body of knowledge of digital signal processing in a niche of Electronic Warfare mixed signal processing through the following contributions:

- An introduction of a mathematical model for odd/even order sampling with memory considerations
- A simulation performance investigation of novel odd/even order sampling
- An experimental setup with laboratory equipment to investigate sampling frequency and memory performance
- A field programmable gate array (FPGA) application experimental setup to investigate the performance of odd/even order sampling when compared to other sampling schemes.

This paper is arranged as follows:

Section 2 presents the materials and methods used in developing this study. Section 3 dives straight into the investigation results. The material presented in this section includes but is not limited to model derivation, a laboratory experimental setup including results, and an FPGA experimental setup includes results. Section 4 gives a discussion of any deviations that these results presented.

2. Materials and Methods

Materials used in this study include:

- Laboratory equipment, Excel, a simulation tool and FPGA implementation.
- Laboratory equipment such as an oscilloscope, spectrum analyzer, Radar signal synthesizer, and Excel were used during preliminary efforts to develop research assumptions for a feasible study. A four channel Tektronix oscilloscope with a maximum resolution of 10 million sampling points and a maximum operating frequency of 1 GHz was used to capture a sample for preliminary processing with Excel. A Tektronix spectrum analyzer with a maximum operating frequency of 26 GHz was used to evaluate a quadrature signal in time and frequency domains. An Anritsu signal generator with a maximum operating frequency of 20 GHz was used to generate a Radar signal. A simulation was conducted on Matlab Simulink and the delta-sigma model in reference [14] was used and modified to cater for an odd/even order sampling architecture. An ADL5380-EVALZ-ND I/Q demodulator was used as a quadrature demodulator. Xilinx Vivado was used for a FPGA firmware design, with MiniZed being the FPGA of choice.

Other relevant factors include:

- High level research assumptions were that odd/even order sampling would reduce the total sample number and signal frequency without affecting the dynamic range.
- An I/Q sine signal was designed on the Anritsu signal generator and was supplied as input to an I/Q demodulator.
- Outputs of the I/Q demodulator were connected to two channels of the oscilloscope.
- The two channels of the oscilloscope were captured and the signal was stored as comma-separated values (CSV) files for further analysis on Excel. Results were plotted using Excel figures.

Methods developed include:

- A derived mathematical model used to process the CSV captured sine signal from the oscilloscope.
- A simulation on Matlab Simulink was used investigate the performance of step size while evaluating the effect on dynamic range.
- A 1st order delta-sigma model was used in all simulation investigations and all results were plotted using Matlab figures.
- Four sampling schemes were implemented on Xilinx Vivado, one being the proposed novel odd/even order sampling scheme and the others were from the literature.
- Performance of these schemes were captured and exported to CSV using Integrated Logic Analyzer(ILA) from Vivado.
- CSV were further processed for SNR and results were plotted using Excel figures.

3. Results

3.1. Derivation of Odd/Even Order Sampling I/Q Demodulator

3.1.1. I/Q Demodulator

The design of soft-core architecture depends largely on the I/Q demodulator and the Analog to Digital Converter (ADC). Traditionally, the design of I/Q demodulator ADC interface for Radar and Electronic Warfare (REW) applications follows five different options as depicted in reference [1].

This modification to an even order sampling equation was initiated by declaring the complex signal components I and Q, as shown in Equations (1)–(3) below.

$$s(t) = a_m(t) * (w_{IF} * t + \varphi_M(t)), s(t) = I(t) * \cos(w_{IF} * t) - Q(t) * sin(w_{IF} * t) \quad (1)$$

$$I_{raw}(t) = a_M(t) * \cos(\varphi_M(t)), \quad (2)$$

$$Q_{raw}(t) = a_M(t) * \sin(\varphi_M(t)), \quad (3)$$

The modulator produces a signal governed by Equation (1) and Table 1, while the demodulator produces signals governed by Equations (2), (3) and Table 2. The current form of the equations does not consider the behavior of the sampling circuit.

Table 1. Variable description for Equation (1).

Variable	Description
$s(t)$	Complex signal
$I(t)$	Inphase component
$Q(t)$	Quadrature component
W_{IF}	Intermediate Freq

Table 2. Variable description for Equations (2) and (3).

Variable	Description
$I_{raw}(t)$	Demodulated I component
$Q_{raw}(t)$	Demodulated Q component
$a_m(t)$	Demodulated amplitude
$\varphi_m(t)$	Demodulated phase

3.1.2. Odd Order Sampling

The final form of the I/Q digital mixer was obtained by applying a finite impulse response(FIR) filter to the digital firmware mixer. It should be noted that reference [2] implements a 4th order FIR as compared to reference [1], which implements a 7th order FIR. Table 3 elaborates the switching pattern of the mixer. Parameters for Equations (4) to (7) are defined in Table 4.

$$I_{odd} = \cos(W_{IF} * (T_1 + \Delta)) * C_1 - \cos(W_{IF} * (T_3 + \Delta) + \varphi_{IF}) * C_3 \quad (4)$$

$$Q_{even} = -\sin(W_{IF} * (T_2 + \Delta) + \varphi_{IF}) * C_3 + \sin(W_{IF} * (T_4 + \Delta) + \varphi_{IF}) * C_1 \quad (5)$$

The Odd order I/Q demodulator presented in reference [2] does not clearly derive the odd 3rd order sampling characterization equation that it presents. Equations (6) and (7) in this paper initiate the derivation for the proposed odd/even order sampling algorithm:

$$I = u_1 - 3u_3 where u_1 = \cos(W_{IF} * (T_1 + \Delta) + \varphi_{IF})) * C_1 \textit{ is the ADC samples}, \quad (6)$$

$$Q = -(3u_2 - u_4) where u_2 = \cos(W_{IF} * (T_2 + \Delta) + \varphi_{IF})) * C_3 \textit{ is the ADC samples}. \quad (7)$$

Table 3. I/Q demodulator odd 4th order digital mixing [2].

Sample No: (n)	0	1	2	3	4
I-coefficients	0	1	0	−1	0
Q-coefficients [1]	0	0	−1	0	1

[1] Q coefficients is phase lag (n−1).

Table 4. Variable description for Equations (4) and (5).

Variable	Description
$I_{odd}(t)$	Odd sampled I component
$Q_{even}(t)$	Even sampled Q component
$T_{1,3}(t)$	Odd sampling time
$C_{1,3}$	FIR coefficients
$T_{2,4}(t)$	Even sampling time
Δ	Quantization error

3.1.3. Even Order Sampling

In the previous section, the idea of odd order was induced and preliminary derivation of equations was initiated. The final form of the derived equations includes the FIR 4th order filtering presented in Table 5. This section will restate work in reference [1] as an initialization step towards the derivation of an odd/even 7th order sampling scheme.

$$I_{even} = \cos(W_{IF} * (T_0 + \Delta)) * C_1 - \cos(W_{IF} * (T_2 + \Delta) + \varphi_{IF}) * C_{11} + \cos(W_{IF} * (T_4 + \Delta) + \varphi_{IF}) * C_{15} - \cos(W_{IF} * (T_6 + \Delta) + \varphi_{IF}) * C_5 \quad (8)$$

$$Q_{odd} = \sin(W_{IF} * (T_1 + \Delta) + \varphi_{IF}) * C_5 - \sin(W_{IF} * (T_3 + \Delta) + \varphi_{IF}) * C_{15} + \sin(W_{IF} * (T_5 + \Delta) + \varphi_{IF}) * C_{11} - \sin(W_{IF} * (T_7 + \Delta) + \varphi_{IF}) * C_1 \quad (9)$$

Before we dive down to the derivation of odd/even order sampling, we need to develop digital sampling for filtered even 7th order sampling, as shown in Table 6 below. After a 7th order filter has been applied Table 7 is produced with unit numbers replaced with filter coefficients.

Table 5. A 4th order FIR filtering I/Q demodulator odd order digital mixing pattern [2].

Sample No: (n)	0	1	2	3	4
I-coefficients	0	1	0	−3	0
Q-coefficients [1]	0	0	−3	0	1

[1] Q coefficients is phase lag (n−1), FIR filter introduces coefficient −3.

Table 6. I/Q demodulator for even 7th order digital mixing [1].

Sample No: (n)	0	1	2	3	4	5	6	7
I-coefficients	1	0	−1	0	1	0	−1	0
Q-coefficients [1]	0	1	0	−1	0	1	0	−1

[1] Q coefficients is phase lag (n−1).

Table 7. I/Q demodulator for odd 7th order digital mixing [1].

Sample No: (n)	0	1	2	3	4	5	6	7
I-coefficients	1	0	−11	0	15	0	−5	0
Q-coefficients [1]	0	5	0	−15	0	11	0	−1

[1] Q coefficients is phase lag (n−1).

3.1.4. Odd/Even Order Sampling

The proposed odd/even order sampling algorithm excludes the FIR filtering stage, filter phase Δ, and filter coefficients, leading C_n in Equations (4) to (7) fall away. We introduce analog-to-digital converter tuning signal controlled by random access memory strobe. When the following modifications are applied to Equations (4) and (5), the new equation become Equations (10) and (11).

$$I_{odd} = \{(odd\_even\_adc\_sampling = 1) \\ |\{\cos(W_{IF} * T_1 + \varphi_{IF}) - \cos(W_{IF} * T_3 + \varphi_{IF}) + \cos(W_{IF} * T_5 + \varphi_{IF}) - \cos(W_{IF} * T_7 + \varphi_{IF})\}\} \quad (10)$$

$$I_{odd} = \{(odd\_even\_adc\_sampling = 1) \\ |\{\cos(W_{IF} * T_1 + \varphi_{IF}) - \cos(W_{IF} * T_3 + \varphi_{IF}) + \cos(W_{IF} * T_5 + \varphi_{IF}) - \cos(W_{IF} * T_7 + \varphi_{IF})\}\} \quad (11)$$

We assumed that a sampling window N is selected in such a way that 8-bit addressing is achieved to realize the memory mapping proposed in Table 8. A 2-bit strobe allows for a controlled switch forth and back between an odd order and an even order, while memory located at 0x104 in the reserved memory band is the address that stores the 2-bit control strobe. The ten address locations between address 0xFF and 0x109 are reserved from storage functions. This memory band is used to accommodate the strobe while guarding for data leaks. Memory allocation of address 0x104 is 1 byte, with the first two bits in the lower nibble with write functionality for the strobe are shown in Table 9. The last two bits in the higher nibble with read functionality for the strobe as shown in Table 9.

Table 8. Odd/even order sampling proposed memory mapping.

Input Addr	Dual-Port Mem	Output Addr
0x00	I (0)	0x00
...	...	...
0xFF	I (i)	0xFF
Reserved to guard data leak + 2-bit strobe		
0x109	Q (0)	0x109
...	...	...
0x208	Q (i)	0x208

Table 9. Bit arrangement at memory located 0x104.

Bit No	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
Bit Function	**Strobe**		Reserved	Reserved	Reserved	Reserved	**Flag**	

Equations (6)–(9) are the foundation for derivation of the final form of the proposed odd order sampling with memory considerations. The full form of the proposed odd order sampling is given by Equation (13). The full form in Equation (12) selects odd sampling by using the strobe 8-bit register *s* shown in Tables 9 and 10 which is wired to control the signal that drives the analog-to-digital converter. This operation is also true for even order sampling in Equation (13).

$$dRM_{wr_s}^{rd^s} = \sum_{s_i=0}^{N}\{\{(wr_s = 1\ And\ s = 00)?|\{\{(S_i\ Mod\ 2 = 1)?|\sum_{i_s=0}^{255} I_{odd}(S_i)\}|\{(S_i\ Mod\ 2 = 1)?|\sum_{i_s=269}^{525} Q_{even}(S_i)\}\} \quad (12)$$

$$dRM_{wr_s}^{rd^s} = \sum_{s_i=0}^{N}\{\{(wr_s = 1\ And\ s = 01)?|\{\{(S_i\ Mod\ 2 = 0)?|\sum_{i_s=3}^{255} I_{even}(S_i)\}|\{(S_i\ Mod\ 2 = 1)?|\sum_{i_s=269}^{525} Q_{odd}(S_i)\}\} \quad (13)$$

Table 10. Variable descriptions for Equations (12) and (13).

Variable	Description
dRM	Dual-port memory
wr_s	Memory write
rd^s	Memory read
S_i	Sample number
s	Memory strobe

3.2. Simulation Towards Investigation of Odd/even Order Sampling Step Size

In a previous section, a mathematical model for odd/even order analog-to-digital converter with internal tuning of sampling was established in such a way that a selection between odd and even can be achieved in a soft-core system. In this section, a simulation model that aims to investigate step size performance between the proposed sampling scheme and 1st order sigma-delta sampling is presented.

3.2.1. General Phase Performance

A Delta-sigma model consists of a negative feedback loop (delta part of the design), first order integrator (summation part of the design), 1-bit quantization (first stage for digital formation), zero-order-hold (second stage for digital formation), and multistage digital filtering to reduce the step size (digital filtering as the third and final stage). Simulation results for delta-sigma sampling are shown in Figure 1 with quantization step size clearly defined, especially for odd order sampling (red) and even order sampling (black).

Simulation results for delta-sigma sampling are shown in Figures 1 and 2, with the quantization step size clearly defined. Quantization step size measurement attributes for the same delta-sigma sampling are given in Table 11. These are compared to odd/even order sampling results in Table 12, which indicate that the sampling frequency is reduced from 8 kHz in delta-sigma to 2 kHz in the new odd/even order sampling. The advantage of reducing the sampling frequency to 2 kHz is a simple architectural design and reduced resource utilization. Reduced resource utilization results in a cheaper FPGA choice.

Table 11. The 1st order delta-sigma simulation measurements results.

Quantization Step Parameter	Simulation Measurement
ΔT	124.687 us
ΔY	0.1477 volts
ΔF	8.020 kHz
ΔY/ΔT	1.185 (Volts/ms)

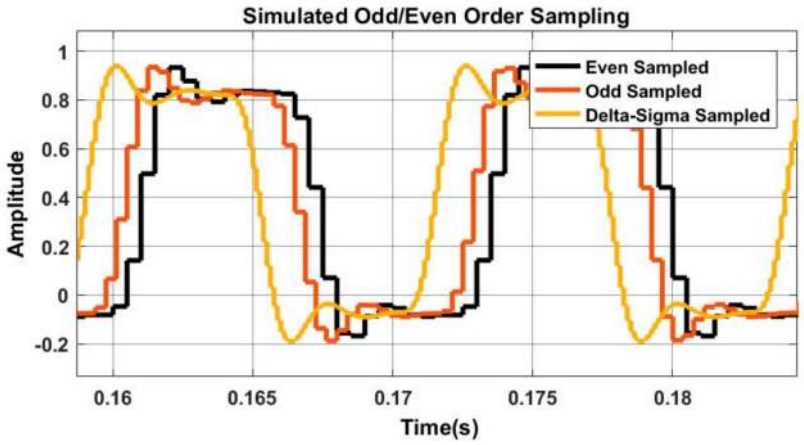

Figure 1. This portrays the phase performance between 1st order delta-sigma and odd/even order sampling. The phase difference between 1st order delta-sigma and odd/even sampling was created for the design by the transport delay between the signals, and should be ignored for analysis. 1st delta-sigma is indicated by the yellow, odd order sampling by red and even order sampling by black. It should be noted there is a (n−1) phase lag between even order sampling (black) and odd order sampling (red).

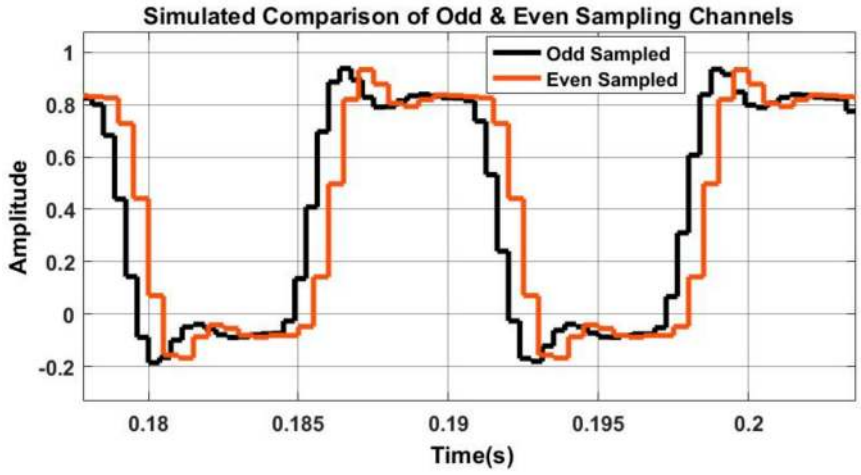

Figure 2. This portrays the phase lag performance between odd and even order sampling. Odd order sampling is marked by black and even order sampling is marked by red. It should be noted that the (n−1) phase lag between even order sampling (red) and odd order sampling (black) varies per period interval.

Table 12. Odd/even order simulation measurements results.

Quantization Step Parameter	Simulation Measurement
ΔT	378.747 us
ΔY	0.4120 volts
ΔF	2.640 kHz
ΔY/ΔT	1.088 (Volts/ms)

3.2.2. Step Size, Dynamic Range, and Mean Square Error Performance

During the simulation investigation, we were also interested in the mean square error (MSE) performance of the new odd/even order sampling. MSE performance results indicate that the proposed sampling scheme has a high MSE as compared delta-sigma sampling. This is because of an increased step size during the odd/even order sampling process. MSE behavior results is shown in Figure 3 below, with 4th even order sampling showing worse behavior compared to 1st odd order sampling.

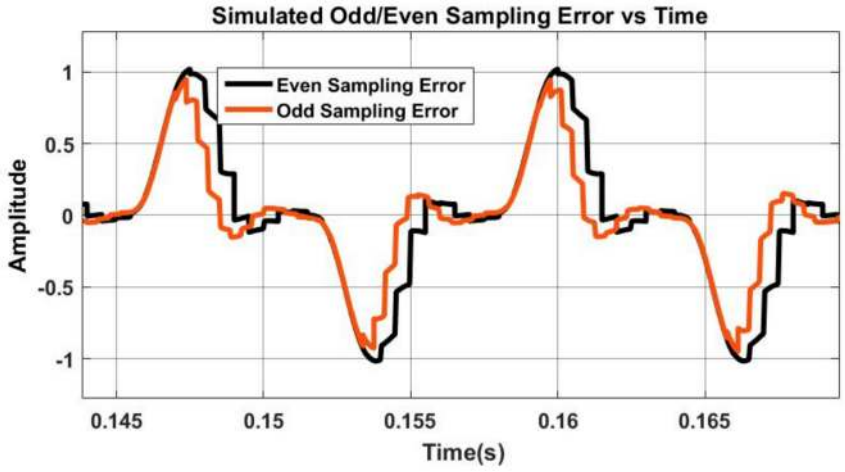

Figure 3. This portrays the phase lag performance between odd and even order sampling. Odd order sampling was marked by black and even order sampling was by red. It should be noted that the (n−1) phase lag between even order sampling (red) and odd order sampling (black) varies per period interval.

3.3. Liborarory Investigation Towards Verification of High Level Research Assupmsions

The high level research initial assumptions were that odd/even order sampling will reduce sampling of the frequency of I/Q signals while maintaining efficient memory usage. The combination of an experimental setup and results would initiate signal data collection, while Excel implementation of the new odd/even order sampling on collected data would provide results for further interpretation.

3.3.1. Experimental I/Q Signal Design

This experimental setup is centered around generation of I/Q demodulator signals as system under investigation. The experimental equipment available to conduct this experiment are presented in Table 13.

Table 13. Measurement equipment available for the experimental setup.

Experimental Equipment	Equipment Range
Anritsu Signal Generator	1 Hz to 20 GHz
Tektronix Oscilloscope	1 Hz to 1 GHz
Tektronix Spectral Analyzer	1 Hz to 26 GHz

Flexible waveguides were selected for interconnection between the signal source, system under investigation, and measurement equipment. Procured I/Q demodulator with dual p and n channels was used throughout the measurement efforts. It is important to emphasize that the procured I/Q demodulator was supplied without an n channel connected on the printed circuit board (PCB). An I/Q demodulator connection schedule was given in Table 14.

Table 14. ADL5380-EVALZ-ND I/Q Demodulator Electrical Connection Schedule.

Connector Schedule	Electrical Schedule
RF_p	SMA to Waveguide from Signal Gen
RF_n	No SMA connector PCB terminated
I_p	SMA to Waveguide to Oscilloscope
I_n	No SMA connector PCB terminated
Q_p	SMA to Waveguide to Oscilloscope
Q_n	No SMA connector PCB terminated
V_cc	Croc Clips to Power Supply
Ground	**Croc Clips to Power Supply**

A proposed experimental setup to investigate research assumptions for the new odd/even order sampling of I/Q signals was conducted in a laboratory environment. The experiment setup to acquire I/Q signals consisted of a Tektronix Oscilloscope with an integrated spectral analyzer and a 12-bit analog-to-digital converter, a 5 GHz local oscillator (LO) driven by a voltage-controlled oscillator (VCO), which can be configured to generate 1 Hz to 5 GHz, and an Anritsu Signal Generator. The Anritsu signal generator was used as the signal source with 5 Ω characteristic load and maximum signal power design to 0.0 dBm. The source was configured to produce a phase modulated complex signal with I and Q separated by a constant phase shift. To verify the design of the complex, a Tektronix spectral analyzer was used in complex function. Other analyses such as a spectrogram to confirm the percentage pulse overlap between I and Q was also conducted, and an overlap of 19% was verified as shown in Table 15.

Mod-Δ sampling was implemented under an Intelligent Processing sub block, along with other components of architectural design in Figure 8 and Table 15. The mathematical model equations of the new odd/even order sampling were replaced by that of Mod-Δ sampling. The modification is also evident with resource utilization in Table 16 registering a DSP usage of just over 30% and with total resource utilization at just above 75%.

Table 15. Spectrogram measurements results.

Measurements		Settings	
Δ Overlap	**Freq**	**Time/Div**	**Span**
19%	1.004649 GHz	450 us	24.40 MHz

Table 16. High-end wave front frequency spectrum measurements results.

Measurements		Settings	
Amplitude	**Freq**	**Time/Div**	**Span**
−72.56 dBm	1.004649 GHz	10 dB	24.40 MHz

From the spectrogram window, it was possible to place the marker at the signal wave front and able to measure the high-end signal cut off in frequency domain as shown in measurement results in Table 13.

3.3.2. Experimental I/Q Signal Acquisition

The next step in the experimental setup was to pass the confirmed complex signal to the I/Q demodulator hardware to recover complex I and Q components. The I/Q demodulator operates at 5 volts, the power supply was set to 5 volts, and the device was confirmed to draw 200 mA of current. Preliminary results on the performance of the procured I/Q demodulator are given in Figure 4.

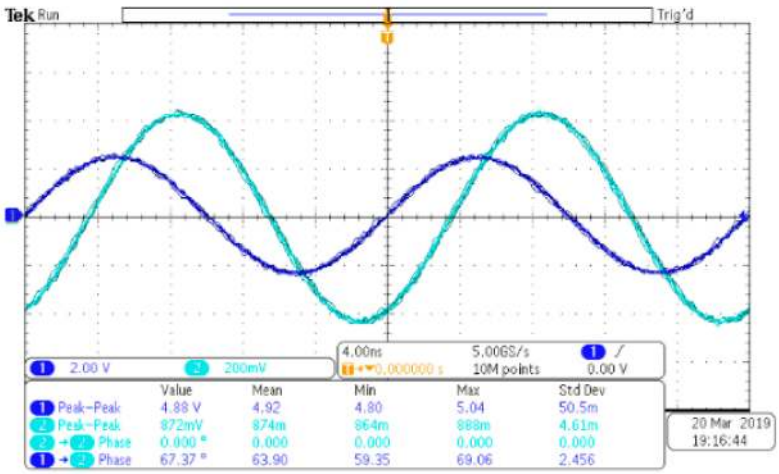

Figure 4. The oscilloscope output performance of I/Q demodulator with I component connected to Channel 1 and Q connected to Channel 2.

A complex signal from the signal generator was passed through I/Q demodulator, while outputs of the I/Q demodulator were passed to the oscilloscope for analysis. Analysis results revealed that the Q component lags the I component by 63.90°, as shown in Table 17 and Figure 4.

Table 17. I/Q demodulator performance measurements results.

Type	Measurements		Settings	
	Ch1	**Ch2**	**Ch1**	**Ch2**
Amplitude (P-P)	4.92 V	874 mV	2 V/div	200 mV/div
Phase	63.90°	0.00°	4 ns/div	4 ns/div

3.3.3. Experimental I/Q Signal Odd/even Order Sampling

The initial step in approaching the analysis of the captured signal wave data is used to verify that the exported CSV signal data is valid. The signal wave data acquired in Figure 4 was reproduced in Excel, and the phase and amplitude of Excel reproduced data that align with that presented in Figure 4. The Excel reproduced signal data is presented in Figure 5. It is important to note that the reproduced signal is limited to 256 samples, this is to ease the processing pressure on Excel.

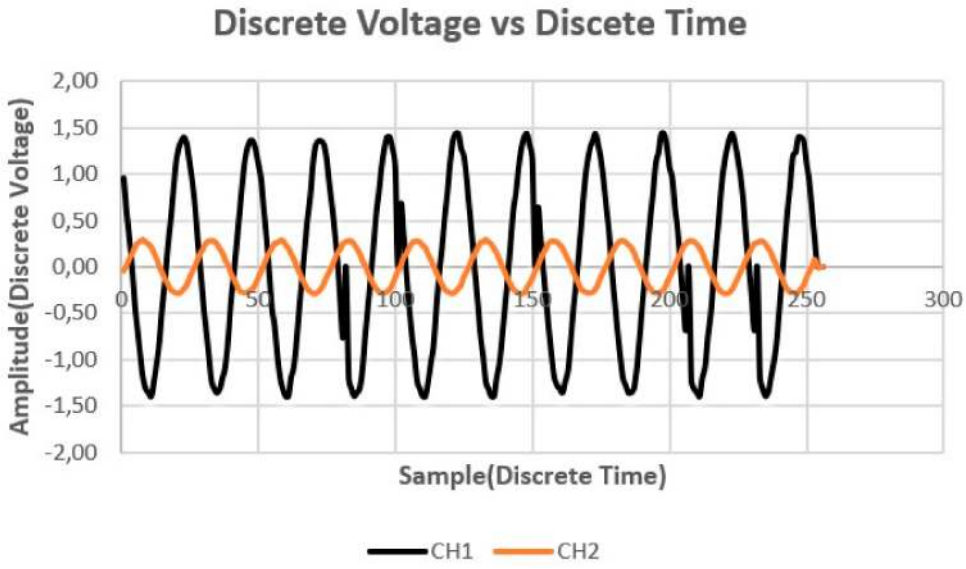

Figure 5. The Excel reproduced acquired I/Q demodulator samples.

The new odd/even order sampling mathematical model in Equations (12) and (13) was applied after Fourier Transform Analysis was applied to obtain the sample frequency behavior shown in Figure 6. Results in Figure 6 validate the research assumption that the new odd/even order sampling was half the sampling frequency.

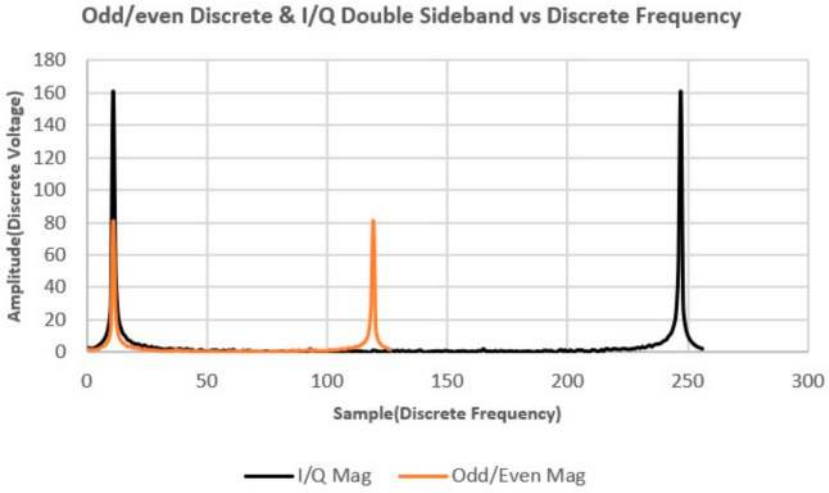

Figure 6. New odd/even order sample frequency behavior.

A separate investigation into effects of the new odd/even sampling onto phase behavior has indicated that it suffers from phase error with the I sampling component affected more than the Q sampling component, as shown in Figure 7. It is not clear what causes this behavior but reference [1] has recommended the use of a FIR filter to correct this issue.

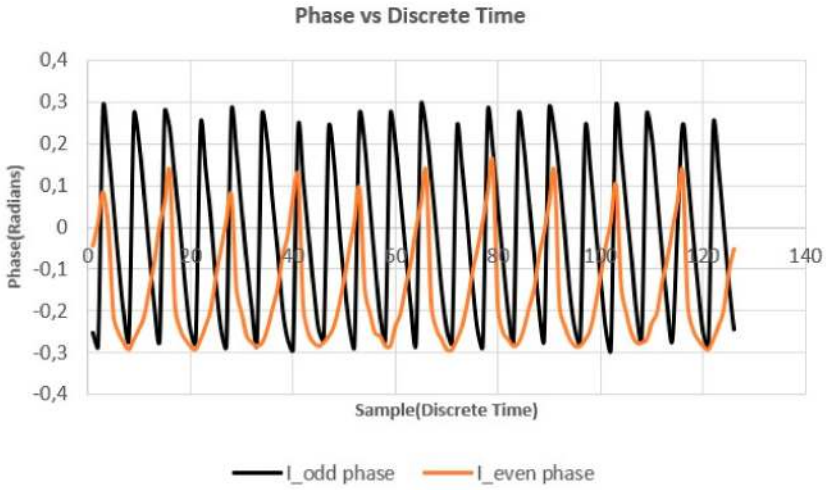

Figure 7. The phase error behavior of the new odd/even order sampling.

3.4. FPGA Implementation Investigation Towards Verification of Practical Applications of New Odd/even Order Sampling and A Signal-to-Noise (SNR) Performance Comparison to the Literature Available on Sampling Schemes

This section proposes new soft-core architecture for odd/even order sampling, with memory considerations shown in Figure 8. The architecture uses digital signal processing (DSP) slices under an intelligent Processing sub block. Block-RAM store signal data, Registers interface with a Scalar Processing sub block, and Process Containers contain logic to configure both Block-RAM and Register configurations. Axi bus access is primary self-controlled but state transitions such as write, read, and enable are externally controlled by Process Controllers. The derived Equations (12) and (13) are implemented onto a DSP and signal data is loaded through the axi bus from Block-RAM. Different signal source data selection, a switch between odd or even order through memory strobe, and any other interesting application procedure is software programmed through a Scalar Processing sub block. This section will implement the proposed architecture in Figure 8 and Table 18 and compare results to simulation for practical performance evaluation.

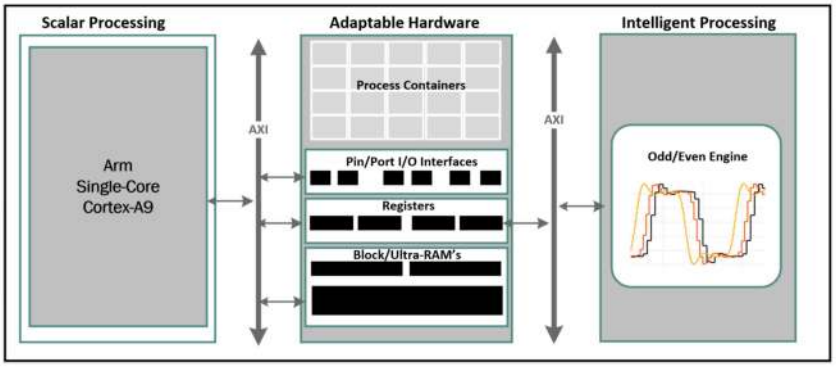

Figure 8. This presents the proposed new odd/even order sampling architecture block diagram.

Table 18. Proposed new odd/even order sampling architecture breakdown.

Sub Block	Functionality
Scalar Processing	Access to Registers as Datatype for Software
Adaptable Hardware	Process Container access to Digital Logic(LUT), Pin/Ports, Registers, Block RAM
Intelligent Processing	Access to a ground of DSP Slices for equation manipulation

3.4.1. Verification of Practical Application of New Odd/even Order Sampling

Laboratory verified signals captured in Section 3.3 were loaded and stored on Xilinx FPGA flash memory to accommodate implementation into FPGA chipset. Resource utilization for the proposed new soft-core architecture for odd/even order sampling is presented in Table 19, with total resource utilization at just below 50%.

Table 19. FPGA resource utilization for the new odd/even order sampling.

Description	Used	Available	Utilization
SliceUtilization			
Slice LUTs	2044	14,400	14.19%
LUT as Logic	1828	14,400	12.69%
LUT as Memory	216	6000	3.60%
SliceRegUtilization			
Reg as Flip Flop	3158	28,800	10.97%
Reg as Latch	0	28,800	0.00%
MultiplexerUtilization			
F7 Muxes	52	8800	0.59%
F8 Muxes	5	4400	0.11%
MemoryUtilization			
Black RAM	1.5	50	3.00%
DSPUtilization			
DSPs	2	66	3.03%
SpecificFeatureUtilization			
XADC	0	1	0.00%
Total Utilization			**48.15%**

Step size performance shown in Figure 9a,b is comparable to the expected results derived from the simulation presented in Section 3.2. The error performance in Figure 10 is also comparable with the expected simulation results in Section 3.2.

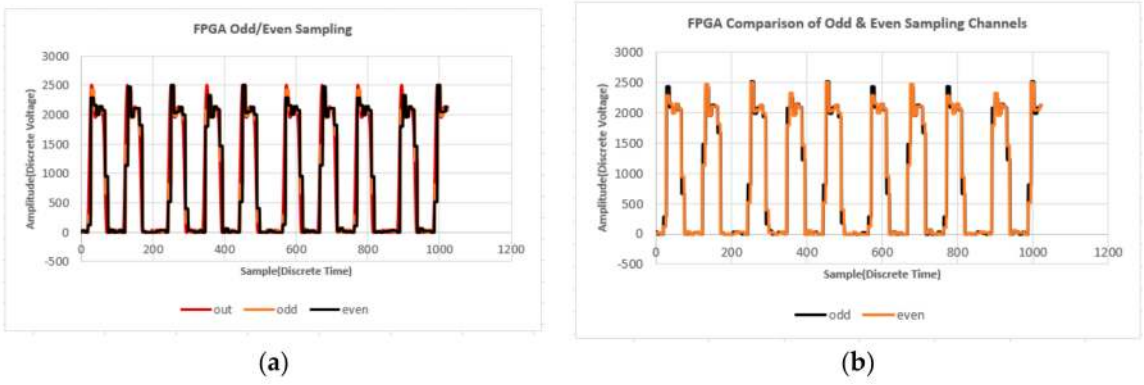

Figure 9. FPGA architecture implementation results: (**a**) Source signal which is in phase with I and odd/even order sampling results; (**b**) Odd and even order sampling results with Vivado integrated logic analyzer (ILA) window configured to 1 kilobyte.

Figure 10. This figure presents error performance for odd/even order sampling.

3.4.2. Signal-to-Noise (SNR) Performance Comparison to Literature Available Sampling Schemes

Implementation from the previous subsection was followed by implementation of other sampling schemes from the literature such as Mod-Δ, Mod-Δ (Gaussian), and Mod-Δ (Sinusoidal). According to reference [13], Mod-Δ (Gaussian) is a gaussian process whose PSD is flat within the designed band, and Mod-Δ (Sinusoidal) is a sinusoidal waveform whose frequency is chosen at random, uniformly on [0, B), and whose amplitude is the square root of covariance.

Many field tests were conducted to investigate the realistic noise behavior of Radar systems. The field tests were conducted at OR Tambo International Airport. The best noise performance was stored and noise was extracted for both I and Q components as shown in Figure 11. In Mod-Δ (Sinusoidal) the sinusoidal can be replaced by the noise in Figure 11 to make Mod-Δ (Noise) within the specification of random frequency.

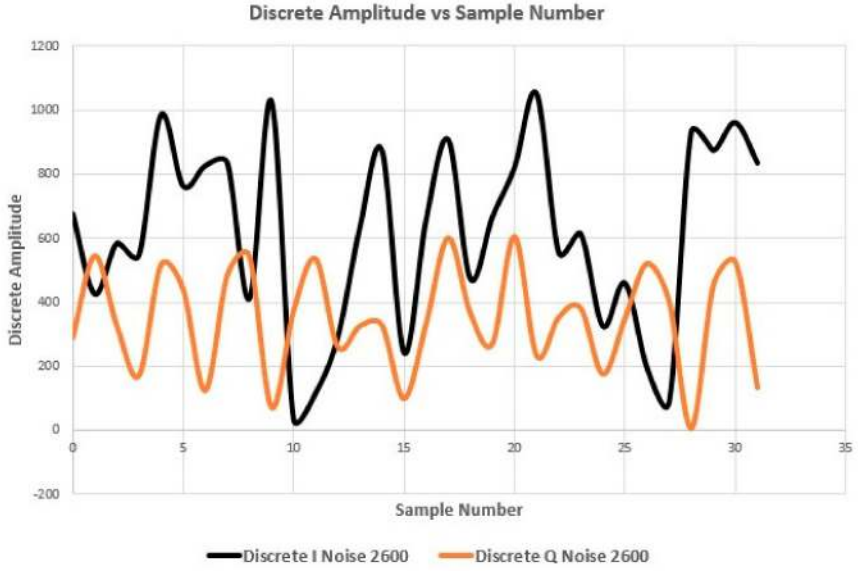

Figure 11. The noise captured from Radar source on a field test.

Implementation Mod-Δ sampling implemented under Intelligent Processing sub block was followed by that of Mod-Δ (Gaussian). The mathematical model equations of Mod-Δ sampling were replaced by that of Mod-Δ (Gaussian) sampling. The modification is also evident with resource

utilization in Tables 20 and 21 registering a DSP usage of just over 30% and 33% with total resource utilization at just above 75% and 78% respectively.

Table 20. FPGA resource utilization for the existing Mod-Δ sampling.

Description	Used	Available	Utilization
SliceUtilization			
Slice LUTs	2044	14,400	14.19%
LUT as Logic	1828	14,400	12.69%
LUT as Memory	216	6000	3.60%
SliceRegUtilization			
Reg as Flip Flop	3158	28,800	10.97%
Reg as Latch	0	28,800	0.00%
MultiplexerUtilization			
F7 Muxes	52	8800	0.59%
F8 Muxes	5	4400	0.11%
MemoryUtilization			
Black RAM	1.5	50	3.00%
DSPUtilization			
DSPs	20	66	30.30%
SpecificFeatureUtilization			
XADC	0	1	0.00%
Total Utilization			**75.45%**

Table 21. FPGA resource utilization for the existing Mod-Δ(Gaussian) sampling.

Description	Used	Available	Utilization
SliceUtilization			
Slice LUTs	2044	14,400	14.19%
LUT as Logic	1828	14,400	12.69%
LUT as Memory	216	6000	3.60%
SliceRegUtilization			
Reg as Flip Flop	3158	28,800	10.97%
Reg as Latch	0	28,800	0.00%
MultiplexerUtilization			
F7 Muxes	52	8800	0.59%
F8 Muxes	5	4400	0.11%
MemoryUtilization			
Black RAM	1.5	50	3.00%
DSPUtilization			
DSPs	22	66	33.33%
SpecificFeatureUtilization			
XADC	0	1	0.00%
Total Utilization			**78.48%**

The implementation of Mod-Δ (Gaussian) sampling under an Intelligent Processing sub block was followed by that of Mod-Δ (Noise). The mathematical model equations of Mod-Δ (Gaussian) sampling were replaced by that of Mod-Δ (Noise) sampling. The modification is also evident in the resource utilization in Table 22, which registered a DSP usage of just over 40% with a total resource utilization of just above 86%.

Table 22. FPGA resource utilization for the existing Mod-Δ(Noise) sampling.

Description	Used	Available	Utilization
SliceUtilization			
Slice LUTs	2044	14,400	14.19%
LUT as Logic	1828	14,400	12.69%
LUT as Memory	216	6000	3.60%
SliceRegUtilization			
Reg as Flip Flop	3158	28,800	10.97%
Reg as Latch	0	28,800	0.00%
MultiplexerUtilization			
F7 Muxes	52	8800	0.59%
F8 Muxes	5	4400	0.11%
MemoryUtilization			
Black RAM	1.5	50	3.00%
DSPUtilization			
DSPs	27	66	40.91%
SpecificFeatureUtilization			
XADC	0	1	0.00%
Total Utilization			86.06%

After the four implementations, a usable SNR investigation was conducted on a Vivado ILA tool. The investigation involved experiments for quantization resolution from 2 to 12 bits, and SNR results are presented in Figure 12. SNR shows that below 3 bits, the resolution of Mod-Δ has the worst performance when registering 12 dB signal distortion, while Mod-Δ (Noise) had the worst overall performances for all types of quantization designs between 2 and 12 bits, and the new odd/even had average overall performance. Above 8 bits, the new odd/even order sampling and Mod-Δ (Gaussian) provided the best performance, with the new odd/even order sampling recording 6 dB.

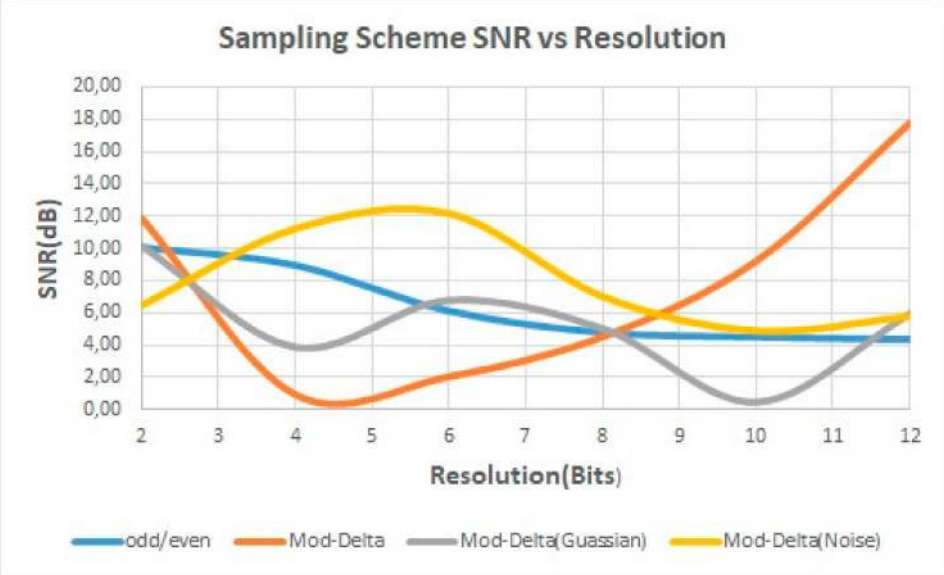

Figure 12. This figure presents SNR performance between the new odd/even order, Mod-Δ, Mod-Δ (Gaussian) and Mod-Δ (Noise) sampling.

4. Discussion

Section 3 presented numerical and experimental merits in four subsections. Section 3.1 derived a numerical demonstration of the proposed odd/even order sampling. Section 3.2 used the numerical model to a develop simulation model to investigate MSE performance on an odd/even order sampling. A clear description of numerical parameter that represent quantization error was provided.

Quantization error is very important in this study as it is largely influenced by the arrangements of samples. Figure 3 from the simulation and Figure 10 from FPGA implementation seems to indicate that quantization error behavior is consistent between the simulation and the implementation.

Section 3.3 develops an experimental setup to capture source signal data and used it to investigate the sample frequency performance using Excel for the implementation of the numerical model developed in Section 3.1. Spectral analysis on Excel in Figure 6 indicated that the sample frequency has been reduced after odd/even order sampling, which validates the research assumption that initiated this study. Section 3.4 implemented proposed odd/even order sampling, Mod-Δ, Mod-Δ (Gaussian), and Mod-Δ (Noise) on an FPGA platform to capture computational requirements. Section 3.4 went further to investigate SNR performance for the four sampling schemes to demonstrate the merits of the new odd/even order sampling.

It is important to note that the quantization error based on MSE calculation for both simulation and FPGA implementation is comparable, as shown in Figure 3 for the simulation and Figure 10 for the implementation. A detailed step size and dynamic range investigation revealed that the step size reduced from 8 kHz to 2 kHz, while the dynamic range slightly reduced from 1.185 Volts/ms to 1.088 Volts/ms. Implementation investigations have revealed that FPGA resource utilization for the new odd/even order sampling, Mod-Δ, Mod-Δ(Gaussian), and Mod-Δ(Noise), respectively, is approximately 45%, 75%, 78%, and 86%. This is a clear indication FPGA is very undemanding when it comes to computation requirements, as it has the least resource utilization compared to the other studied schemes.

5. Conclusions

By reducing the sample frequency of digitized signal, the issue of complicated architecture and expensive FPGA selection can be reduced. This paper proposes a new novel odd/even order sampling architecture that eliminates odd and even sampling on quadrature signals to reduce sample frequency. It uses realistic case studies that investigate the behavior of the proposed new novel odd/even order sampling architecture using computational simulation, laboratory studies, and implementation experimentation. In addition:

- A simulation investigated step-size, dynamic range, and dynamic range error behavior. Results verified that odd/even ordered sampling can significantly reduce the sample frequency from 8 kHz to 2 kHz, while not adversely affecting the dynamic range.
- Laboratory experimentation investigated the feasibility of the research assumption that ordered sampling reduces sample frequency. Results verify this assumption using time and spectral analysis.
- Implementation experimentation the investigated feasibility of implementing ordered sampling on a FPGA platform in comparison to sampling architecture in the literature. We also investigated the SNR behavior of odd/even ordered sampling in comparison to Mod-Δ, Mod-Δ (Gaussian), and Mod-Δ (Noise) literature. Results indicate that odd/even order sampling is the most economical method in comparison to architectures evaluated with resource utilization at 45%. SNR results were not conclusive for a sampling resolution below 8 bits, for a resolution between 8 bits and 11 bits odd/even ordered sampling is the second-best performer, while showing the best performance for a sampling resolution above 11 bits.

Future studies will involve a detailed study of computation requirements of the different sampling schemes with numerical tracking of the cause for deviations in resource utilization. Mod-Δ(Sinusoidal) has frequency domain and amplitude constraints defined as:

- Random frequency uniformly distributed [0, B)
- Amplitude is a square root of covariance.

Mod-Δ(Sinusoidal) generally requires the sinusoid to be noisy to meet the frequency constraint, while the amplitude of that noise must be a square root of the covariance. The sinusoid used in this

paper was noise signal acquired realistic Radar equipment, as shown in Figure 11. This acquisition was made without any verification that was conducted against the Mod-Δ(Sinusoidal) amplitude constraint. Future work also includes an amplitude investigation into the implementation of Mod-Δ(Noise) that validates whether it satisfies the square root of a covariance constraint.

Author Contributions: M.M., A.A. and A.N.H. conceived and designed the experiments; M.M. performed the experiments; M.M., A.A. and A.N.H. analyzed the data; and M.M. wrote the paper.

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Nomenclature

RAM	Random Access Memory
FPGA	Field Programmable Gate Array
LUT	Look Up Table
DSP	Digital Signal Processing
ILA	Integrated Logic Analyzer
RMS	Root Mean Square
ARMS	Average Root Mean Square
PDF	Probability Distribution Function
CDF	Cumulative Distribution Function
PSD	Power Spectral Density
AR-PSD	Autoregressive Power Spectral Density
ADC	Analog-to-Digital Converter
SNR	Signal-to-Noise Ratio
SQNR	Signal-to-Quantization-Noise Ratio
R	Bit Rate
D	Distortion
MASH	Multi-Stage Noise Shaping
dB	Decibels
dBm	Decibel-milliwatts
dBFS	Decibels Relative to Full Scale
dBTP	Decibels True Peak
MSE	Mean Square Error
DR	Dynamic Range
Mod-Δ	Mod-Delta
REW	Radar & Electronic Warfare
PRI	Pulse Repetition Interval
PRF	Pulse Repetition Frequency
SAR	Synthetic Aperture Radar
ISAR	Inverse Synthetic Aperture Radar
EW	Electronic Warfare
ECM	Electronic Counter Measure
ECCM	Electronic Counter-Counter Measure
ESM	Electronic Support Measure
RGPO	Range Gate Pull Off
VGPO	Velocity Gate Pull Off
AGPO	Angle Gate Pull Off
RSP	Radar Signal Processor
DRFM	Digital Radio Frequency Memory
FMCW	Frequency Modulated Continuous Wave
AI	Artificial Intelligence
ML	Machine Learning
ANN	Artificial Neural Network
BPNN	Back-Propagation Neural Network

FNN	Fuzzy Neural Network
GA-NN	Generic Neural Network
GA	Generic Algorithm
Hz	Hertz
kHz	Kilohertz
MHz	Megahertz
GHz	Gigahertz
I	Current
V	Voltage
DoE	Design of Experiment

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