On-Chip Analog Output Response Compaction

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Abstract

In this paper, we propose a technique for on-chip analog output response compaction in order to implement self-test capabilities in analog and mixed-signal integrated circuits. The integration function is identified as a powerful analog compression scheme and an analog signature analyzer is proposed. The opamp-based implementation allows to define single and multiple-input versions. The multiple-input analyzer permits the monitoring of some extra internal nodes in addition to the classical output nodes, or the concurrent control of both voltage and current levels. This ability leads to an improvement of the circuit testability and consequently, the on-chip response evaluation gives a higher fault coverage than the off-chip one.

1. Introduction

The development of CMOS technologies gives the possibility of designing high quality analog circuits as well as complex mixed analog/digital circuits. Due to their monolithic realization and also to the inherent complex nature of analog signals, testing such circuits is still a hard task. As experienced from testing complex digital ICs, this task can only be managed economically if test requirements are taken into account during the design phase.

Built-In Self-Test (BIST) techniques are known to be efficient to reduce the test cost of a circuit. Indeed, these techniques allow to transfer some of the test resources from the Automatic Test Equipment into the Circuit Under Test. In particular on-chip signature analysis consists in designing built-in devices to (i) compress the output response into a reduced set of data values called the signature, (ii) compare this signature to the golden one and (iii) generate a "go/no-go" signal.

In the case of digital circuits, various techniques exist to compress the output response sequence with a logarithmic factor to obtain a test signature [1], thus allowing to significantly reduce the amount of storage. For analog circuits the compression operation aims at replacing a continuous-time output response by a steady-state analog signature. So, this makes it possible to replace the multiple-time observation of several sampled signals by a single-shot measurement.

In the past, a number of efficient devices has been reported for response compaction in digital circuits [2]. Concerning analog circuits, the state of the art is not so advanced. Only a limited number of papers deals with the problem of analog response compaction. Mainly two following approaches have been prospected.

The first one is based on specification monitoring [3,4]. Various analog controllers are implemented that verify the goodness of defined behavioral parameters. This approach suffers two main drawbacks: it is not possible to evaluate the efficiency of the method in terms of fault coverage, and the test duration may be prohibitive.

The second approach is based on deterministic test techniques in which analog test stimuli are generated with the aim of detecting targeted faults. In the H-BIST technique of Olhetz [5], the analogue responses are first digitalized before compressed in a Linear Feedback Shift Register (LFSR). In the same way, Nagi [6] uses the digital integrators of Rajsky [2] to generate signatures for analog and mixed-signal circuits. Due to the use of a digital compression procedure, these techniques only address a given class of mixed-signal circuits, namely circuits having an on-chip ADC. For other types of circuit (purely analog circuits or mixed-signal circuits without ADC) it would be necessary to add this on-chip ADC. Because of the extra silicon area needed to implement this module, this option is discarded.

This paper is organized as follows. Section 2 gives some definitions on the concept of analog response analysis. It is demonstrated the integration function can be considered as a very interesting analog response compression technique. Section 3 gives the detailed implementation of our analog signature analyzer. Section 4 shows the advantages of the multiple-input implementation in terms of fault coverage enhancement. The application of the technique is presented for a switched-capacitor circuit in section 5 and finally, section 6 discusses the performances of the proposed compression technique and gives some concluding remarks.

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2. Analog Response Compaction

In digital world, several techniques have been developed in order to obtain a m-bit Digital Signature (DS) from an n-vector output response sequence $\{O_i\}$. Among these various digital compaction procedures, two techniques are found to be currently used: the polynomial division [1] and the cumulative addition [2].

The first technique uses a LFSR to obtain the single-output circuit signature as the remainder of the division between the polynomial associated with the output sequence and the characteristic polynomial of the LFSR. As an extension of this technique, MISRs allow to cope with multiple-output circuits.

The second technique consists in successively adding the n output vectors O_i. At the end of the compression phase the m-bit register contains the final signature that corresponds to the bit-by-bit discrete sum of all the n output vectors.

Up to now only few research works have been done on the way to realize analog compaction using on-chip analog devices. Considering the two main digital techniques, it appears it is not obvious to derive an equivalent to the polynomial division for analog signature elaboration. At the opposite, the discrete sum of successive vectors in digital field has a straightforward equivalent in the analog domain. The discrete sum in the digital domain corresponds to continuous sum in the analog domain, i.e. the integration function. So, we propose to perform the integration of the continuous-time output test response O(t) between time t_1 and t_n to build the Analog Signature (AS):

$$DS = \sum_{i=1}^{n} O_i \quad \Leftrightarrow \quad AS = \int_{t_1}^{t_n} O(t) \, . \, dt \qquad [1]$$

In the context of a fault-based strategy, the use of on-chip opamp-based integrator to compress analog data has been concurrently proposed by two research teams [7,8]. Therefore, the two approaches are somewhat different. The ABILBO structure of Lubaszewski et al. aims at achieving both test frequency generation and test response compaction. This is a frequency approach based on the determination of the time needed for the double-integrated output signal to reach a reference level. At the opposite, our technique is based on the integration of a transient response. So, we simply replace the hard-to-manage observation of a time-dependent voltage response by a single-shot on-chip voltage comparison.

3. Analog Signature Analyzer

The objective is now to build a module that implements the integration function as a compression technique to compute the analog signature of the CUT. This analog module has to be realized with a simple circuitry in order to exhibit a reasonable silicon overhead.

The implementation we propose for the analog signature analyzer is based on the use of the classical opamp integrator structure, as illustrated in figure 1. Two additional switches (M1-2) have been added for initialization and integration time control purposes. We define a logic control signal C_i that allows to configure the analyzer either in stand-by or integration mode.

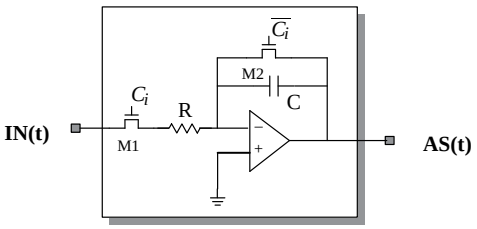

Figure 1: Analog signature analyzer

When a low logic value is applied on C_i, the output is initialized to 0 by bypassing the capacitor C, otherwise the module performs the integration function. So, the Analog Signature AS provided by the module is equal to the input signal integral weighted by the time constant of the integrator τ=RC.

To validate the opamp based implementation of the integration function, a second order Sallen-Key filter has been studied as an example (see figure 2). Using a catastrophic fault model (open and short on MOS transistors and passive components), we determine the fault coverage of the filter. This fault coverage is calculated processing either the transient response O(t) during the test interval, or the analog signature AS delivered by the analyzer. The input test stimulus is a pulse signal. This type of test stimulus has been identified as very efficient and is widely used for test purpose [9,10].

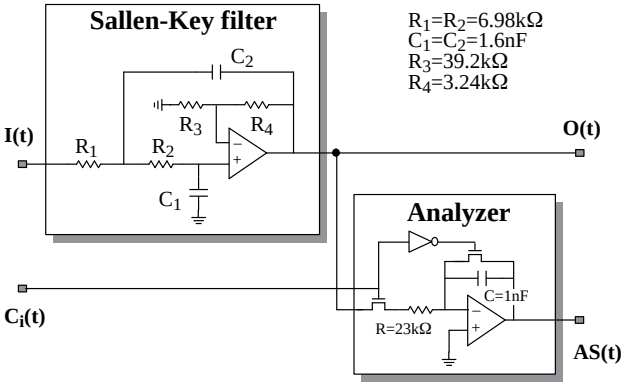

Figure 2: Opamp-based analyzer validation

Under these conditions, using a classical tolerance of 10% around the nominal response of the filter, 41 of 48 faults are detected when processing the transient response. This off-chip time-domain analysis gives a fault coverage FC_{ref} equal to: FC_{ref} =85.4%. This fault coverage is considered as the reference value for the filter under test.

In a second step, the fault coverage is established using the analog signature; the analyzer input is directly connected

to the output node of the filter. Fault detection is then determined by a single comparison between the signature generated for faulty circuits and the pre-determined fault-free one, taking into account the same tolerance of 10%. Simulation results demonstrate that 40 of 48 faults are detected, that corresponds to a fault coverage FC_{AS} equal to: FC_{AS} =83.3%.

Comparison between time-domain and signature analysis results shows that among the 41 faults normally detected when processing the transient response O(t), 40 faults are detected when observing the analog signature AS. So, for this example, the aliasing problem occurs for only one fault of the list. This result points out that the continuous integration function can be considered as an efficient analog compression technique and that the proposed implementation of the analyzer correctly works.

The real implementation of such an opamp-based integrator will certainly suffers some realistic problems. For example, the offset signal induced by unavoidable symmetry defects in the differential stage may change output value thus invalidating the interpretation of the output level. So, in a real case we will have to take into account this problem. One of the possibility could be to evaluate the offset value during the initialization phase in order to take it into account for result analysis.

4. Multiple-Input Analog Signature Analyzer

On the basis of the analog signature analyzer presented above, we define a multiple-input module. Indeed, the analyzer is based on the classical opamp integrator and this integrator exists in both single and multiple-input versions. So, taking advantage of the opamp summation properties, it is easy to define a multiple-input signature analyzer implementation, as described in figure 3.

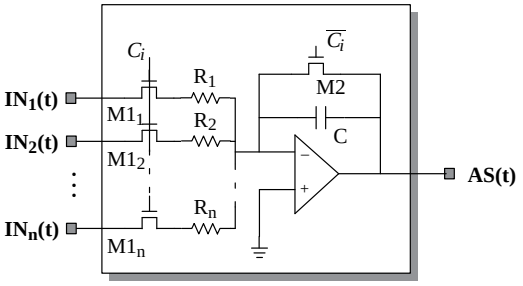

Figure 3: Multiple-input analog signature analyzer

The area overhead induced by the replacement of a single-input analyzer by a multiple-input one is very low: it is sufficient to add one resistor and one switch per additional input, a single opamp and a single capacitor being required to perform the integration.

This multiple-input signature analyzer can be considered as the analog counterpart to the digital Multiple-Input Shift Register (MISR). Obviously, as in the digital domain, such a structure can be used to implement self-test capabilities for multiple-output analog circuits with a minimal area overhead. It is to remark that it has been mandatory to develop multiple-input analyzers for digital circuits, since these circuits usually exhibit a high number of output pins. On the contrary, analog circuits often present few output pins, and frequently a single output pin (for example when dedicated to filtering applications). In this case, one can wonder the interest of a multiple-input analyzer. Actually, we suggest at least two different uses of such a structure: to perform either voltage testing based on multiple-node observation or mixed voltage/current testing. These solutions will be detailed in the following sections.

4. 1. Multiple-node voltage testing

The first solution investigated for the use of a multiple-input analog signature analyzer consists in concurrently processing the output nodes of the circuit together with some internal nodes. The analog signature generated is then based on a multiple-node observation. In fact, in this situation the multiple-input analyzer adds some extra observation points in the circuit, thus increasing the global observability. Observability is commonly accepted as one of the most important attribute of the testability, and so, by increasing the observability, we make the circuit more testable.

To illustrate this idea, we study the fault coverage achieved for the previous Sallen-Key filter using a 2-input signature analyzer. One input of the module is used to process the filter output node and the other constitutes the additional observation point. Obviously, this point has to be judiciously chosen to be able to get an increase in fault coverage. So, the two analyzer inputs are connected to (i) the output node of the filter and (ii) the output node of the opamp differential stage as illustrated in figure 4.

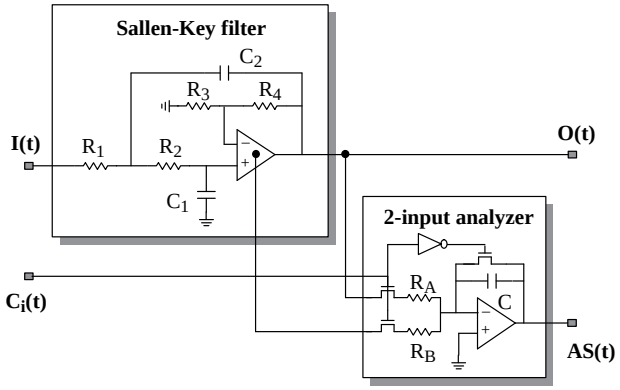

Figure 4: Multiple-node voltage observation

The HSPICE fault simulations show that comparing the faulty analog signatures with the fault-free one, only one fault is non-detected. The corresponding fault coverage FC_{AS*} is equal to: FC_{AS*} =97.9%.
Keeping in mind that the reference fault coverage achieved by an off-chip time-domain analysis is equal to FC_{ref}=85.4%, we note a very significant increase when

using the multiple-input analyzer. So, as expected the addition of an internal observation point greatly improves the circuit testability.

It has to be emphasized that usually, when using signature analysis techniques, the problem is to minimize the number of error masking phenomena to obtain a fault coverage as close as possible to the one achieved by an external test. With the multiple-input analog analyzer, not only we can partially overcome aliasing problems by introducing redundancy but also we permit an improvement of the fault coverage. This solution consequently goes beyond the classical objectives of signature analysis techniques.

4. 2. Mixed voltage/current testing

The second solution investigated for the use of a multiple-input analog analyzer is based on mixed voltage/current testing. Indeed, within the last few years, investigations in the domain of current testing have demonstrated the interest of this approach for analog circuits [11]. Furthermore, it has been pointed out that the use of both voltage and current measurements often allows to maximize the fault coverage, since these two types of test are complementary [12]. We then propose to use the multiple-input analyzer to concurrently observe the output voltage together with the supply current of the circuit.

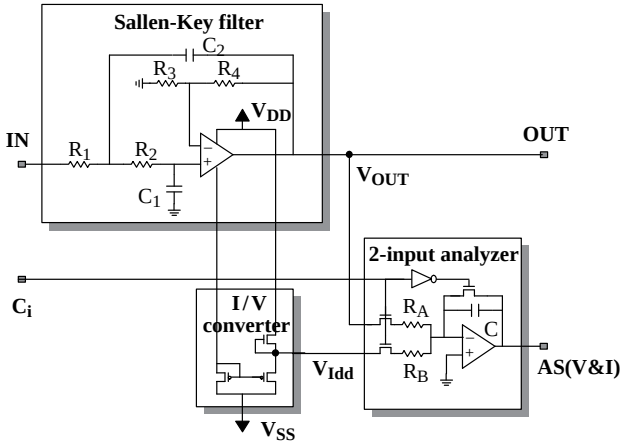

Figure 5: Mixed voltage/current signature

This solution is illustrated in figure 5 for the previous Sallen-Key filter with a 2-input analyzer. The analyzer being designed for voltage integration, an additional sub-circuit is required to provide a voltage $V_{Idd,}$ which is an image of the supply current Idd of the CUT. The two analyzer inputs are then connected to (i) the output node V_{OUT} of the CUT and (ii) the output node V_{Idd} of the I/V converter. The converter we use for test performance evaluation is based on the work related in [13] in the area of current sensor development.

Comparison between the simulated faulty signatures and the pre-determined fault-free one shows that this structure allows to detect 47 of 48 faults for the filter. The resulting fault coverage $FC_{AS(V\&I)}$ is equal to: $FC_{AS(V\&I)}$ =97.9%.

So, as for the analog signature based on multiple-node observation, by generating a mixed voltage/current signature, the multiple-input analyzer allows to obtain a higher fault coverage than that usually obtained by a direct time-domain observation: the fault coverage is increased from 85.4% to 97.9%.

5. Switched-capacitor implementation

This section is dedicated to the application of the previous analog signature analyzer to switched-capacitor circuits. A 4th order Sallen-Key filter (see figure 6) has been chosen as an example and we study the fault coverage achieved using either the transient output voltage, or the analog signature of the circuit. Fault coverage calculation is based on HSPICE fault simulations, taking into consideration all the catastrophic faults (short and open) on MOS transistors, capacitors and switches.

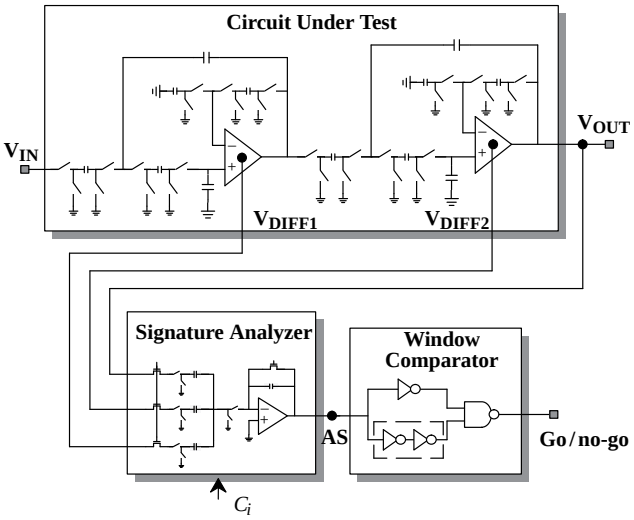

Figure 6: Self-testing switched-capacitor filter

In a first step, we determine the fault coverage obtained by the external time-domain analysis as the reference value: FC_{ref} (filter) =81.5%.
Then in a second step, we determine this fault coverage when the analog signature analysis technique is used. For this, we have to define the switched-capacitor implementation of the analyzer. This implementation is very straightforward, replacing each resistor by a periodically charged and discharged capacitor through 4 switches. After minimization of the number of switches in case of a multiple-input analyzer, we obtain the implementation depicted in figure 6. This 3-input analyzer is used to generate the analog signature AS, which is based on the observation of the output node V_{OUT} of the filter together with the two output nodes V_{DIFF1} and V_{DIFF2} of each opamp differential stage.

Furthermore, the comparison of the signature with the fault-free value is realized on-chip, using a window comparator. The comparison window corresponds to the

good circuit signature with a 10% tolerance and is determined by an appropriate sizing of the inverters [14]. The comparator then delivers a go/no-go signal that allows to directly declare the CUT as a faulty or a fault-free circuit.

Fault simulation results show that the fault coverage achieved is equal to: FC_{AS} (filter) =95.4%. So, as for the continuous-time filter example, we note a significant improvement of the fault coverage achieved. Moreover, the on-chip window comparator allows a very simple test procedure and the circuit can directly be declared faulty or fault-free, just monitoring the go/no-go signal.

6. Discussion and Conclusion

To properly test an integrated circuit necessitates to use a complex and expensive Automatic Test Equipment (ATE). This is particularly true when mixed analog/digital circuits are concerned. In this case the ATE has to be equipped with high performance analog signal generation and capture resources. Also sophisticated fixturing and connecting are required in order to manage high frequency measurements and minimize the noise level.

To move some test functions from ATE onto chip is one of the most important issues of the present day research on test. The problem has found some kinds of solution in the digital field where on-chip (or on-board) structures exist that can be used to generate a test sequence, compress the resulting response and derive an analog signature. Up today, no equivalent facilities exists in the analog domain.

In this work, we propose a system to derive an analog signature for analog circuits (or analog parts of mixed-signal circuits). This system may be viewed as an analog counterpart of the cumulative adder proposed in [2] for test response compaction. The idea is to replace the discrete summation of a digital output sequence by the integration of an analog transient response. This operation can be easily implemented using an on-chip opamp-based integrator. This analog signature analyzer then permits to replace the hard-to-manage external monitoring of a continuous time-varying response by a simple single-shot analog measurement. Obviously, due to the fact that different transient responses may present an identical integral value (two different curves may have an identical surface), aliasing problems may also occur in analog domain as in digital one. This may lead to fault coverage values under that obtained by a direct observation of the global transient response. The ability of our system to concurrently monitor different internal test points allows to partly overcome this drawback. Moreover because additional internal points are observed, some extra faults may be caught. The example given in section 4.1 shows that we can drastically improve the fault coverage by using this technique. Also, it is shown that our system allows to implement the concurrent control of both voltage and current levels, thus allowing to fully profit from the complementarity between voltage and Iddq test techniques. Finally, the analog integrator we propose may be extended from continuous-time to sampled-time domain. This ability is demonstrated from the switched capacitor example given in section 5.

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