On-Chip ECC for Multi-Level Random Access Memories

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In this talk we investigate a number of on-chip coding techniques for the protection of Random Access Memories which use multi-level as opposed to binary storage cells. The motivation for such RAM cells is of course the storage of several bits per cell as opposed to one bit per cell [1]. Since the typical number of levels which a multi-level RAM can handle is 16 (the cell being based on a standard DRAM cell which has varying amounts of voltage stored on it) there are four bits recorded into each cell [2]. The disadvantage of multi-level RAMs is that they are much more prone to errors, and so on-chip ECC is essential for reliable operation. There are essentially three reasons for error control coding in multi-level RAMs: To correct soft errors, to correct hard errors, and to correct read errors. The source of these errors is, respectively, alpha particle radiation, hardware faults, and data level ambiguities. On-chip error correction can be used to increase the mean life before failure for all three types of errors. Coding schemes can be both bitwise and cellwise. Bitwise schemes include simple parity checks and SEC-DED codes, either by themselves or as product codes [3]. Data organization should allow for burst error correction, since alpha particles can wipe out all four bits in a single cell, and for dense memory chips, data in surrounding cells as well. This latter effect becomes more serious as feature sizes are scaled, and a single alpha particle hit affects many adjacent cells. Burst codes such as those in [4] can be used to correct for these errors. Bitwise coding schemes are more efficient in correcting read errors, since they can correct single bit errors and allow the remaining error correction power to be used elsewhere. Read errors essentially affect one bit only, since the use of Grey codes for encoding the bits into the memory cells ensures that at most one bit is flipped with each successive change in level. Cellwise schemes include Reed-Solomon codes, hexadecimal codes, and product codes. However, simple encoding and decoding algorithms are necessary, since excessive space taken by powerful but complex encoding/decoding circuits can be offset by having more parity cells and using simpler codes. These coding techniques are more useful for correcting hard and soft errors which affect the entire cell. They tend to be more complex, and they are not as efficient in correcting read errors as the bitwise codes. In the talk we will investigate the suitability and performance of various multi-level RAM coding schemes, such as row-column codes, burst codes, hexadecimal codes, Reed-Solomon codes, concatenated codes, and some new majority-logic decodable codes. In particular we investigate their tolerance to soft errors, and to feature size scaling.

References

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