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On-chip Hot Spot Remediation with Miniaturized Thermoelectric Coolers

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Abstract The rapid emergence of nanoelectronics, with the consequent rise in transistor density and switching speed, has led to a steep increase in chip heat flux and growing concern over the emergence of on-chip "hot spots" in microprocessors, along with such high flux regions in power electronic chips and LED's. Miniaturized thermoelectric coolers (μ-TEC's) are a most promising cooling technique for the remediation of such hot spots. This paper presents a comprehensive review of recent advances in novel applications of superlattice, mini-contact, and silicon-based miniaturized thermoelectric coolers in reducing the severity of on-chip hot spots.

Keywords Thermal management · Electronic cooling · Thermoelectric cooler · Hot spot cooling

Introduction

Microelectronics has become the heart of any modern electronic product from home/office PC systems to advanced military/defense electronic systems. However, because all the microelectronic devices require power for their use, the conversion of electrical energy to thermal energy is an unavoidable byproduct of the normal operation of any electronic devices and leads to higher microprocessor temperature that, if not properly managed, will significantly affect the performance, leakage power, and reliability of microelectronic chip, assembly, and product. Moreover, recent advances in device miniaturization and design complexity are causing highly non-uniform power distribution on the microprocessors, producing "high-flux hot spots". These specific regions on the chip can have a heat flux several times higher than the chip average, and of the order of 1 kW/cm^2, thus resulting in exceedingly high local temperatures and degrading microprocessor performance and system reliability dramatically (Shakouri 2006). On the other hand, if effective localized cooling of the hot spots can be achieved, the resulting "cold chip" can produce speed gains as large as 200% in some CMOS microprocessors (Tritt 2006). For this reason, mitigating the chip-level hot spot effects through localized cooling has become one of the most significant factors in the design of high-performance electronic products and developed into a primary driver for today's innovation in electronics cooling technology. Due to technical difficulties, the development of efficient cooling technologies to handle such micro-scale high flux hot spots poses a significant challenge in thermal management research and has become a primary roadblock in developing the next generation of microelectronic devices and systems.

Two-phase flow cooling techniques, such as microchannel heat sinks, spray cooling, and pool boiling, provide very high heat transfer coefficients and could be used to meet high-flux cooling requirements as well

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as provide thermal management in future spacecraft and space stations (Di Marco and Grassi 2002; Silk et al. 2008; Kabov et al. 2007). However, under microgravity conditions, the thermal/fluid characteristics of two-phase systems could significantly differ from that at 1-g condition. Although extensive research has been conducted in this area since the Space Station was proposed, the two-phase heat transfer mechanisms under microgravity environments are still unclear. Therefore, successful use and optimization of two-phase cooling systems for space applications, requires the determination of the as yet unavailable flow patterns, pressure drops, and heat transfer coefficients associated with the flow at microgravity conditions. Because of this lack of understanding, lower power components have to be used in space-based systems since higher power systems requiring the use of two-phase flow has been considered to be risky (Kim 2003). Therefore, the relatively poor understanding of gravity effect on two-phase flow heat transfer has been identified as one of the primary obstacles to reliable design of electronic cooling systems.

Recently advanced miniaturized thermoelectric coolers (TEC's) have received great attention for hot spot thermal management because these solid state devices can offer high reliability, can be locally and selectively applied for spot cooling, can provide high cooling heat flux, can be integrated with IC processing, and is not vulnerable to the gravity effect (Wang et al. 2009; Yang et al. 2007; Wang and Bar-Cohen 2007a, b; Chowdhury et al. 2009; Wang et al. 2006a, b). In this paper, the recent advances of several advanced miniaturized thermoelectric coolers for on-chip hot spot remediation, including mini-contact enhanced TEC's, silicon μTEC's, superlattice TEC's, and miniaturized bismuth telluride TEC's are evaluated.

Mini-Contact Enhanced TEC

Conventional thermoelectric coolers can only provide a cooling heat flux about 5 to 10 W/cm^2, which severely limits the application of these devices to hot spot remediation (Shakouri 2006). Recently, a novel use of a mini-contact pad, which connects the TEC and the silicon chip, thus concentrating thermoelectric cooling power on the top of the silicon chip to significantly improve hot spot cooling performance, was proposed and investigated (Wang et al. 2009; Yang et al. 2007). The physical phenomenon underpinning the use of mini-contact-enhanced thermoelectric coolers is displayed in Fig. 1, where it can be seen that the mini-contact pad is used to concentrate the thermoelectric cooling power on the top of the silicon chip. A 3D FEM thermal model was developed and used to determine the efficacy of applying such a mini-contact TEC cooler to a chip with 70 W/cm^2 background heat flux 1250 W/cm^2, 400 μm × 400 μm hot spot. Figure 2 shows the temperature profiles that could be achieved along a line bisecting the bottom of the silicon chip, with a 20 μm-high Bi_2Te_3 legs TEC. When such an advanced miniaturized TEC is activated with 10W and enhanced with a 1,250 μm × 1,250 μm mini-contact pad, a 17°C hot spot temperature reduction can be obtained (Wang et al. 2009). However, due to the effect of the heat concentrating/spreading resistance inside the mini-contact pad and the silicon chip, this is the "optimum" geometry for this application and if the mini-contact size is extended to 2,400 μm × 2,400 μm or reduced to 600 μm × 600 μm, the hot spot cooling is decreased to 12°C and 9°C, respectively.

It is also found that achieving low thermal resistance interfaces is critical to the success of mini-contact TEC

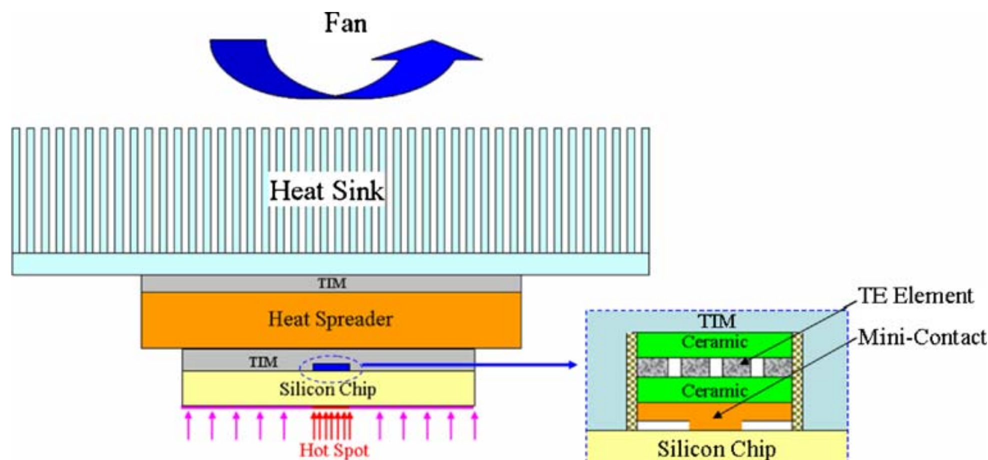

Fig. 1 Schematic of mini-contact-enhanced thermoelectric cooler for on-chip hot spot remediation (Wang et al. 2009)

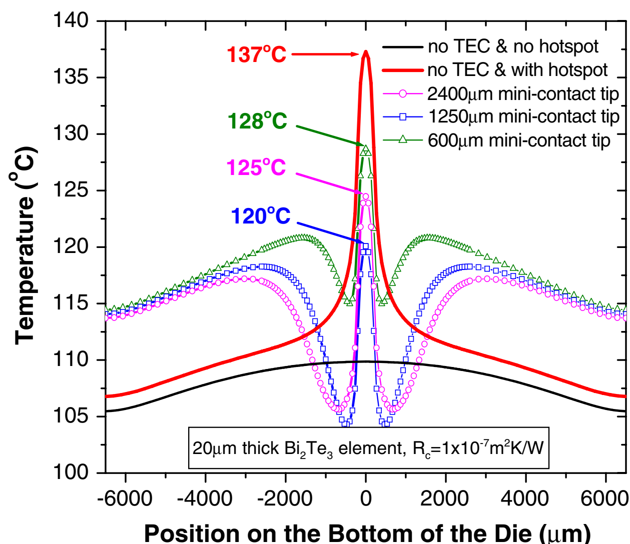

Fig. 2 Effect of mini-contact size on TEC-induced temperature profile (Bismuth telluride leg thickness is 20 μm, silicon chip thickness is 500 μm and input power on TEC is 10 W) (Wang et al. 2009)

cooling, since a high thermal resistance at the mini-contact/chip interface will significantly reduce the effectiveness of the mini-contact enhancement. Moreover, a poor thermal interface between the TEC and the TIM will impede the conduction of thermoelectric and Joule heat into the heat spreader and then into the heat sink and the ambient, raising the temperature of the TEC. Figure 3 displays the interplay between the thermal contact resistance and the maximum achievable hot spot cooling, with the assumption of equal thermal contact resistance at the two interfaces (e.g. $R_{c1} = R_{c2} = R_c$), revealing that with increasing thermal contact resistance at both interfaces, the net cooling achievable on the hot spot diminishes. For the typical configuration studied, the mini-contact is seen to provide excellent cooling with interface resistances below 1×10^{-6} m^2 K/W but to display diminishing returns as the contact resistances increase and to elevate the hot spot temperatures for thermal contact resistances equal to or above 1×10^{-5} km^2/W.

To demonstrate mini-contact enhancement of TEC coolers, 200 μm-thick miniaturized TECs from Thermion (model number: 1MC04-018-02-2200D) (www.thermion-company.com) were tested. The experimentally observed effect of the mini-contact tip size on the temperature reduction at the targeted spot of a uniformly heated chip is displayed in Fig. 4 for three different power dissipations on a 2 mm × 2 mm × 500 μm chip. For the case of no power dissipation on the silicon chip, if the mini-contact is of the same size as the TEC base, the measured maximum spot cooling is about 3.3°C. However, if a 1.8 mm × 1.8 mm copper mini-contact is integrated onto the TEC, 7.1°C maximum spot cooling can be obtained which results in 115% improvement on spot cooling performance. Similarly, spot cooling performance can be improved by 100% and 80% if the power dissipation of the silicon chip is 30 W and 67 W, respectively.

Recently more advanced 130 μm-thick Thermion miniaturized TEC's were used to further test the spot

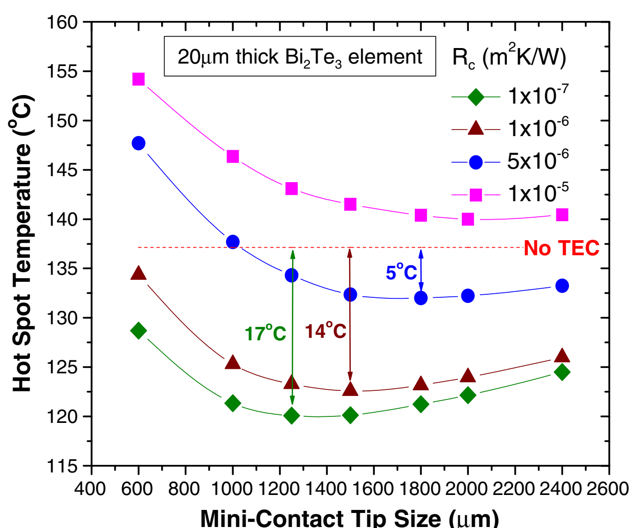

Fig. 3 Influence of thermal contact resistance on hot spot cooling (Bismuth telluride leg thickness is 20 μm and silicon chip thickness is 500 μm) (Wang et al. 2009)

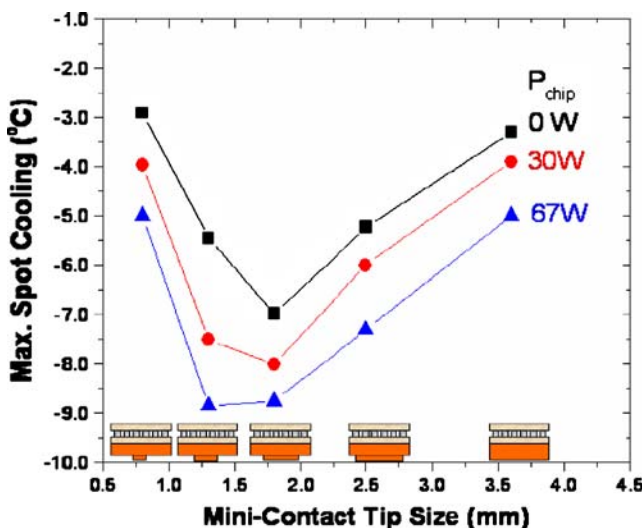

Fig. 4 Variation of measured spot cooling with copper mini-contact size (Bismuth telluride leg thickness of Thermion miniaturized TEC is 130 μm and silicon chip thickness is 500 μm) (Wang et al. 2009)

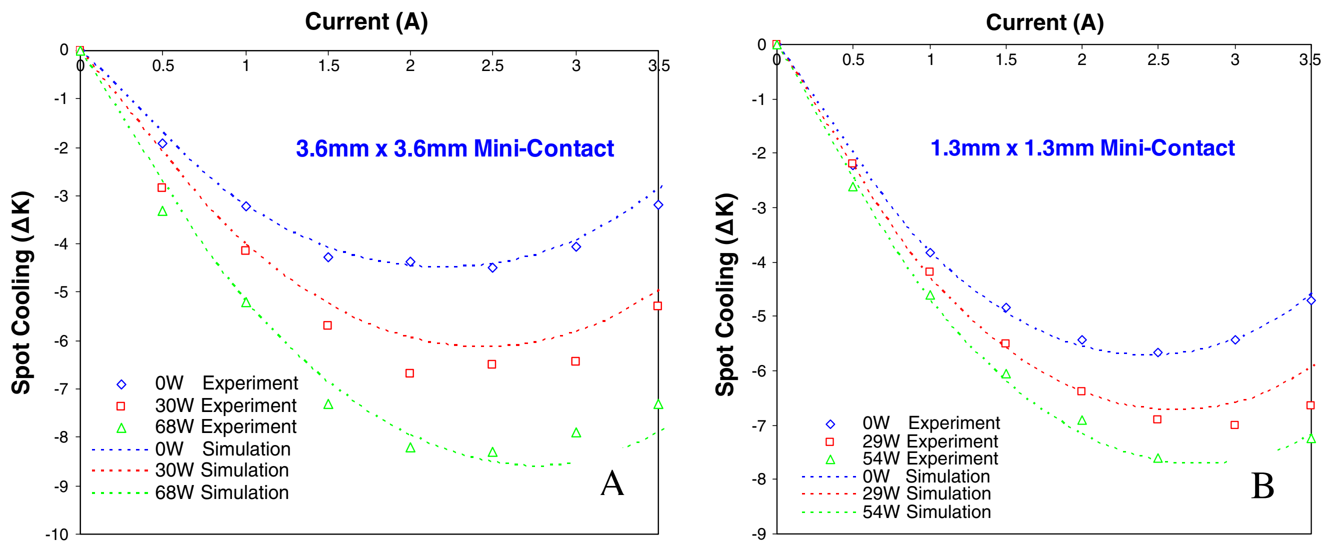

Fig. 5 TEC spot cooling performance with a mini-contact size of **a** 3.6 mm × 3.6 mm. **b** 1.3 mm × 1.3 mm (Bismuth telluride leg thickness of Thermion miniaturized TEC is 200 μm and silicon chip thickness is 500 μm) (Litvinovitch and Bar-Cohen 2009)

cooling capability of a mini-contact TEC. The results displayed in Fig. 5 for 3.6 mm × 3.6 mm and 1.3 mm × 1.3 mm mini-contact sizes, showed very close agreement between the FEM simulations and experiments and revealed that, despite the relatively high contact resistance (9×10^{-6} m^2 K/W and 8.5×10^{-5}m^2 K/W for the 3.6 × 3.6mm^2 and 1.3 × 1.3mm^2 mini-contact tests, respectively) significant cooling of nearly 8°C could be achieved with this configuration (Litvinovitch and Bar-Cohen 2009). Using the calibrated FEM model, the effect of the chip thickness and contact resistance on hot spot cooling performance of the mini-contact TEC was evaluated. As indicated in Fig. 6, for the best thermal interface (with a contact resistance of 1×10^{-7} m^2 K/W) the numerical simulations show that the mini-contact can achieve a maximum of 13.8°C hot spot cooling on a 100 μm thick chip but less than 3°C hot spot cooling on a 500 μm-thick chip. For both chip thicknesses, an increase in the contact resistance to 5×10^{-6} m^2 K/W, decreases the hot spot temperature reduction by approximately 33% and nearly doubles the dimensions of the optimum mini-contact pad.

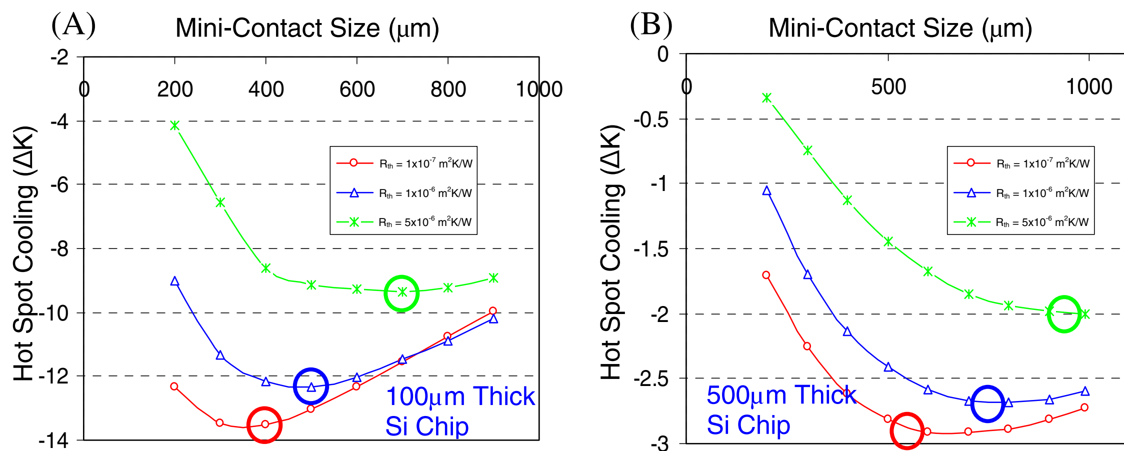

Fig. 6 Effect of chip thickness and thermal contact resistance on mini-contact enhanced TEC hot spot cooling (Bismuth telluride leg thickness is 20 μm) (Litvinovitch and Bar-Cohen 2009)

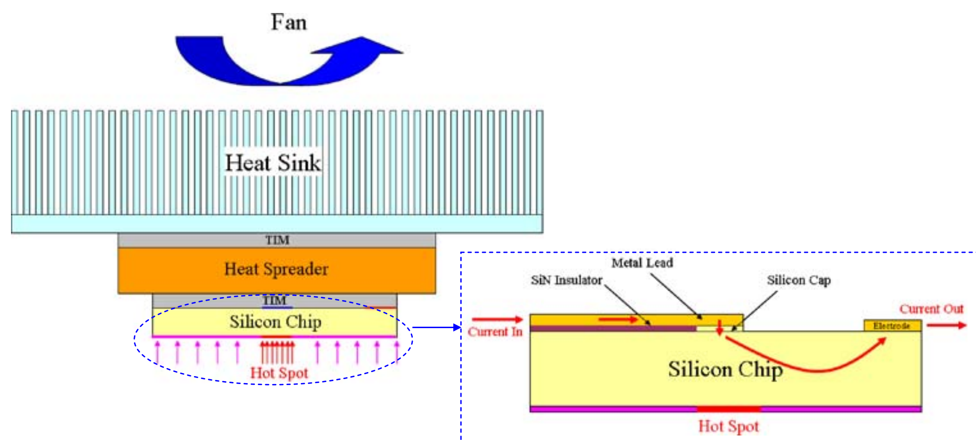

Fig. 7 Schematic of silicon microcooler (The arrows indicate the direction for electric current) (Wang and Bar-Cohen 2007a; Wang et al. 2006c)

In-Plane Silicon Microcooler

The concept of silicon thermoelectric microcooler for on-chip hot spot cooling, fabricated on the back of the silicon chip, is illustrated in Fig. 7, which displays a single microcooler, activated by an electric current entering the silicon chip through the metal lead and the silicon cap, flowing laterally through the chip, and exiting at the ground electrode located on the periphery of the chip (Wang et al. 2006c). The possible use of silicon microcoolers for the remediation of on-chip hot spots is facilitated by the use of well established metal-on-silicon fabrication techniques, yielding a very low thermal contact resistance between the metal and the chip. In addition, incorporation of the silicon chip into the thermoelectric circuit makes it possible to transfer the absorbed energy via the electric current to the edge of the chip, far from the location of the hot spot, thus substantially reducing the detrimental effect of thermoelectric heating on the temperature of the active circuitry.

The thermoelectric properties of silicon material are strongly dependent on doping concentration but modestly on the doping type (Herwaarden and Sarro 1986). The variation of maximum hot spot cooling with doping concentration for various microcooler sizes is presented in Fig. 8 for 100 μm thick chip with 70 W/cm^2 background heat flux and 680 W/cm^2, 70 μm × 70 μm hot spot and the specific electric contact resistance ranging from 1×10^{-7} Ω cm^2 to 1×10^{-4} Ω cm^2,

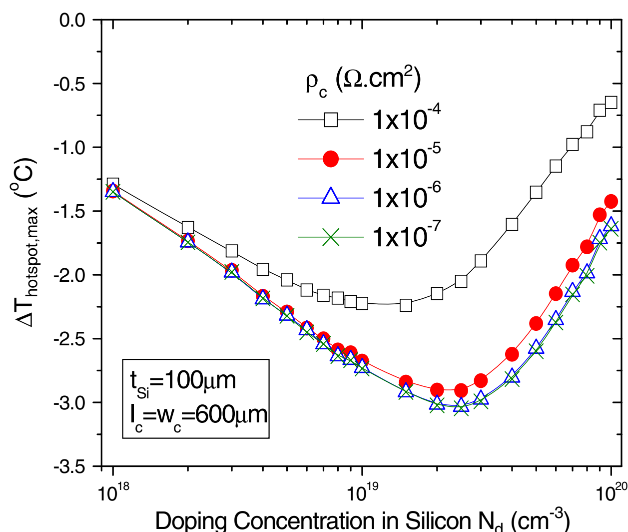

Fig. 8 Hot spot cooling as a function of boron doping concentration for various specific electric contact resistances (Wang and Bar-Cohen 2007a)

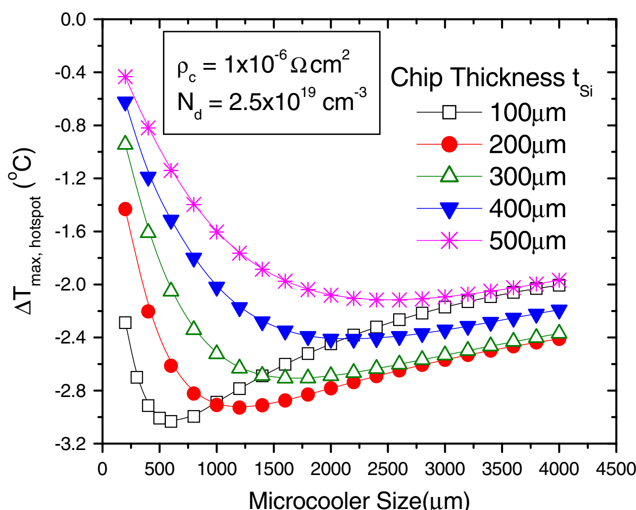

Fig. 9 In-plane silicon thermoelectric hot spot cooling as a function of microcooler size and chip thicknesses (Wang and Bar-Cohen 2007a)

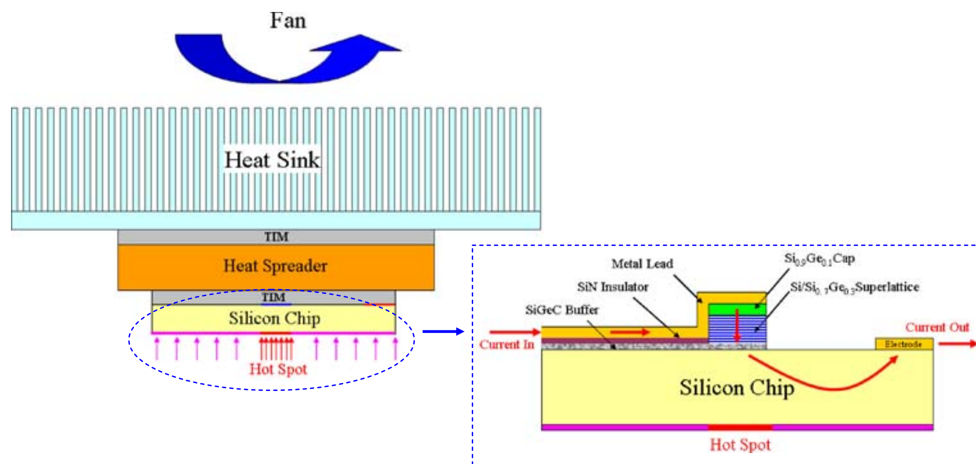

Fig. 10 Schematic of Si/SiGe superlattice microcooler integrated on the top of silicon ship for hot spot cooling (The arrows indicate the direction for electric current) (Wang et al. 2005)

revealing that across the range of microcooler sizes studied, with increasing doping concentration the hot spot cooling increases until reaching a maximum value and then decreases with further increases in the doping concentration.

The effect of microcooler size on cooling performance involves the interplay of thermoelectric cooling by the microcooler and thermal diffusion from the hot spot to the microcooler. Figure 9 displays this behavior and shows the temperature reductions at the hot spot for a wide range of microcooler sizes and silicon chips operating under the background and hot spot heat fluxes of 70 W/cm^2 and 680 W/cm^2, respectively. It is seen that the temperature reduction at the hot spot first increases with microcooler size and, after reaching the maximum value of 3.0°C for 600 μm × 600 μm microcooler, decreases with a further increase in microcooler size. In the application of silicon microcoolers to hot spot remediation, the silicon chip plays multiple roles, functioning as a thermoelectric material, to provide on-chip cooling and, at the same time, as an electrical conductor to transfer electrons from the ground electrode to the microcooler, and as a thermal conductor to provide a diffusion path for the heat generated in the chip to the ambient. Therefore, the chip thickness influences Joule heating distribution inside the chip, heat spreading from the hot spot, heat diffusion from the hot spot to the microcooler, and heat diffusion from the ground electrode, where Peltier heating occurs, to the hot spot. As the chip becomes thinner, the thermal resistance between the microcooler and the hot spot decreases, allowing the microcooler to achieve greater hot spot temperature reductions, e.g., 2.05°C to 3.03°C as the chip thickness decreases from 500 μm to 100 μm, for the conditions of Fig. 9.

Although the in-plane configuration of the silicon does minimize the parasitic effects of "back conduction" (from the hot to the cold side of the TEC), its extremely low ZT value of about 0.01, limits the usefulness of the current silicon microcooler to relatively small high flux "micro" hot spots. Recent breakthroughs in silicon thermoelectrics shows that nanowire structured silicon can reach a ZT value of 0.6 at room temperature and 1.0 at 200 K due to reduction of thermal conductivity (Hochbaum et al. 2008; Boukai et al. 2008). Moreover, it is predicted that it should

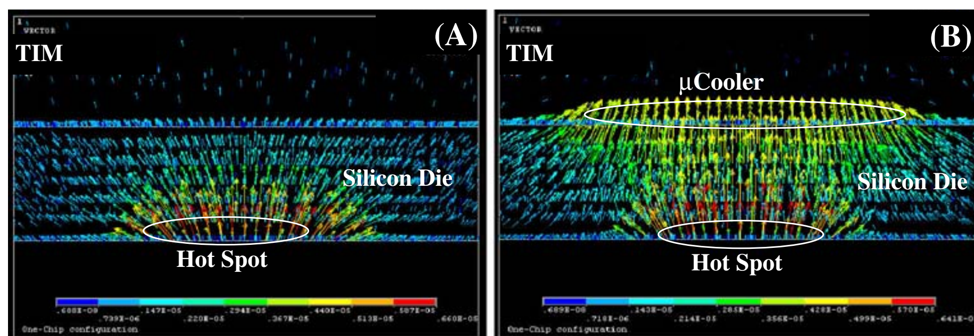

Fig. 11 Hot spot heat flux distribution: **a** without microcooler, and **b** with microcooler powered with 0.6 A. (Hot spot size is 70 μm × 70 μm, chip thickness is 50 μm, and microcooler size is 150 μm × 150 μm) (Wang et al. 2005)

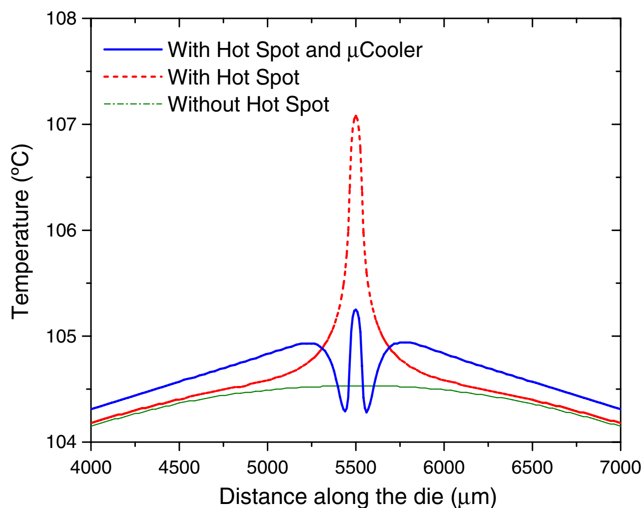

Fig. 12 Temperature profile on the bottom of silicon chip (Silicon chip thickness is 50 µm and the SiGe superlattice microcooler size is 150 µm × 150 µm) (Wang et al. 2005)

be possible to reach even higher values of ZT by optimizing the diameter, doping and other properties of the nanowires. Similar improvements might be possible through the use of functionally-graded doping of the silicon. If such modified silicon nanomaterials can be commercialized and integrated with semiconductor silicon chips, they could enable a dramatic advance in in-plane silicon thermoelectric cooling and make this the technology of choice for thermal management of silicon-based semiconductor devices.

Si/SiGe Superlattice Microcooler

SiGe/Si superlattices have been investigated extensively for more than 15 years due to their unique nanostructure, with very low thermal conductivity and thus high thermoelectric *figure of merit, ZT,* value. However, there are few reports of the on-chip hot spot cooling potential of SiGe/Si microcoolers when integrated into electronic packaging (Zhang et al. 2005). Bar-Cohen, Shakouri and co-workers pioneered this study using the configuration shown in Fig. 10. The corresponding temperature profile along the bottom (active surface) of the silicon chip (11 mm × 13 mm × 50 µm) 70 W/cm^2 background heat flux and 680 W/cm^2, 70 µm × 70 µm hot spot is illustrated in Fig. 11 (Wang et al. 2005; Litvinovitch et al. 2008). It is observed that when a 3 µm thick Si/SiGe superlattice cooler is integrated onto the top of the silicon chip with an optimized applied current of 0.6 A, the hot spot temperature is reduced by 1.8°C, corresponding 80% reduction of the local temperature rise produced by the 680 W/cm^2, 70 µm × 70 µm hot spot. Figures 11 and 12 show the heat flux profile and temperature profile, respectively, around the hot spot and the Si/SiGe microcooler. It can be seen that when the microcooler is not powered, heat spreading from the hot spot dominates while when the microcooler is operating, the heat flux leaving the hot spot is re-directed towards the microcooler. Their studies revealed that for best effect, the Si/SiGe microcooler should substantially exceed the size of the hot spot, thus, serving to not only directly cool the hot spot but also indirectly reducing the temperature of the surrounding silicon.

Bi_2Te_3 Superlattice Microcooler

Recently Chowdhury integrated a 100 µm thick Bi_2Te_3 superlattice cooler into an electronic package to investigate its hot spot cooling capability and the test vehicle is illustrated in Fig. 13 (Chowdhury et al. 2009). The silicon chip background heat flux is 42.7 W/cm^2 and the hot spot is 400 µm × 400 µm with a heat flux of 1,250 W/cm^2. The superlattice TEC consists of p-type Bi_2Te_3/Sb_2Te_3 and n-type $Bi_2Te_3/Bi_2Te_{2.83}Se_{0.17}$ that were grown by metal-organic chemical vapour deposition (MOCVD) on GaAs substrates. The TEC, with a lateral dimension of 3.5 mm × 3.5 mm and a total thickness of 100 µm, was then mounted on a heat spreader and embedded into a layer of thermal interface material when integrated into the electronic package. Figure 14 gives the thermoelectric cooling performance on the hot spot, showing that, at the optimum

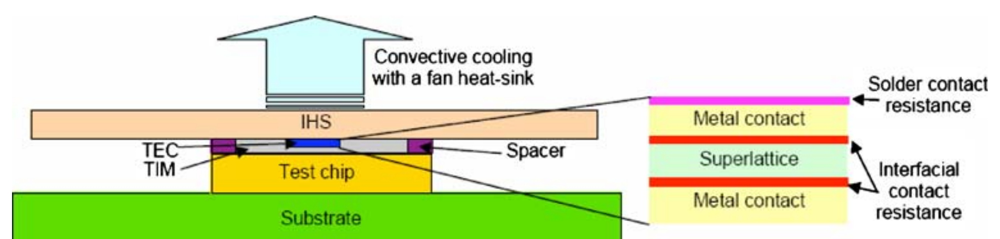

Fig. 13 Cross-section of the electronic test package with the TEC attached to the underside of the integrated heat spreader (Chowdhury et al. 2009)

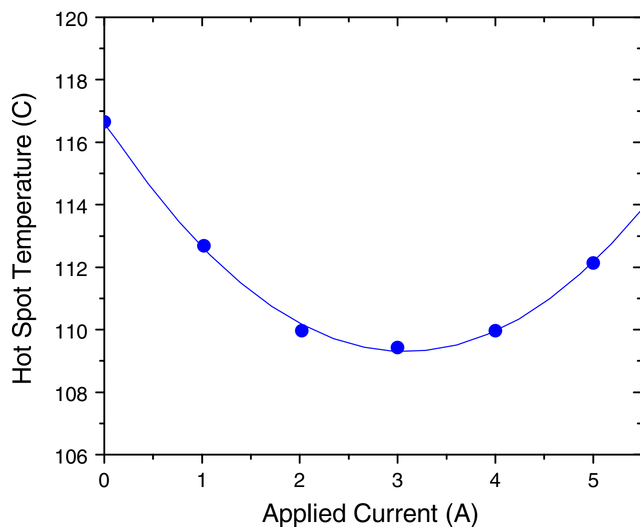

Fig. 14 Temperature of the localized high heat-flux region on the chip as a function of current through the thermoelectric cooler (Chowdhury et al. 2009)

current of 3 A, this bismuth–telluride superlattice TEC can offer an impressive temperature reduction of 7.3°C of a very aggressive hot spot. The authors noted the strong dependence of the cooling capability of such microcoolers on the interface thermal resistance.

Conclusion

Recent advances in development of miniaturized thermoelectric coolers for the thermal management of on-chip hot spots have been reviewed. A number of novel applications and designs of miniaturized thermoelectric components, ranging from mini-contact enhanced μTECs, through in-plane silicon microcoolers, and on to bismuth–telluride superlattice microcoolers, have been discussed from both modeling and experimental viewpoints. The experimentally-observed temperature reductions and model-based predictions of hot spot cooling have shown that such miniaturized thermoelectric coolers are a potent tool in the remediation of on-chip hot spot effects in advanced semiconductor devices.

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