On-chip Phase Change Heat Sinks Designed for Computational Sprinting

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Abstract

Computational sprinting has been proposed to improve responsiveness for the intermittent computational demands of many current and emerging mobile applications by briefly activating reserve cores and/or boosting frequency and voltage to power levels that far exceed the system's sustained cooling capability. In this work, we focus on the thermal consequences of computational sprinting, studying the use of silicon thermal test chips as processor proxies in a real smartphone package with realistic thermal constraints. We study conditions in which multiple cycles of sprint and cooldown are repeated every few seconds to verify the feasibility of sprinting. Integrated on-chip phase change heat sinks filled with low melting temperature metallic alloys are demonstrated to provide a thermal buffer during intermittent computations by keeping the chip at lower peak and average temperatures.

Keywords

Computational sprinting, phase change materials, smartphone, thermal test chips

1. Introduction

Increasing power consumption per chip area has posed a serious thermal management problem in hand-held mobile devices, such as tablets, electronic readers, and smartphones [1, 2], which are constrained by the poor heat dissipation of passive convection. To stabilize device and chip temperatures, clock frequencies are typically lower than those used in laptops and desktops (PCs) [3], and only a fraction of the transistors may be on at any one time (a phenomenon known as "dark silicon" [1, 2, 4]).

Many current and emerging mobile applications, such as web browsing, visual search [5, 6], and handwriting recognition [7], are characterized by short bursts of intense computation punctuated by long idle periods waiting on user input. To improve responsiveness for the intermittent computational demands of these applications, recent research has proposed *computational sprinting* [8, 9, 10, 11], which improves responsiveness by briefly activating reserve cores and/or boosting frequency and voltage to power levels that far exceed the system's sustained cooling capability (known as the thermal design power or TDP). Sprinting exploits thermal capacitance to buffer temporary but significant increases in processor power, dissipating this energy to the ambient after a sprint while waiting for the next user input. For safety, sprinting operation throttles execution after exhausting thermal headroom so that the chip never overheats.

Prior research explored an implementation of computational sprinting in a hardware testbed comprising a modified conventional quad-core Core i7 desktop system [9]. The thermal capacitance of the metallic integrated heat spreader in contact with the silicon chip was used to buffer the heat generated during intense sprints, while phase change materials (PCMs), such as paraffin wax, were used to extend the sprinting duration by utilizing a large amount of latent heat during melting. However, the use of a desktop system as a proxy leads to thermal timescales as long as tens of seconds to several minutes due to the large thermal time constant associated with the system's bulky components, and therefore it is not representative of the mobile platform for which computational sprinting was conceived. Furthermore, the use of a fan for active convection in the desktop system leads to different thermal boundary conditions than those found in mobile devices.

In this work we study the use of a phase change heat sink within a smartphone to explore implementations of computational sprinting in a package with realistic thermal constraints. Although computational sprinting poses various challenges [8] in both hardware (processor designs, power delivery, packaging, etc.) and software (allocation of computing cores, parallel computing, application designs, etc.), we focus here on the thermal consequences of computational sprinting, using integrated on-chip phase change heat sinks to extend sprinting durations.

To implement sprinting, a chip in a mobile device would ideally offer peak power exceeding its sustainable TDP by an order of magnitude or more [8, 9]. Because it is not feasible for existing mobile chips to work at such high power due to current chip designs and the power delivery constraints of mobile batteries, we instead use a silicon thermal test chip (TTC) as a proxy for the smartphone processor. This proxy allows us to apply customized power traces that represent various patterns of intermittent computation and idle states, including power levels exceeding TDP. In addition, PCMs can be easily integrated with TTCs as on-chip phase change heat sinks to manage the excessive heat generated during sprints.

Conventional PCMs like paraffins have been used for thermal management on timescales of more than an hour in systems as small as batteries [12] and solar cells [13] and as large as buildings [14]. Metallic PCMs like Ge-Sb-Te have been used on timescales of microseconds to nanoseconds for non-volatile memories [15]. Few studies, however, have examined the use of PCMs in the sub-second timescale, which is

the range relevant for human perception of mobile device responsiveness. Using conventional PCMs like paraffins or salt hydrates as thermal buffers on this timescale is challenging, because their low thermal conductivities [16] dominate the thermal time constant, requiring small PCM volumes and hence low thermal capacitances. Previous work has examined the use of metal or diamond microchannels [17] or copper-coated fiber mesh carriers [18] to improve thermal conductivity in PCM-based heat sinks. In this work, we use metallic alloys with low melting temperature as PCMs due to their relatively high thermal conductivity and volumetric latent heat [19].

Section 2 describes the TTC fabrication process and experimental setup. Section 3 presents and discusses experimental results. Thermal properties of computational sprinting are first examined while the TTC is suspended in air (Section 3.1), after which the TTC is mounted in a real smartphone package to investigate single and multiple cycles of computational sprinting as well as the TDP of the modified smartphone test bed (Section 3.2). In all the experimental results, comparisons between using on-chip integrated PCM and without using it are shown and discussed in detail.

2. Experiments

Fig. 1 shows the process used to fabricate TTCs with on-chip phase change heat sinks. The TTCs were made from 0.525 mm thick 4 inch silicon wafers with 0.002 mm thick thermally grown silicon dioxide (SiO_2). On the top side of the wafer, 10/100 nm Ti/Pt thin film heaters and resistance thermometers were patterned by photolithography, e-beam evaporation, and lift-off. These top-side components form the test system for generating heat bursts as a proxy for a sprint-enabled smartphone chip as well as measuring the integrated heat sink's thermal response. On the bottom side, 8×8 mm^2 square wells 0.2 mm deep were patterned by back side aligned photolithography and formed by deep reactive ion etching. The wafers were then diced into 10 mm×10 mm chips. An alloy composed of 49% Bi, 21% In, 18% Pb, and 12% Sn (mass percentages) with a melting temperature of 58 ℃ [20] was cut into small pieces (0.115 g), each having a size appropriate to completely fill a well when melted. This alloy is known to have a latent heat of 28.9 J/g, a density of 9.01 g/cm^3, and a thermal conductivity of 10 W/mK [20]. 0.1 mm thick copper tape was used to encapsulate the alloy in the PCM-filled TTCs so that it did not leak after melting. Finally, wires were soldered to the Ti/Pt thin films to apply electrical currents and measure voltages. The integrated PCM does not add extra thickness to the processor, which is critical for consumer mobile device designs. Fig. 1 (f) shows a TTC without etched well and PCM filling, which serves as a proxy for the traditional chip design in order to provide a comparison with the integrated PCM design shown in Fig. 1 (e).

The TTCs were operated by a DC power supply, two solid state relays (SSRs), and a Labview-controlled data acquisition (DAQ) device, as shown in Fig. 2 (a). When SSR 1 was turned on and SSR 2 was turned off, a small constant current was applied to the Pt thin film, representing a mobile processor's idle state. Conversely, when SSR 1 was off and the SSR

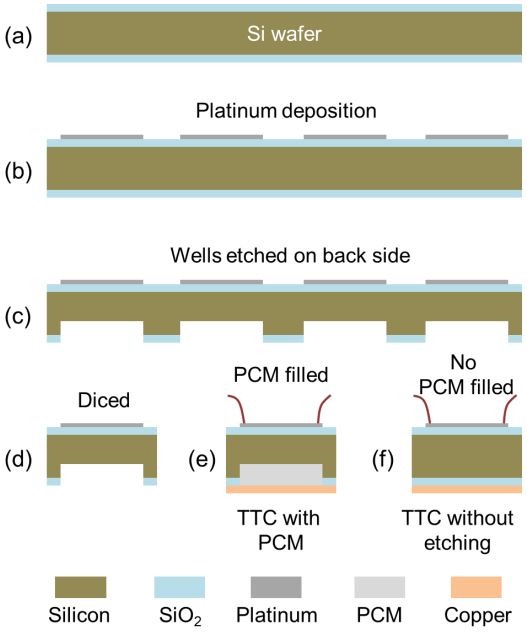

Figure 1. (a) - (e) Fabrication process of TTCs with integrated on-chip phase change heat sinks. (f) TTCs without etched wells or PCM filling are used for comparison.

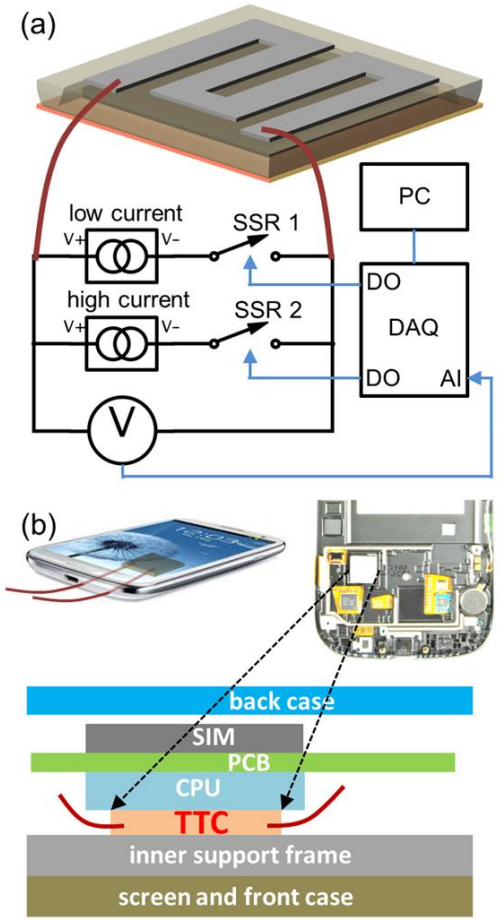

Figure 2. (a) Illustration of the TTC with encapsulated PCM, connected to a PC-controlled circuit used to operate the TTC. (b) Smartphone with TTC mounted inside with cross-sectional view of the TTC-mounted smartphone.

2 was on, a high constant current was applied. Relay switching occurred in less than 1 ms. The voltage drop across the Pt resistor was logged with 1 ms resolution by the DAQ. Because the resistance of the Pt thin film changes linearly with temperature and can be calibrated precisely, the measured voltage can be used to calculate the TTC temperature.

3. Results and discussions

3.1. TTCs suspended in air

To study the performance of the TTC during computational sprinting, a TTC was first operated while being suspended in steady air. The low current used was 20 mA and the high current was 650 mA, while the resistance of the Pt thin film was approximately 26 Ω at room temperature. The idle state therefore consumed approximately 10 mW, while the sprinting state consumed around 11 W. In current smartphones, processor power consumption is approximately 10 – 20 mW when idle and 1.2 – 1.3 W at maximum [21]. This maximum power for all smartphones is limited by the ability of steady-state natural convection to keep the surface at a temperature no greater than that of human hands (~ 35 ℃) [22]. Thus, the power applied to the TTC at idle was realistic for existing smartphone technologies, whereas the power applied during sprinting was nearly an order of magnitude greater than the current smartphone maximum, approximating (for example) ten times as many active cores under parallel computation.

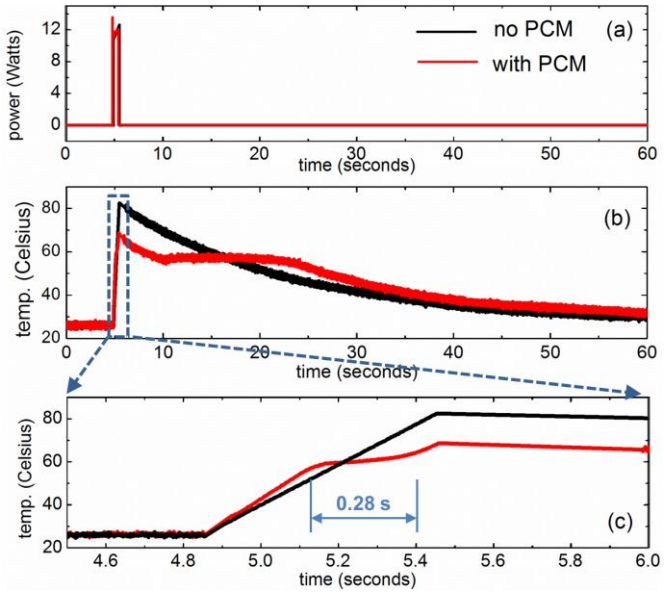

Figure 3. Comparison of two TTCs (suspended in air) under computational sprinting operation, one filled with PCM (Fig. 1 (e)) and the other without integrated PCM (Fig. 1 (f)). (a) Applied power, (b) temperature transients before, during, and after sprinting, and (c) zoomed-in temperature transients.

Fig. 3 compares the temperature transients of two TTCs, one filled with PCM as shown in Fig. 1 (e) and the other without well-etching as shown in Fig. 1 (f). The chips were operated in sprinting mode for 0.6 second, after which they were switched to idle mode to cool down. In Fig. 3 (c), which shows a zoomed-in portion of the temperature plot during the sprint, the temperature of the chip filled with PCM is higher until it reaches the PCM's melting point due to both the lower specific heat capacity and lower thermal conductivity of the alloy as compared to silicon. However, for the chip filled with PCM, the temperature transient has a shoulder of 0.28 seconds at 58 ℃, demonstrating the metal alloy's phase change. Based on its thermal properties, the 0.115 g of PCM used (measured by a precision scale) is predicted to absorb 3.32 J of heat during melting, translating into a 0.28 second phase change for a ~11 W heating power, which agrees well with the experimental results. At the end of sprinting, the temperature of the TTC filled with PCM is 14 ℃ lower than that of the other chip. The benefit of the PCM is reduced if the sprint is longer than the PCM melting time. We note that this integrated PCM configuration is far from optimized, and there is still significant room for improvement. The peak temperature for the TTC filled with PCM can be further decreased, for example, by increasing the amount of PCM (e.g., by etching a deeper well) or by using a different metallic alloy with higher latent heat.

In addition to the sprinting duration, another important metric is the cooldown time required for the chip to cool down to the initial temperature after a sprint [9]. A comparison of the cooling transients of the two chips (Fig. 3 (b)) reveals that although they return to the initial temperature after a similar time of around 1 minute, the PCM-filled chip cools more slowly due to the additional PCM re-solidification time (~ 14 seconds). This 1-minute long cooldown time can be significantly shortened to several seconds through the use of heat spreading materials in a smartphone, as described below.

3.2. TTCs mounted in a smartphone

To study the performance of sprinting in an actual smartphone package, an Android smartphone (Samsung Galaxy S3) was disassembled, and the TTCs described in the previous section were mounted (in separate measurements) on the inner support frame with the copper tape side (PCM side) in contact with the frame, as illustrated in Fig. 2 (b). The frame, made of a metal alloy coated with a thin electrical insulator, acts as a relatively efficient heat spreader to dissipate the heat stored in the PCM due to its high thermal conductivity and high heat capacity. This inner support frame is in contact with the back side of the screen. We note that no thermal grease was used between the TTC's copper layer and the frame to make sure different TTCs have the same thermal contact resistance with the frame, leading to a more fair comparison. The smartphone motherboard was then put back in place so that the side of the TTC with the soldered Pt thin film faced the processor package. Between the processor package and the inner support frame, there was originally a 0.6 mm thick pad of thermal interface material, which was removed to accommodate the TTC. The smartphone was then re-assembled and could be turned on to work normally. The two soldered lead wires extended out of the smartphone to operate the TTC. We note here that the reliability of the alloy and its compatibility with the rest of the smartphone assembly, with regard to factors such as corrosion and wearout, are beyond the scope of this paper and will need further investigation.

3.2.1. TDP of the TTC-mounted smartphone

To provide a baseline for the smartphone modified to have a TTC mounted inside it, we first measured the TDP of the modified smartphone. Both the TTC filled with PCM and the other without integrated PCM were used for comparison. The smartphone was suspended in steady air, turned on, and left at idle with the screen on (auto-brightness) to provide realistic background heating and thermal boundary conditions. A thin thermocouple (0.127 mm diameter) was mounted on the screen's surface by silver paste at a location that was exactly above the TTC. This thermocouple measured the maximum screen temperature of the smartphone, which needs to be maintained within a comfortable range (< 35 ℃ [22]) for human hands. The temperatures of the TTC and the thermocouple were logged, while a number of different constant currents were applied to the Pt heater on the TTC for 30 minutes (separate measurements) to test the TDP until we found the proper one, which was 0.2 A (~ 1.0 W). Fig. 4 compares the temperatures for both smartphone-mounted TTCs (separate measurements) at 1.0 W applied power. The temperatures asymptotically reached steady state while the screen was kept no higher than the body temperature. This applied power of 1.0 W is the TDP of the modified smartphone and also the maximum power for sustained operation, which is used for later duty cycle calculations. Fig. 4 also shows that the chip temperature is 5.5 ℃ higher when using the TTC with integrated PCM because the alloy sandwiched between the TTC's silicon layer and the smartphone's inner support frame has a lower thermal conductivity than silicon (~ 150 W/mK), inducing a higher thermal resistance between the heat source and case. Different alloys with higher thermal conductivity could be used to reduce this effect.

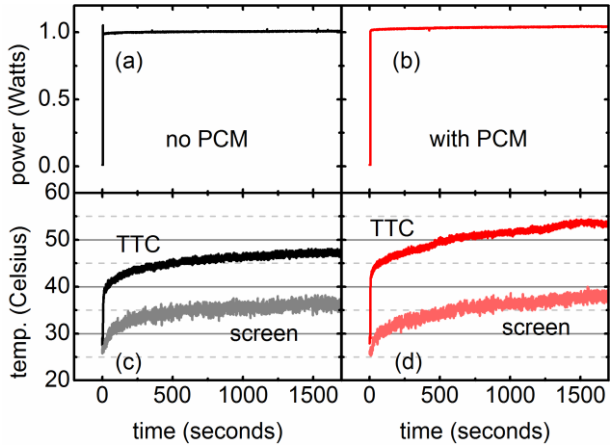

Figure 4. TDP of TTC-mounted smartphones measured by applying a constant current to the TTCs while monitoring the temperatures of both the TTC and the screen. (a) TTC shown in Fig. 1 (f) (without integrated PCM). (b) TTC shown in Fig. 1 (e) (with integrated PCM).

3.2.2. Single sprint

Next, we cycle the TTC mounted inside the smartphone to study its thermal characteristics during a complete sprint and cooldown process. Fig. 5 (a) compares the applied power and measured temperature transients of two smartphone-mounted TTCs, one filled with PCM and the other without PCM. To be consistent with the previously described testing of the TTCs suspended in air, a constant current of 20 mA was applied to the thin film resistor to represent the idle state and a 650 mA current was used for the sprinting state. The sprinting length was again 0.6 seconds.

Fig. 5 (a) shows a single sprint and cooldown cycle of two TTCs; one without PCM shown in black and the other with PCM shown in red. The peak temperature of the TTC without PCM reached 80 ℃ at the end of the 0.6-second sprint whereas the peak temperature of the PCM-filled TTC was only 64 ℃. The PCM-filled TTC takes 0.93 seconds to reach 80 ℃, leading to a 55% sprinting duration extension (not shown in figure). Thus, PCMs can not only store excessive heat to extend sprinting duration, but may also improve a chip's lifetime and reliability by keeping it at lower peak and average temperatures for the same sprinting duration.

Fig. 5 (a) also shows that the time for the TTCs to cool down is significantly reduced due to the rapid heat dissipation of the inner support frame compared to passive convection with air. The cooling transient of the PCM-filled TTC is almost as short as that of the TTC without PCM filling. This result suggests that sprinting using a PCM-filled chip requires little additional cooldown time between sprints.

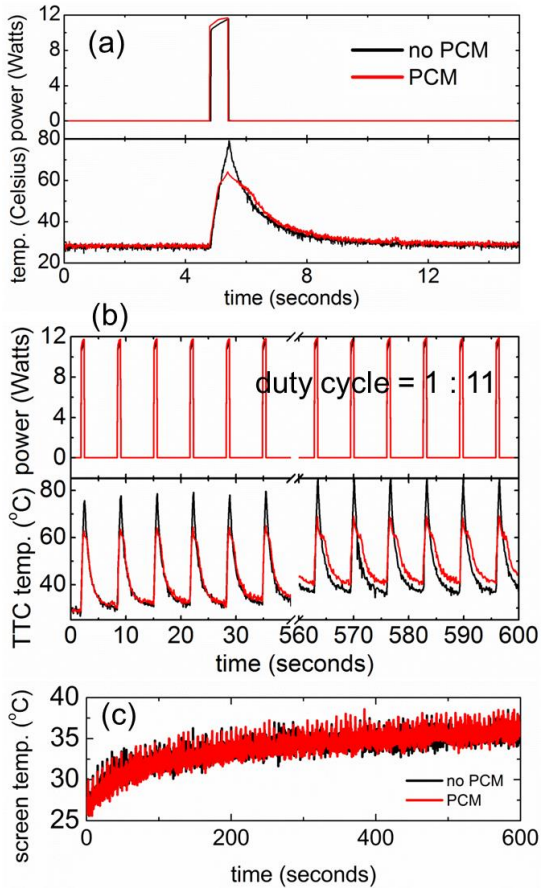

Figure 5. (a) Single sprint of smartphone-mounted TTCs, (b) power and TTC temperatures, and (c) screen temperatures for sprint and cooldown cycles with a sprinting-to-cooling ratio of 1:11 lasting for 10 minutes (only showing the first 40 seconds and the last 40 seconds in part b).

3.2.3. Multiple sprint and cooldown cycles

We now address temperature transients of multiple sprint and cooldown cycles by comparing TTCs with and without PCM filling and study the performance improvement induced by the integrated PCM.

First we consider the case of a TTC without integrated PCM. A duty cycle *D* (sprint length per cycle) no greater than the inverse of the sprint power ratio (sprint power/sustained power) will provide an off percentage large enough so that the TTC has enough time to cool after a sprint, while the peak temperature asymptotically reaches its maximum during continuous sprint and cooldown cycling. Based on Fig. 4, the maximum sustained power is 1.0 W. Thus, given an 11 W sprint power, the maximum duty cycle for this sprint power is 1/11 to ensure the screen is kept at a temperature lower than the human body. Black curves in Fig. 5 (b) show the temperature transients of repeated sprints over 10 minutes with a duty cycle *D = 1:11* (with a 0.6-second sprint length and 6-second cooling time) and sprint power of 11 W, which is equivalent to a sustained power of 1.0 W for average heat energy pumped into the system. The peak temperature of the TTC, at the end of each sprint, gradually increases from 75.6 ℃ to 85 ℃, while the thermocouple mounted on the screen reaches the same temperature as in Fig. 4 (c).

The simplified assumption that the consumed energy is proportional to the computational work (recent work suggests sprinting can finish more work than sustained operation due to a race-to-idle effect [9]) indicates that sprinting would allow a 6 second workload to be completed in 0.6 seconds and potentially improve the user's experience with shortened response times. However, because the relationship between frequency and power of common commercial dual- and quad-core chips is not easy to ascertain, what impact the end-user could experience with real phone applications by sprinting needs further investigation.

Currently, compute intensive mobile applications like speech recognition are routinely deferred to the cloud. A sprinting phone could potentially complete such tasks locally within the acceptable response-time limits of interactive applications. Furthermore, using sprinting to execute typical phone workloads, such as touch screen tracking, web page rendering, application initialization, etc., may also greatly improve responsiveness. Therefore, sprinting can potentially significantly enhance the end-user perception of quality and performance for consumer mobile devices.

Finally, we showed that the performance of multiple sprint and cooldown cycles can be efficiently improved by using the on-chip integrated PCMs. The red curves in Fig. 5 (b) show the same sprint and cooldown operation described in Section 3.2.3 while the TTC mounted in the smartphone has the fabricated on-chip integrated PCM. The same duty cycle *D = 1:11* was used here again. Near the end of the 10 minutes, it clearly shows that PCM not only reduces the peak temperature from 85 ℃ to 69 ℃, but also reduces the rapid temperature variation from a difference of 48.6 ℃ to 27.3 ℃ (improved by 44%) that may reduce stresses associated with thermal cycling.

We note that the duty cycle chosen here is optimized for continuous sprint and cooldown operation of the TTC-mounted smartphone. A smaller duty cycle will work but it does not take the full advantage of computational sprinting. A larger duty cycle, however, will not work because it not only causes a screen temperature higher than human hands, but also reduces the cooling period. With a larger duty cycle, the PCM does not completely re-solidify during the cooling time after several minutes of cycling, remaining in liquid phase throughout the sprint and cooldown operation, which ultimately may result in overheating.

The power-on time (sprint length) in this demonstration also falls in the optimized range for the specific TTC geometry, PCM volume, and PCM property used in this paper. The PCM does not reach its melting point if the sprint length is shorter than 0.3 second as shown in Fig. 5 (a), whereas the junction temperature reaches 80 ℃ if the sprint length is longer than 0.9 second, which corresponds to a power on time that continues sufficiently long after all the PCM completely melts. Thus, the optimized sprint length is from 0.4 to 0.8 second for maximized benefits of the PCM. Therefore, integrated wells of PCM are especially useful for long workloads which originally need multi-second duration execution under conventional sustained operation. To expand sprint length, PCMs with higher latent heat would need to be used, requiring future research on developing new PCMs.

4. Conclusion

We studied the thermal implications of computational sprinting using proof-of-concept TTCs as processor proxies in a real smartphone package. Multiple cycles of sprint and cooldown were repeated to demonstrate the thermal feasibility of computational sprinting. Furthermore, these TTCs incorporated on-chip phase change heat sinks filled with low melting temperature metallic alloy PCMs that can provide a thermal buffer during intermittent computations. Directly integrating the PCM with the chip enables the melting process to completely occur within a second. In addition, PCM-filled TTCs were shown to be able to cool down and resolidify in only a few seconds if mounted inside a smartphone. By keeping the chip at lower peak and average temperatures, integrated on-chip PCMs could potentially improve chip lifetime and reliability.

Acknowledgments

This work was supported by the National Science Foundation under Grant No. CCF-1161505 and No. CCF-1161681.

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